

## Design and Simulation of 64-Point FFT Using Radix-4 Algorithm for OFDM Applications

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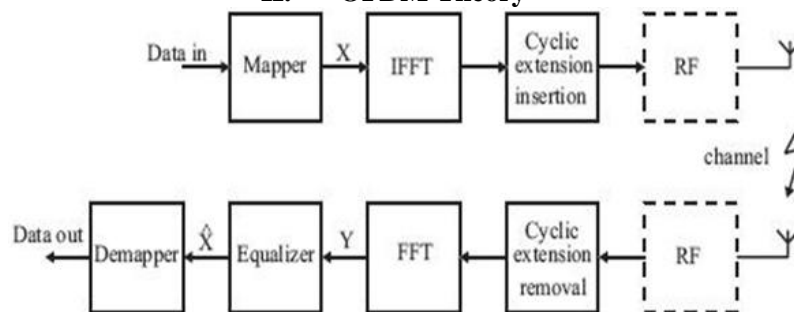
**Abstract:** OFDM technology promises to be a key technique for achieving the high data capacity and spectral efficiency requirements for wireless communication systems in future. Fast Fourier transform (FFT) processing is one of the key procedures in popular orthogonal frequency division multiplexing (OFDM) communication systems. A parallel and pipelined Fast Fourier Transform (FFT) processor for use in the Orthogonal Frequency division Multiplexer (OFDM). Unlike being stored in the ROM, the twiddle factors in our pipelined FFT processor can be accessed directly. The radix 4 FFT is proposed. Finally, the pipelined 64-point FFT processor can be completely implemented using Xilinx 13.2 software.

**Keywords:** OFDM, radix- 4, DIT-FFT, DIF-FFT, Twiddle factor.

### I. Introduction

The Fast Fourier Transform (FFT) are essential in the field of digital signal processing (DSP), widely used in communication systems, especially in orthogonal frequency division multiplexing (OFDM) systems. A computationally efficient version of the DFT is known as the Fast Fourier Transform (FFT) and is commonly used to reduce the computational burden transmitter chip. There are various algorithms to implement FFT, such as radix-2, radix-4 and split-radix with arbitrary sizes. Radix-4 is another FFT algorithm which was to improve the speed of functioning by reducing the computation; this can be obtained by change the base to 4. For a same number if base increases the power/index will decrease. For radix-4 the number of stages are reduced to 50% since  $N=4^3$  ( $N=4^M$ ) i.e. only 3 stages. Radix-4 is having four inputs and four outputs and it follows in-place algorithm.

### II. OFDM Theory



The digital baseband parts of an OFDM transceiver, is shown in Figure. The basic idea of OFDM[2] is to divide the available spectrum into  $N$  orthogonal subchannels. In the mapper, data is converted to signals located in the frequency domain where each subchannel is assigned one signal. The signals are then transformed to the time domain with the inverse fast Fourier transform (IFFT). The FFT is an efficient method to implement the DFT algorithm, based on a divide and conquer approach. The last digital part of the transmitter inserts a cyclic extension to remove the effects of intersymbol interference (ISI) and interchannel interference (ICI). The FFT and the IFFT[7] of length  $N$ , is defined by the equations

$$x_i = \left(\frac{1}{N}\right) \sum_{k=0}^{N-1} X_k W_N^{-ki}, 0 \leq k < N$$

$$X_k = \sum_{i=0}^{N-1} x_i W_N^{ki}, 0 \leq k < N$$

Where, I is the sample index and K is subcarrier index.

### III. Radix-4

- The Radix-4 algorithm decompose a N-point DFT into four (N/4)-point DFT .
- Radix-4 algorithm requires only half as many stages as radix-2 requires .
- No. of stages in radix 4 are  $\log_4 N$ .
- This involves  $(3N/8) \cdot \log_2 N$  complex multiplication and  $(3N/2) \cdot \log_2 N$  complex additions.
- N/4 butterflies are used in each of  $(\log_2 N)/2$  stages, which is one quarter the number of butterflies in a radix-2 FFT.
- The radix-4 butterfly is consequently larger and more complicated than a radix-2 butterfly.
- Addressing of data and twiddle factors is more complex.
- Radix-4 FFT requires fewer calculations than a radix-2 FFT.
- Radix-4 FFT is significantly faster than radix-2 FFT.
- A radix-4 FFT combines two stages of a radix-2 FFT into one, so that half as many stages are required.
- The overall number of operations is lower.

Fig 3.1: A Simple Radix 4 DIF FFT algorithm

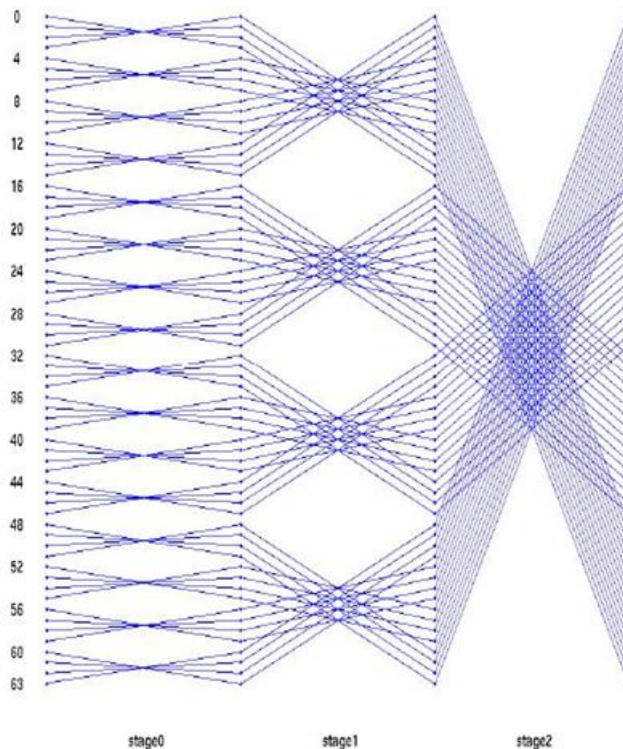
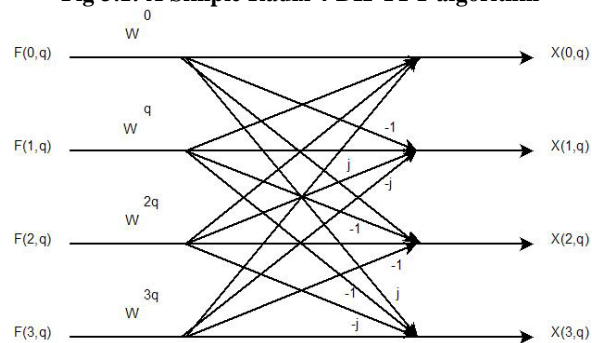
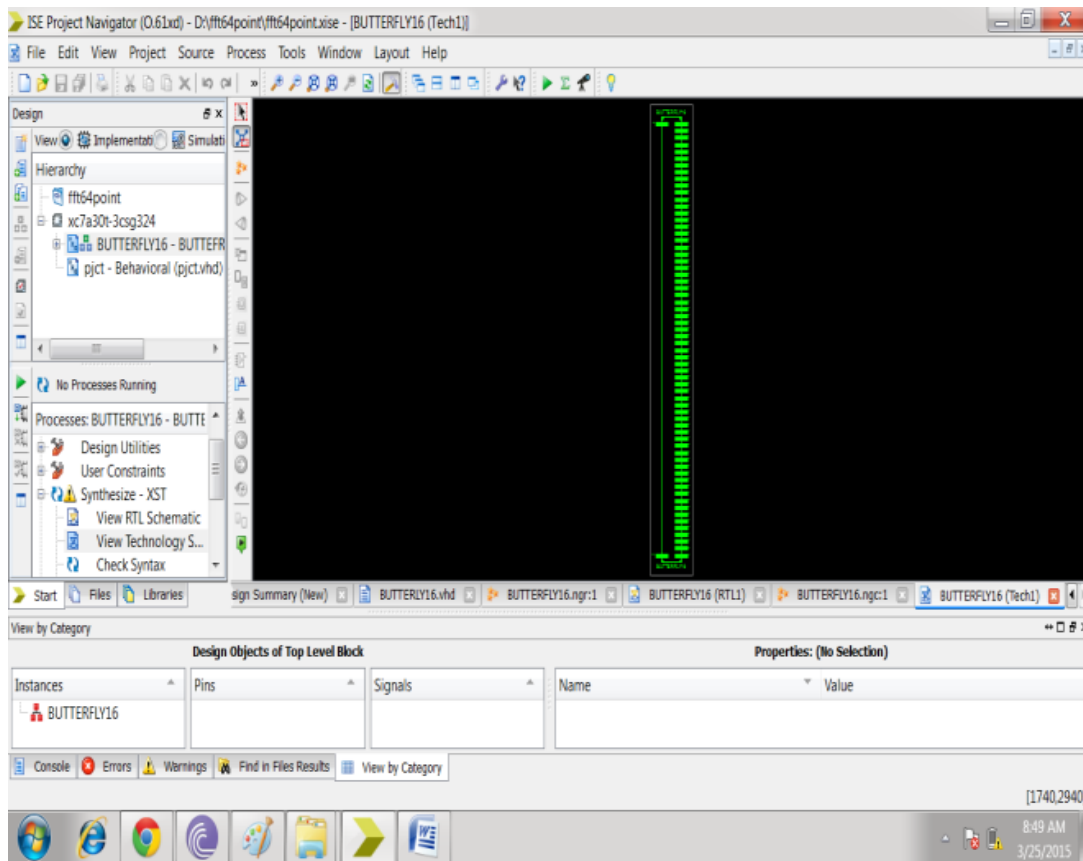


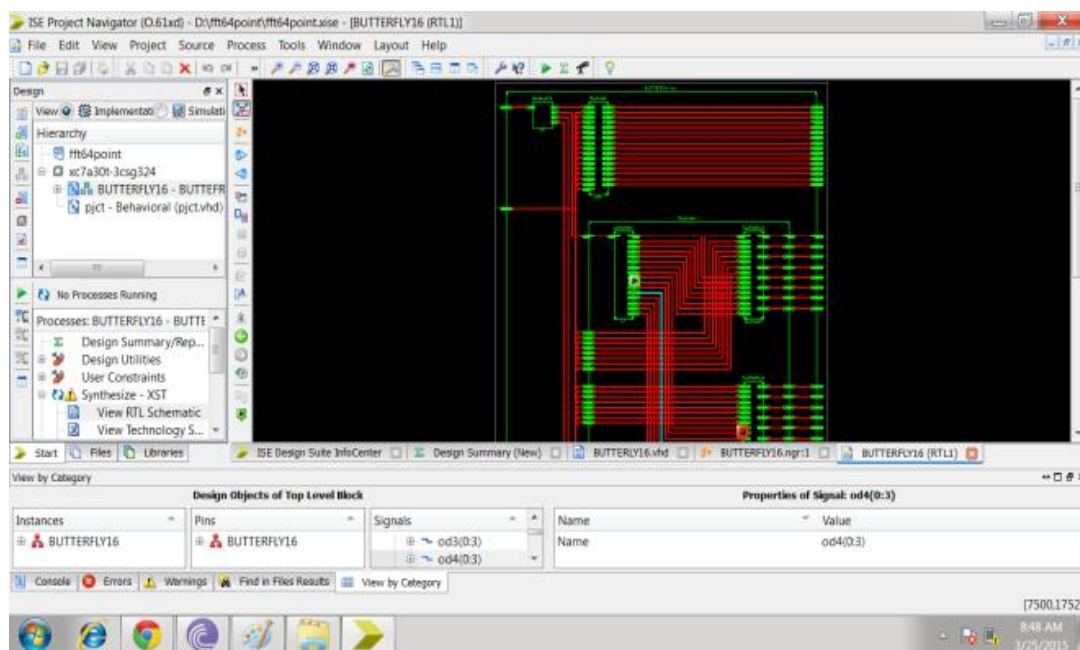
Fig 3.2 : 64point DIT FFT in Radix-4

#### IV. Simulation Results

The proposed FFT block of signal length 64 is been simulated and synthesised using the Xilinx Design Suite 13.2. The RTL block thus obtained for the decimation in frequency domain radix -4 Fast Fourier transform algorithm which is same as time domain is shown - Fig 4.1



The RTL view of the butterfly structure obtained after the simulation of the 64-point FFT block, Decimation in frequency domain which is same as time domain is shown next and also the internal architecture of the butterfly block is shown. Fig





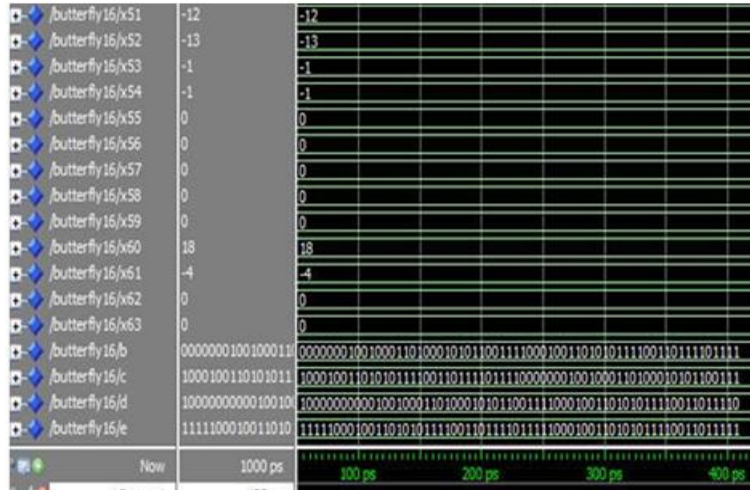


Fig: 4.3(Simulation results)

- Simulation results, 64-point radix-4 DIT-FFT Total time- 7.666ns (6.004ns logic, 1.662ns route)

### V. Results

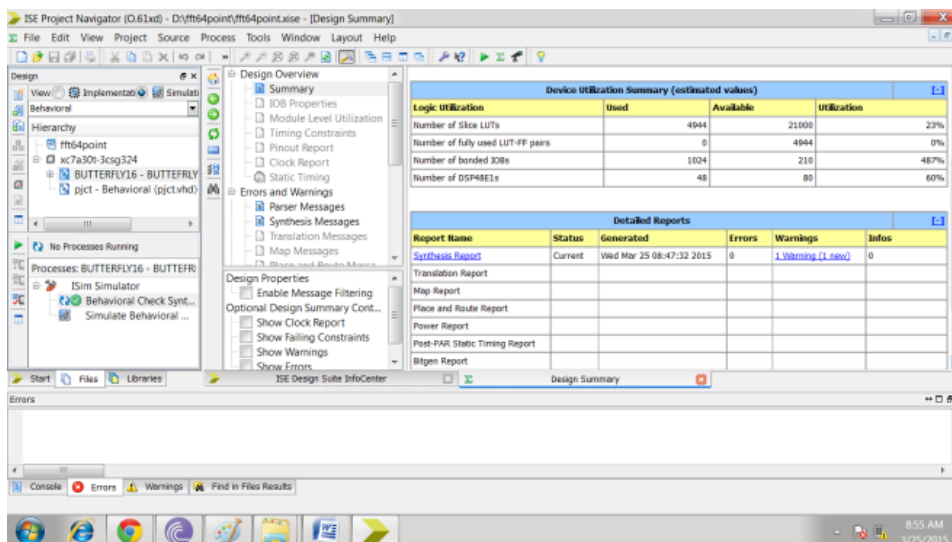
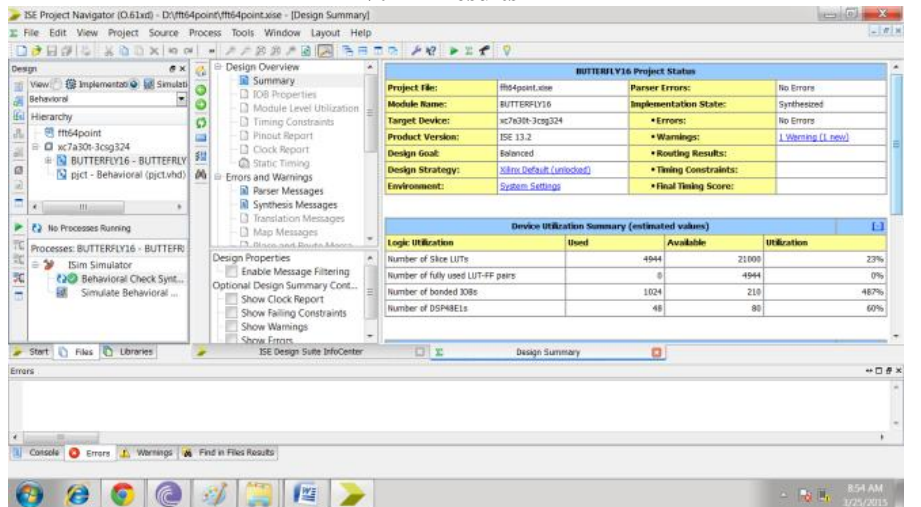


Fig: 5.1(Report)

-: Slice logic utilization:

No of slice luts:4944 out of 21000 - 23%

Number used as logic:4944 out of 21000- 23%

-Slice Logic Distribution: Number of LUT Flip Flop pairs used: 4944.

Number with an unused Flip Flop:4944 out of 4944 100% . Number with an unused LUT: 0 out of 4944 - 0% .

Number of fully used LUT-FF pairs: 0 out of 4944-0% . Number of unique control sets: 0

-:IO utilization:

No of bonded IOB's: 1024 out of 210 - 487%

(overmapped)

## VI. Conclusion

A low power pipelined 64-point FFT processor for OFDM applications has been described in this paper using radix 4 reduce the stages, less voltage, number of additions and multiplications when compared to radix-2. From the above synthesis and simulation results of radix-4 64-points it is understandable that radix-4 having less delay in processing the input when compared with radix-2. Comparing with radix-2 algorithm, 80% of time is saved in radix-4 algorithm. As the delay time is reduced the fastness of the system is increased.

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