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Boosting the Speed of Booth Multiplier Using Vedic Mathematics

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Abstract : *A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. This paper presents a high speed (8x8) modified booth multiplier which is quite different from the conventional booth multiplier. The most significant aspect of the proposed method is that, the developed multiplier is based on Vertical and Crosswise structure of Ancient Indian Vedic Mathematics. It generates all partial products and their sum in one step. This also gives chances for modular design where smaller block can be used to design the bigger one. So the design complexity gets reduced for inputs of larger number of bits and modularity gets increased. The proposed booth multiplier using Vedic mathematics is coded in VHDL (Very High Speed Integrated Circuit Hardware Description Language) and simulated using XilinxISE12.1. Finally the results are compared with conventional booth multiplier to show the significant improvement in its efficiency in terms of path delay (speed). The path delay has reduced by 44.35 % compared to the conventional booth multiplier path delay.*

Keywords : *Booth multiplier, Vedic Mathematics, Urdhva Tiryakbhyam-Vedic formula*

I. Introduction

Multiplication is a fundamental function in arithmetic operations. Arithmetic Functions are currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform (FFT), filtering and in microprocessors in its arithmetic and logic unit. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Hence reducing the time delay and power consumption are very essential requirements for many applications. In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm [1].

The speed of multiplication operation is of great importance in DSP as well as in general processor. In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. There have been many algorithm proposals in literature to perform multiplication, each offering different advantages and having tradeoff in terms of speed, circuit complexity, area and power consumption. Array multipliers, Booth Multiplier are some of the standard approaches used in implementation of binary multiplier.

Section 2 covers the literature survey. Conventional Booth multiplier has been explained briefly in section 3. Section 4 covers Booth multiplier using Vedic mathematics. The results have been discussed in section 5. Conclusion has been given in section 6.

II. Literature Survey

The Urdhva Tiryakbhyam-Vedic method for multiplication strikes a difference in the actual process of multiplication itself. It enables parallel generation of intermed Urdhvaiate products, eliminates unwanted multiplication steps with zeros and scale to higher bit levels using Karatsuba algorithm with processors(compatibility to different data types). This sutra is used to build a high speed power efficient multiplier in the coprocessor [2]. Digital signal processors (DSPs) are very important in various engineering disciplines. Fast multiplication is very important in DSPs for convolution, Fourier transforms etc. Among the various methods of multiplications in Vedic mathematics, Urdhva tiryakbhyam is discussed in detail [2]. The vedic based multiplier is compared with binary multiplier (partial products method).Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. Employing this technique in the computation algorithms will reduce the complexity, execution time, power etc. [3]. SUMBE multiplier [4], the requirement of the modern computer system is a dedicated and very high speed unique multiplier unit for signed and unsigned numbers. Since signed and unsigned multiplication operation is performed by the same multiplier unit the required hardware and the chip area reduces and this in turn reduces power dissipation and cost of a system. A new high speed approach utilizing 4:2 compressors and novel 7:2 compressors for addition has also been incorporated in the same and has been explored [5]. Upon comparison, the compressor based multiplier has been introduced in this paper, is almost two times faster than the popular methods of multiplication.

This paper proposes a design of high speed Booth multiplier using the technique of Vedic mathematics. In this multiplier, the basic multiplication is performed using one of the techniques of Vedic Mathematics. The

Vedic technique, results in a high speed multiplier. Vedic Mathematics is based on 16 sutras, out of which we are using "Urdhva Tiryakbhyam" sutra. In this technique intermediate products are generated in parallel that makes multiplication faster. The proposed multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language) and simulated using Xilinx ISE 12.1 tool. Finally the results are compared with 8-bit Booth Multiplier to show the significant improvement in its efficiency in terms of path delay (speed).

III. Booth Multiplier

Booth algorithm gives a procedure for multiplying binary integers in signed 2's complement representation. It operates on the fact that strings of 0's in the multiplier require no addition but just shifting and a string of 1's in the multiplier from bit weight 2k to weight 2m can be treated as (2K+1-2m). It consists of four registers X, Y, E and Z. Register X and E are initially set to 0. If the two bits are same (11 or 00), then all the bits of X, Z and E registers are shifted to right 1-bit without addition or subtraction. If the two bits differ, then the multiplicand is added to or subtracted from the X register, depending on the status of bits. After addition or subtraction right shift occurs such that the left most bit of X (Xn–1) is not only shifted into (Xn-2), but also remains in (Xn-1). This is required to preserve the sign of the number in X and Z.

IV. Modified Booth Multiplier

Our proposed 8-bit booth multiplier is based upon Vedic mathematics. In this Booth multiplier has been used for the multiplication purpose according to the Urdhva Tiryakbhyam sutra. The approach is different from a number of approaches that have been used to realize multipliers.

4.1. Urdhva Tiryakbhyam Sutra (Vedic Algorithm)

The multiplier can be designed based on the "Urdhva Tiryakbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the binary number system. In this work, the same ideas have been implemented to the decimal number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for (n x n) bit number. Since the partial products and their sums are calculated in parallel and the multiplier is independent of the clock frequency of the processor.

4.2. Vedic Multiplier for (8x8) Bit Module

The (8x8) bit Vedic multiplier module can be easily implemented by using four (4x4) bit Vedic multiplier modules. Let's analyze (8x8) multiplications, say A= (A7 A6 A5 A4 A3 A2 A1 A0) and B= (B7 B6 B5B4 B3 B2 B1B0). The output line for the multiplication result will be of 16 bits as (S15 S14 S13S12 S11 S10 S9 S8 S7 S6S5S4 S3 S2 S1 S0). Let's divide A and B into two parts, say the 8 bit multiplicand A can be decomposed into pair of 4 bits (AH-AL). Similarly multiplicand B can be decomposed into (BH-BL). The 16 bit product can be written as: P = A x B = (AH-AL) x (BH-BL) = AH x BH + (AH x BL + AL x BH) + (AL x BL). Using the fundamentals of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block we can perform the multiplication. The outputs of (4x4) bit multipliers are added accordingly to obtain the final product.

4.2.1. The Steps Followed In Proposed Multiplier

1. Inputs to the proposed multipliers are two 8 bit binary numbers.
2. These binary numbers are unpacked by using binary to BCD code.
3. Multiplication is done according to Urdhva Tiryakbhyam sutra.
4. Multiply the unpacked number by calling the Booth multiplier.
5. Unpack the first step multiplication result to separate sum and carry. Sum is the LSB bit of the final result and carry is added to the next multiplication result.
6. Continue the previous step for step 2 and 3 according to Urdhva Tiryakbhyam sutra.
7. Finally the results are stored.

4.2.2. Flowchart

The flowchart of the proposed multiplier is as shown in figure 1 below.

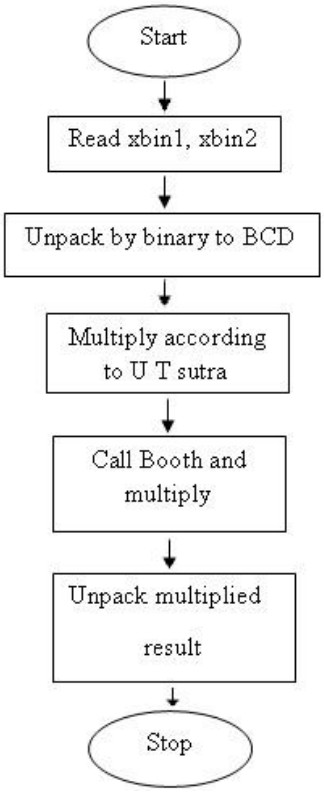

Fig.1 Flowchart for Proposed multiplier

V. Result Analysis

The result analysis is presented in terms of simulation and comparison of the modified booth multiplier with conventional booth multiplier.

5.1. Simulation Results

The multiplication is carried out for integers 88 (01011000) * 88 (01011000) which gives the answer 7744(00100110101000100) as shown in the figure 2. The simulation result indicates that the proposed multiplier is faster than conventional Booth multiplier for Xilinx 12.1, Spartan3 family.

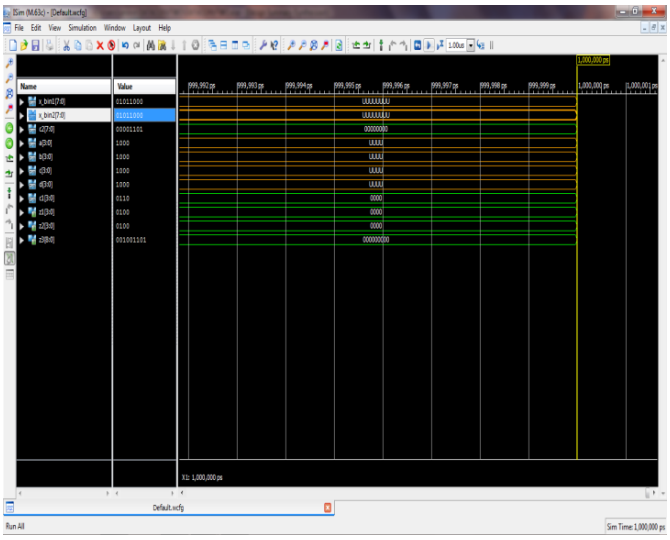

Fig. 2 Simulation result of (8*8) modified booth multiplier

5.2. Comparison between Conventional Booth Multiplier and Proposed Multiplier

The comparison of conventional (8x8) bit Booth multiplier with (8x8) proposed multiplier in terms of computational path delay in nanoseconds (ns) is as shown in table 1. The timing result shows that modified multiplier has the greatest advantage as compared to conventional Booth multiplier in terms of execution time which is as shown in figure 3.

MULTIPLIER	PATH DELAY (ns)
(8*8) bit conventional Booth multiplier	42.57
(8*8) bit modified Booth multiplier	23.69

Table 1 Comparison in terms of path delay (ns)

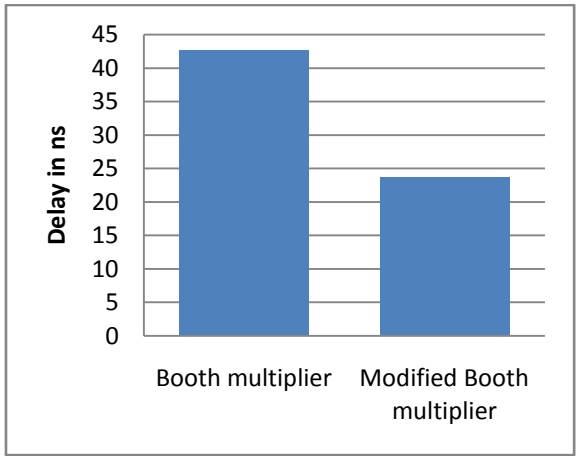

Fig 3 Graphical representation of comparison in terms of path delay (ns)

VI. Conclusion

A high efficient method of multiplication based on Vedic mathematics "Urdhva Tiryakbhyam Sutra (Algorithm)" is presented in this paper. It gives the method of hierarchical multiplier design and indicates that computational advantages offered by Vedic methods. The path delay for proposed (8x8) bit proposed multiplier is found to be 23.69 ns which is less than conventional booth multiplier.

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