Performance Analysis of QPSK Receiver and the effect of Frequency offset on AWGN Channel

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Abstract: *This work tries to evaluate a digital communication system using quadrature phase shift keying (QPSK) modulation and demodulation. It also shows the effect of an Addictive White Gaussian Noise (AWGN) channel with variable frequency offset on the transmitted signal. The work was carried out using MATLAB QPSK model and the effect of varying the frequency offset of the AWGN channel on the bit error rate (BER) was plotted. The transmitted signals are baseband signals and the received signals are in plain text. The text are American Standard Code for Information Interchange (ASCII) codes generated by the bit generator for each frame, transmitted by the transmitter and decoded by the receiver in plain text. The work shows that the level of immunity depends on the frequency offset used in QPSK receiver and least BER recorded at a fixed signal-to-noise (SNR) ratio of 20dB, a frequency offset of 4500Hz.*

Keywords: *Addictive White Gaussian Noise (AWGN), Bit Generator, Demodulation, Digital Communication, Modulation, Quadrature Phase Shift Keying (QPSK)*

I. Introduction

In quadrature phase shift keying, the basic functions for modulation are achieved from two sinusoids (sin and cos). Modulation is achieved by varying the phase of these basic functions which also depends on the message symbols. Modulation in QPSK is symbol based and each symbol contains 2 bits. In QPSK demodulation, the receiver's phase lock loop (PLL) is used to lock to the carrier signal of the incoming frequency and the variation in frequency and phase are tracked.

The objective of this paper is to design a QPSK baseband modulation/demodulation receiver and to show the effect of frequency offset on the bit error rate (BER) for series of transmitted messages that gets to the receiver. Quadrature phase shift keying (QPSK) is a digital modulation technique. Each signal point of a QPSK digital encoding scheme represents two bits and it is bandwidth efficient. It uses a phase shift of 90 degrees multiples and can be expressed mathematically as:

Input bits of '11'

$$S(t) = A\cos\left(2\pi F_c t + \pi/4\right) \tag{1}$$

Input bits of '01'

$$S(t) = A\cos\left(2\pi F_c t + \left(3\pi/4\right)/4\right) \tag{2}$$

Input bits of '00'

$$S(t) = A\cos\left(2\pi F_c t - \left(3\pi/4\right)/4\right) \tag{3}$$

Input bits of '10'

$$S(t) = A\cos\left(2\pi F_c t - \pi/4\right) \tag{4}$$

Where:

$S(t)$ is the complex signal

A is the amplitude

F_c is the carrier frequency

t is the time

QPSK converts the two input binary bits to complex signal $S(t)$. Based on the two binary digits, one out of the four phases of the complex signal is selected and the state of each complex signal is known as a symbol.

1.1. QPSK Modulation

Modulation in QPSK is symbol based. The basic functions for modulation in QPSK are taken as two sinusoids (sin and cos). The QPSK constellation diagram has four constellation points on the X and Y axis. This implies that there is an in-phase component and a quadrature component in the modulated QPSK signal.

1.2. QPSK Demodulation

In QPSK demodulation, the receiver must have knowledge of the carrier frequency and phase of the modulated signal. The receiver achieves this using phase lock loop (PLL). The receiver uses the PLL to access the incoming carrier frequency so as to monitor the variation in frequency and phase.

A QPSK modulation is a modulation where a sinusoidal waveform is varied in phase while keeping the amplitude and frequency constant [1]. Modulating two carriers separately in quadrature (Cos (wt) and Sin (wt)), a QPSK signal can be generated.

A QPSK receiver was described in [2] as a super-regenerative receiver (SR) for QPSK signals. This is as a result of increased attention towards regenerative receivers as an alternative for low-power wireless data links. Super-regenerative receivers are known for their reduced complexity, lesser power consumption and reduced cost. In their analysis, they experimentally verified an SR QPSK receiver using N 1-bit samples of each super-regenerative receiver oscillator (OSR) pulse. Their approach was carried out in the digital domain with low complexity.

In [3], they used a digital PLL to compensate for frequency offset. QPSK partition scheme was explained in [4] for digital phase estimation in a coherent system like quadrature amplitude modulation (16-QAM). However, frequency offset compensation before carrier phase recovery is optimal in order to enhance efficient performance. In [4], frequency estimation technique was used that involves only a subset of the 16-QAM symbols with the QPSK partition. It was demonstrated to be an effective technique when applied prior to the carrier phase recovery.

II. System Architecture

The proposed QPSK system architecture (Fig. 1) consists mainly of transmitter subsystem, channel subsystem, receiver subsystem and display.
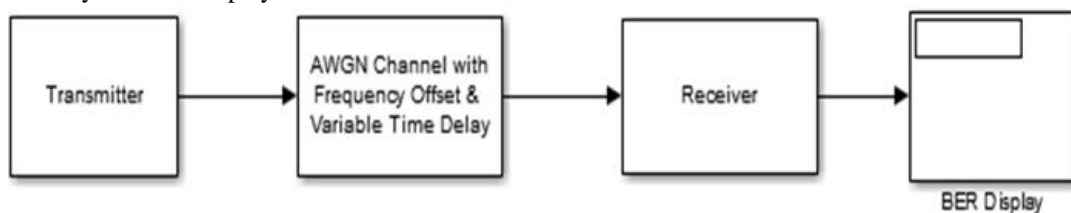

Figure 1: Proposed QPSK system.

2.1 Transmitter subsystem

The diagram (Fig. 2) shows the transmitter subsystem. The transmitter subsystem consists of raised cosine filter block, QPSK modulator block and bit generation subsystem. The QPSK modulator block modulates the input signal using the quadrature phase shift keying method. The raised cosine filter block filters the input signal using square root raised cosine finite impulse response (FIR) filter.

2.1.1   Bit Generation

The bit generation subsystem makes use of a MATLAB script for its implementation and it consists of a unipolar barker code that outputs a constant specified by the parameter of the constant value. It also have a repeater block, a frame conversion block that sets sampling mode of the output signal, a scrambler whose configuration is specified by the parameter of scramble polynomial and accepts a scalar or column vector input signal. The bit generation subsystem is concatenated to create a contiguous output signal which could be in vector or multidimensional array mode. The bit generator makes use of ASCII that sends the message (signal) through the channel, decoded by the receiver and converted into plain text. This is depicted in Fig. 2.
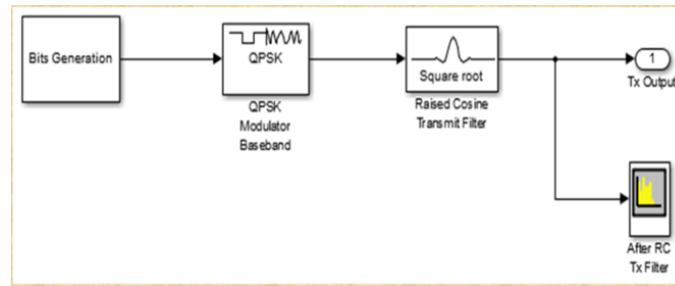
Figure 2: Transmitter subsystem.

2.2 Channel Subsystem

The diagram (Fig. 3) shows an AWGN channel subsystem with frequency offset and variable delay. The channel subsystem consists of phase/frequency offset, delay generator, variable fractional delay, gain and AWGN. The channel uses phase and frequency offset for signal transmission. It then adds a variable delay by using a triangle delay or ramp delay. The triangle delay changes back and forth linearly from minimum delay samples to maximum delay samples at a rate corresponding to the delay step sample of each frame while the ramp delay set at delay start samples and linearly increases at a rate corresponding to the delay step samples of each frame. The receiver's performance is affected by the use of multiple delay characteristics most especially on the timing recovery blocks.
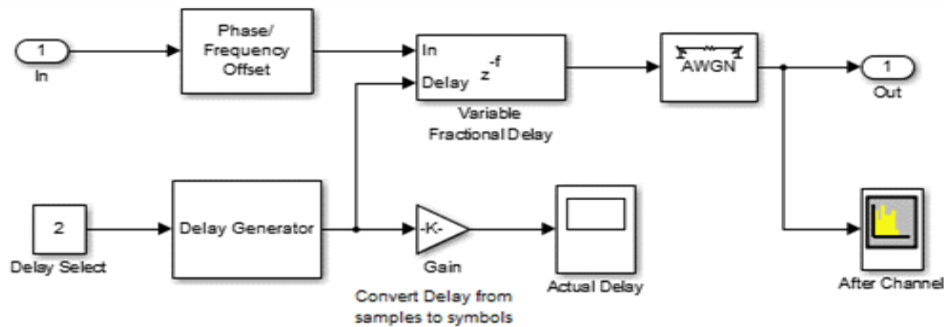

Figure 3: Channel subsystem

2.2.1 Delay generator

The delay generator is a subsystem in the channel subsystem and it consists of multiport switch, delay select, variable ramp, repeating sequence stair and delay.

2.3 Receiver Subsystem

The receiver subsystem does the signal correction for a signal that has been corrupted by the impairments introduced by the channel. The receiver accomplishes this by the use of raised cosine receiver filter, automatic gain control (AGC), coarse frequency correction/compensation, fine frequency correction/compensation, phase error detector (PED), timing recovery and data decoding.
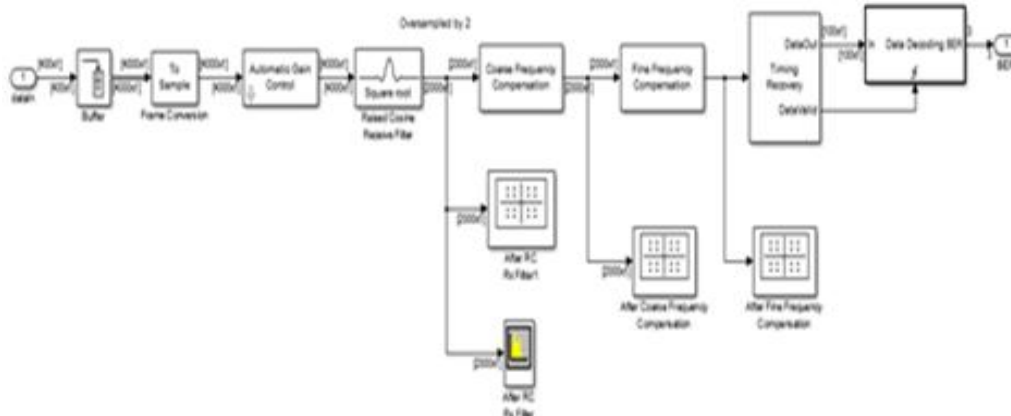

Figure 4: Receiver subsystem

2.3.1 Raised Cosine Receiver Filter

The raised cosine receiver filter is responsible for down-sampling of the input signal. The input signal is down-sampled by a factor of two and the transmitted waveform is matched filtered by the raised cosine receiver filter. The raised cosine receiver filter has the tendency to reduce intersymbol interference (ISI) and it is a filter that is used in digital modulation for pulse shaping. Describing it mathematically, it is a cosine function because of the non-zero portion of its frequency spectrum. The spectrum of the raised cosine receiver filter shows odd symmetry about 1/2T where T is the period.

In frequency domain, it can be described as:

$$H(f)f(x) = \begin{cases} T \\ \frac{T}{2}\left[1 + \cos\left(\frac{\pi T}{\beta}\left[|F| - \frac{1-\beta}{2T}\right]\right)\right] \\ 0 \end{cases} \tag{5}$$

$$|F| \le \frac{1-\beta}{2T} \tag{6}$$

$$\frac{1-\beta}{2T} < |F| \le \frac{1+\beta}{2T} \tag{7}$$

Where β is the roll-off factor
T is the period.

2.3.2 Automatic Gain Control

The AGC is a regulatory circuit in a close-loop. Despite the amplitude variation in the input signal, it serves to maintain a controlled amplitude signal at the output. In this simulation, optimum loop design is achieved by making the amplitude signal of the carrier recovery at the inputs and timing recovery loops stable. The input amplitude of the coarse frequency correction /compensation is a fraction of the up sampling factor. The AGC achieves this by keeping constant the timing error detectors and the phase gains over a period of time. As seen from the diagram above automatic gain control (AGC), the AGC is situated before the raised cosine receiver filter. This is to enhance the accuracy of the estimate and to ensure that an oversampling factor of four is used to measure the amplitude signal.

2.3.3 Coarse Frequency Compensation

The Coarse frequency compensation subsystem uses a rough estimate of the offset to correct the input signal. The coarse frequency correction/compensation subsystem is composed of fine frequency offset and phase/frequency offset. The fine frequency offset has a subsystem (Fig. 4) that is controlled with a MATLAB script. This subsystem compensates for the residual frequency because after coarse frequency compensation, there is a residual frequency offset.

2.3.4 Fine frequency compensation

In electrical engineering, fine frequency compensation serves to prevent amplifier from oscillating and to regulate overshoot in the step response of the amplifier. It also serves to enhance the bandwidth of single pole systems. The residual frequency offset is been tracked by the fine frequency compensation through the use of a phase-locked loop (PLL). The input signal phase offset is also tracked by the fine frequency compensation. It consists of an unbuffer, complex phase shift, a loop filter subsystem, direct digital synthesizer (DDS) and phase error detector (PED). The phase offsets and residual frequency are been offset by the compensation phase generated by the DDS. The PLL uses the DDS to achieve this purpose. The PED is implemented using MATLAB script.

2.3.5 Timing Recovery

To achieve symbol synchronization is the main purpose of timing recovery subsystem. The receiver uses sampling frequency and sampling phase to achieve symbol synchronization. Timing recovery eliminates ISI by sampling the symbol at the center of the symbol period. To correct the timing error in the receiver signal, the timing recovery uses the PLL. For every two input samples, the timing recovery subsystem creates one output sample. The timing recovery subsystem is made up of timing recovery PLL, modified buffer and member valid samples. The control signal is generated by the modified buffer and the timing error detector (TED) uses this control signal to calculate the timing errors at the correct timing instants. The interpolants makes the timing error detector to generate errors. An extra or missing interpolant is seen at the output when the delay is at symbol boundaries. The TED uses bit skipping to address this issue. A total of 100 QPSK symbols per frame are generated by the timing recovery. This can be estimated to be an output symbol for every two input samples. At the input sample rate, there exists a timing strobe that is sent to the output by the timing recovery loop. The timing strobes are value in alternating ones and zeros under normal conditions. The sampled QPSK symbols are filled up by the modified buffer using the timing strobe.

2.3.6 Data Decoding

This subsystem performs many functions. They functions include but not limited to demodulation, compute delay, frame synchronization, text message decoding, descrambling and phase ambiguity resolution. The bit generator subsystem produces a QPSK modulated barker code for data decoding. This is used to realize frame synchronization and correlate the received QPSK symbols. The delay is found by using the peak amplitude index in the compute delay subsystem by correlating the QPSK modulated barker code with the data input. An unmodulated carrier may be located by the PLL of the fine frequency compensation subsystem that have a phase shift of 0, 90, 180 or 270 degrees. This phase shift has the tendency to cause phase ambiguity. However, this phase shift is determined by the phase offset estimator subsystem. The corrected data is demodulated by the estimated phase offset in the subsystem of the phase ambiguity correction and demodulation by rotating the input signal.

2.3.7 Display

The display consists of the scope and spectrum analyzer. They are used to output the various results of the input signal components that they are attached to with respect to simulation time.

III. System Modeling And Simulation

In modern engineering system design, modeling and simulation are inevitable tools. System simulation and modeling optimizes system design and concepts are explored through the use of simulation and modeling.
In this evaluation, the ASCII codes (baseband signals) are generated at the bit generation subsystem at the transmitter. The bit generation subsystem are concatenated to create a contiguous output signal where each data frame contains 26 synchronization bits header and 174 data bits that could be in vector or multidimensional array mode. These baseband signals are transmitted through the AWGN channel. The channel uses phase and frequency offset for signal transmission. At the channel, a variable delay using triangle delay is added and it changes back and forth linearly from minimum delay samples to maximum delay samples at a rate corresponding to the delay step samples of each frame. This usually affects the receiver's performance. The receiver does the signal correction due to impairments introduced by the channel. The receiver uses timing recovery to achieve symbol synchronization and the timing errors are corrected using the PLL. A total of 100 QPSK symbols per frame are generated by the timing recovery. The receiver demodulates the transmitted signal using data decoder which also performs frame synchronization, descrambling and phase ambiguity resolution. The QPSK modulated barker code produced by the bit generator are used by the data decoder to realize frame synchronization and correlate the received QPSK symbols before converting it to plain text
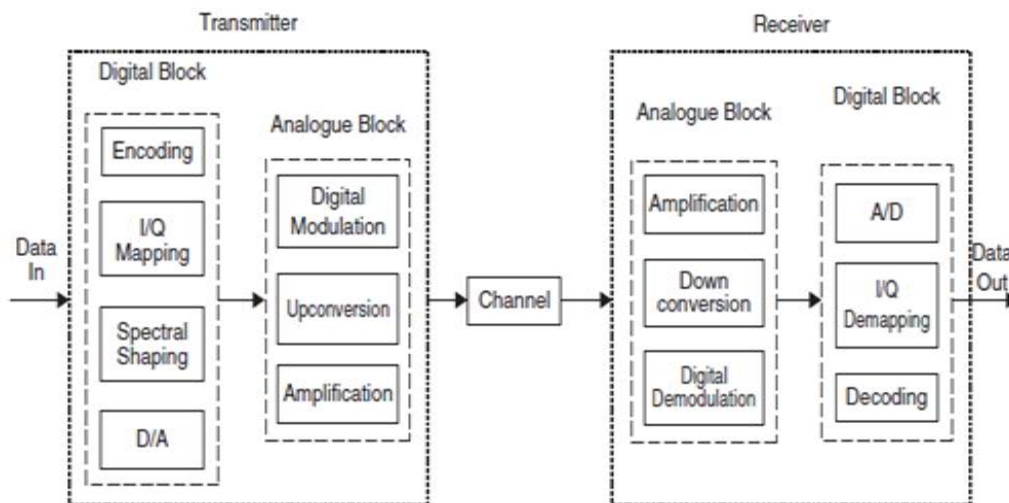

Figure 5: Basic blocks in communication systems [5]

IV. Results And Analysis

This section describes the result of the digital baseband communication system using QPSK modulation. From the result (Fig. 6) each data frame of the transmitted ASCII data code contains 26 bits header mostly for the purpose of synchronization and 174 data bits. The first 105 bits contain "World peace ###" message (where ### represents 000 to 099 repeating sequence). A scrambler was used to improve data transition density and frequency offset estimation.

The diagrams (Fig. 6 and 7) shows that the ASCII transmitted data were successfully received by the QPSK receiver despite impairments introduced by the AWGN channel. The QPSK model was able to

successfully recover the bits corrupted by channel impairments with just few bit in error.

The diagram (Fig. 8) shows the bit error rate measurement with respect to a change in frequency offset. It indicates the number of bits in error at a given frequency offset.
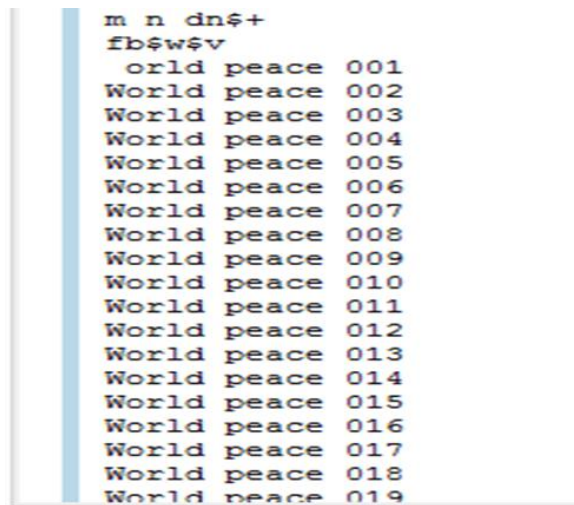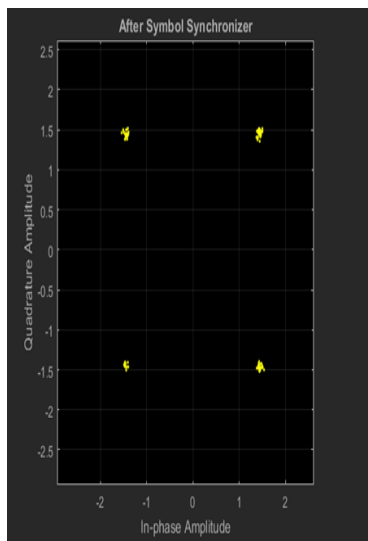

Figure 6: Received signal

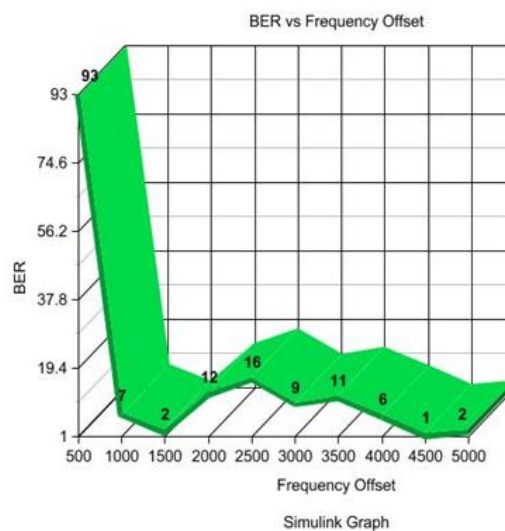**Figure 7:** Received constellation point diagram

Figure 8 BER and frequency offset graph

V. Conclusion

This work evaluates how a QPSK model can successfully transmit and receive baseband signal and recover from impairments introduced by the channel. It also looks at the effect of frequency offset on BER measurement. It can be deduced from simulation that the QPSK receiver model have some level of noise immunity that depends on the frequency offset used and were able to recover 99.8% bits corrupted by channel impairment. From the results of the simulation, at a fixed signal-to-noise (SNR) ratio of 20dB, a frequency offset of 4500Hz gave the least BER. Choosing the right modulation and frequency offset can improve the BER.

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