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Ultra High Frequency Tera/Zetta Hertz Multichannel Long Periodicity PRBS Transceiver – $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 For Advanced Long Distance Satellite Wireless Communication

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Abstract:
Recent years Design verification engineers and scientists facing challenge on effective quality moderate long distance high speed high frequency wireless communication system designs to get original high quality modulated and demodulated serial/ parallel signal with effective frequency bandwidth spectrum and baud rate data transfer without signal loss/ distortion, signal interference noise and degradation, timing violations, glitches, crosstalk, frequency notes, Bandwidth spectrum etc. Due to we proposed new Identification of property of Ultra high frequency carrier wave-based Tera/ zetta hertz PRBS transceiver – $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 for Advanced digital satellite wireless communication systems. The PRBS transceiver /codec consists of transmitter and receiver. The PRBS transceiver ASIC for ultra-high-speed long-distance communication Hi-tech Smart computing products like Cloud & Internet Computing, LTE ASIC, OFDMA/ WCDMA, QCDMA, GPS Satellite Technologies etc. Basically, This Design Contains Tera/ zetta hertz clock frequency synchronized PRBS Transmitter and Receiver of Different PRBS Tapped Sequences existing ones are $2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 etc as well proposed one's are $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 etc and the Multiplexer on the transmitter side and De-multiplexer on the receiver side. These different pattern sequences are Designated as per CCITT ITU Standards. Design compilation, simulation and synthesis done by leading EDA software design tools (Synopsys 2021.1v) as well design flow Implemented by Xilinx ISE 9.2i IDE Software and RTL Design verification done by System Verilog HDL
Background: The Ultra high frequency Tera/Zetta Hertz multichannel PRBS transceiver mainly used for long distance wireless communication system for multiple satellite users by using Pseudo random binary sequence tapped patterns $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 for generation of Ultra high frequency carrier waves to protect low frequency base band signal messages for mutiple lacks of distance kilometers based digital satellites. Why this is because we can easily transmit and receive large signal message data stream information with out any glitches/hazards, signal interference, degradation, signal noise traffic collisions while transmitting and receiving due to efficient effective high quality modulation and de-modulation done at transmitter as well at receiver side.
Materials and Methods: We have used various advanced EDA Software design automation tools Synopsys VCS 2021.1v and Xilinx ISE 9.2i for compilation, simulation, logic synthesis as well floor planning and placement routng. We have implemented Verilog/System Verilog HDL RTL Design method for design of the PRBS Transceier.
Results: We have designed and verifyied the functionality of PRBS transceiver using RTL Design and Test bench and generated signal outputs serial and parallel for both transmitter and receiver.
Conclusion: The RTL Design and Verification of PRBS Transceiver designed using long Periodicity PRBS Pattern Seed words-are $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 for ultra high long distance space/satellite distance applications/products

Keyword: *PRBS Pseudo Random binary sequence, ASIC Application specific integrated circuit, CCITT-Consulting committee for international telegraph and telephone, ITU- International telecom unit, HDL-Hardware description language,*

Date of Submission: 08-04-2024 Date of Acceptance: 18-04-2024

I. Introduction

In Modern Hi-tech Wireless Space/ Satellite Communication Systems, High Speed Data Communication is very Important for future long distance wireless serial and parallel data communication equipment application products for improvement of system bandwidth and Performance, Data Speed is in terms Giga/Tera/ Zetta number of Bits transmitted and received per second, Due to we proposed new Long periodicity seed word pattern based $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 Ultra High Frequency Tera / Zetta Hertz Clock PRBS Transceiver. The advantages are reduction of noise, bit slips, jitter error rate and generate quality eye diagrams of PRBS Transceiver. Why we choose long periodicity seed word PRBS patterns to generate efficient carrier waves and Qualiity modulation at transmitter and demodulation at Receiver due to there should not be any signal integrity problems, signal to noise ratio, AWGN, Improvement Spread spectrum bandwidth and spectral efficiency for multi users. This is parallel communication computing at a time multiple prbs transmitters and receivers communicated using above sequences.

PRBS RTL Design Architecture

[A] PRBS Transceiver RTL Design Architecture Proposed method-1

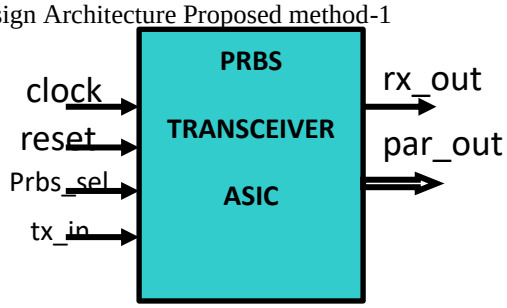

Figure 1. PRBS Transceiver RTL Design

Description: The Multi channel PRBS Transceiver consists Transmitter and receiver of different PRBS patterns- $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 NRZ. The data input transmitted and received serially in the form bit by bit. On the Transmitter side the transmitter accepts low frequency base band signal multiplex/modulate with high frequency PRBS Carrier waves of different PRBS Tapped sequence elements/seed word patterns to generate high frequency modulated transmitter output. On the Receiver side the Receiver accepts the modulated transmitter ouput signal and De-multiplexed/demodulate with different PRBS Carrier wave sequence patterns of above mention to get original low frequency base band signal with out any noise/ distortion/ glitches. Etc..

[B] Proposed PRBS Transceiver Detailed Design Architecture-Method-1

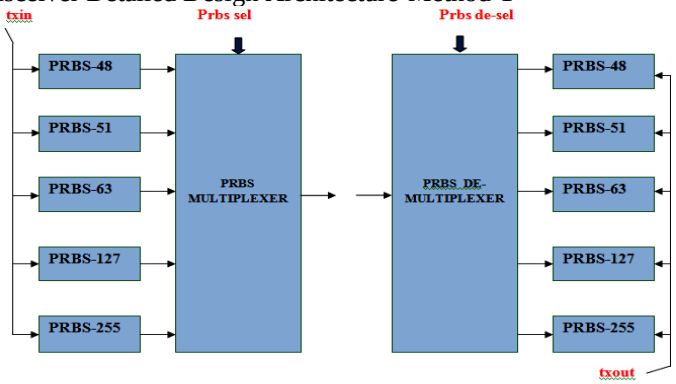

Figure 2. PRBS Transceiver Design-$2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 NRZ etc

Description The Aim and purpose of invention of new multichannel PRBS Transceiver is for transmit and receive data serially by using tx_in and tx_out, rxin, rxout signals and The Transceiver is processed the low frequency signal input with different high speed carrier wave frequencies in the form of different PRBS pseudo random binary sequence seed word bit/byte patterns -$2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 NRZ etc and also on receiver side processed with the above patterns. These PRBS provide different baud rate frequencies speed as per CCITT & ITU O.150,O.151,O.152, AT&T standards. The Modulation done on the Transmitter side and De-Modulation done on Receiver side w.r.t difference PRBS Seed word tapped elements. This Design is mainly intended for High Speed Multi pattern PRBS Transmitter and Receiver of Sequence $2e^{48}$-1,$2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 etc. for Ultra High Speed Wireless Communication Engineering Applications 3rd&4th Generation of wireless communication & network products & Technologies (CDMA, GPS, GSM, WIFI, WIMAX, GiFi, Optical

etc)as per CCITT- ITU Standards. The PRBS Design Implemented based on the linear feedback shift register (LFSR). The family of Shift Registers are used to generate pseudo random binary sequences for Multi Kbps, Mbps & Gbps Speed. These different pattern sequences are Designated as per CCITT ITU 0.151/O.152/O.153 & AT&T Standards. This Soft IP Core Designed by System Verilog HDL/ Verilog HDL. RTL Design simulation done by Synopsys VCS 2020 and Altera model-sim and Logic Design Flow & Synthesis done by Xilinx ISE and Altera Quartus EDA Tools.

[C] Proposed Ultra High Frequency PRBS Transceiver Design Architecture method-2

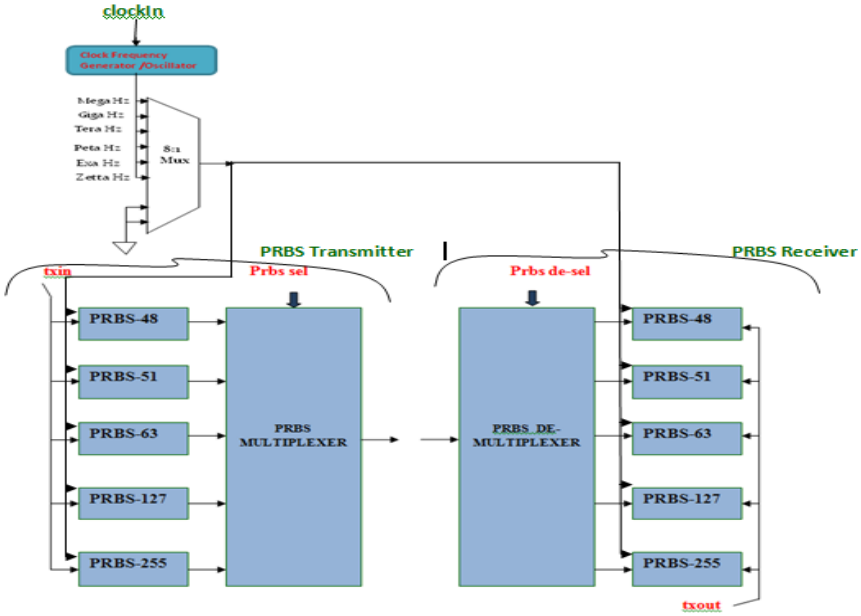

Figure 3. Ultra High frequency PRBS Transceiver Design-$2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 NRZ etc

Description The Aim and purpose of invention of new multichannel PRBS Transceiver is for transmit and receive data serially by using tx_in and tx_out, rxin, rxout signals and The Transceiver is processed the low frequency signal input with different high speed carrier wave frequencies in the form of different PRBS pseudo random binary sequence seed word bit/byte patterns -$2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 NRZ etc and also on receiver side processed with the above patterns. The PRBS Transceiver is purely synchronized with one of Ultra High clock frequencies Mega/Giga/Tera/Peta/Exa/Zetta HZ (MHz/GHz/THz/PHz/EHz/ZHz) clock frequency. The Clock frequency Selector select one of the above mention frequency and synchronize with PRBS Transmitter and PRBS Receiver for improvement of Speed, Bandwidth etc. The Transceiver mainly used for Long Distance Wireless communication Space/Satellite distance level. These PRBS provide different baud rate frequencies speed as per CCITT & ITU O.150,O.151,O.152, AT&T standards. The Modulation done on the Transmitter side and De-Modulation done on Receiver side w.r.t difference PRBS Seed word tapped elements. This Design is mainly intended for High Speed Multi pattern PRBS Transceiver of Sequence $2e^{48}$1,$2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 etc. for Ultra High Speed Wireless Communication Engineering Applications 3^{rd}&4^{th} Generation of wireless communication & network products & Technologies (CDMA, GPS, GSM, WIFI, WIMAX, GiFi, Optical etc)as per CCITT- ITU Standards. The PRBS Design Implemented based on the linear feedback shift register (LFSR). The family of Shift Registers are used to generate pseudo random binary sequences for Multi Gbps, Tbps, Pbps, Ebps, Zbps Speed. These different pattern sequences are Designated as per CCITT ITU 0.151/O.152/O.153 & AT&T Standards. This Soft IP Core Designed by System Verilog HDL/ Verilog HDL. RTL Design simulation done by Synopsys VCS 2020 and Altera model-sim and Logic Design Flow & Synthesis done by Xilinx ISE and Altera Quartus EDA Tools.

[D] Proposed Ultra High Frequency Multi channel PRBS Transceiver Architecture- method-3

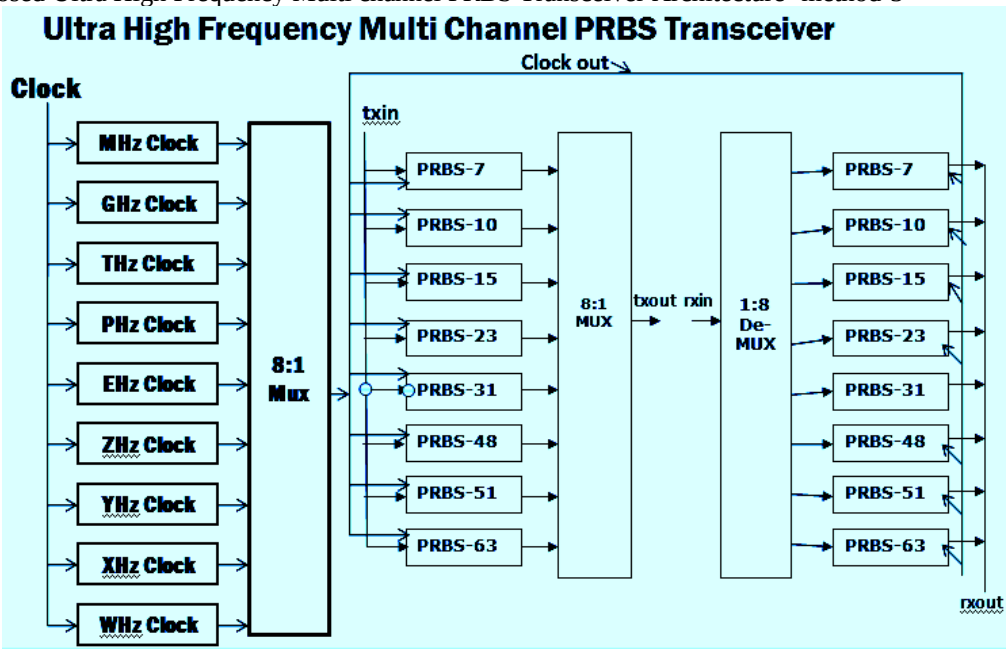

Figure 4. Ultra High frequency Multi Channel PRBS Transceiver Design-$2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 NRZ etc

Description: The Above figure shown Ultra High Frequency (Mhz, Ghz, Thz, Phz, Ehz, Yhz, Xhz, Whz clock) multichannel PRBS Transceiver consists Transmitter and receiver of different PRBS tapped Carrier frequency generator patterns ($2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1).The low frequency transmitter input is modulated with these different high frequency carrier PRBS tapped sequence patterns to generate transmitted output. At the receiver side the same transmitted output is demodulated /decoded to generate original low frequency base band signal receiver output.All these multi channel PRBS Transceiver is synchronized with ultra high clock frequencies(Mhz, Ghz, Thz, Phz, Yhz, Xhz, Whz). These clock frequencies are generated by using 20, 30, 40, 50, 60, 70, 80, 90,100 bit counters and these clock frequencies(Mhz, Ghz, Thz, Phz, Ehz, Zhz, Yhz, Xhz, Whz clock) are generated by synchronizing and toggling at every posedge of $2^{20}/2$, $2^{30}/2$, $2^{40}/2$, $2^{50}/2$,$2^{60}/2$, $2^{70}/2$, $2^{80}/2$, $2^{90}/2$, $2^{100}/2$ clock cycle period with respect to main reference clock. Due to ultra high frequency clock synchronization, The PRBS Transceiver suit for Very Advanced ASIC /SOC Communication engineering - Wireless & engineering communication SOC Applications and products. By using the SOC, could easily transmit and receive large packet transactions data with zero latency time and improve system performance and bandwidth of Any SOC Application/product.The purpose of PRBS Transceiver is designed for very high speed long distance communication suit for Applications /products (CDMA, GPS, Satellite/space products) in terms of multiple thousands/lacks of km's.Simulation and Synthesis done by leading EDA software Simulators (Synopsys VCS 2020.1)

Table 1. PRBS Research Performance Metrics

PRBS Type	Shift Register Length	Characteristic Polynomial	PRBS Length	Clock Frequency's	Bit rate / Spectrum Efficiency	Bandwidth
$2e^{48}$-1	48	$X^{46}+x^{47}+1$	2^{48}-1=281474976710656	1Tera, 1 Peta, 1 Exa, 1Zetta 1Yotta, 1 Xona 1 Weka ,1 VHz	1Tbps,Pbps,Ebps,Zbps,Ybps,Xbps,Wbps,Vbps	2 Tera, Peta,Exa,Zetta,etc
$2e^{51}$-1	51	$X^{48}+x^{51}+1$	2^{51}-1=2.25179981E+15	1Tera, 1 Peta,1 Exa, 1Zetta 1Yotta, 1 Xona 1 Weka, 1 VHz	1Tbps,Pbps,Ebps,Zbps,Ybps,Xbps,Wbps,Vbps	2 Tera, Peta,Exa,Zetta,etc
$2e^{63}$-1	63	$X^{58}+x^{63}+1$	2^{63}-1=9.22337204E+18	1Tera, 1 Peta,1 Exa, 1Zetta 1Yotta, 1 Xona 1 Weka,1 VHz	1Tbps,Pbps,Ebps,Zbps,Ybps,Xbps,Wbps,Vbps	2 Tera, Peta,Exa,Zetta,etc
$2e^{127}$-1	127	$X^{122}+x^{127}+1$	2^{127}-1=1.70141183E+38	1Tera, 1 Peta,1 Exa, 1Zetta 1Yotta, 1 Xona 1 Weka, 1 VHz	1Tbps,Pbps,Ebps,Zbps,Ybps,Xbps,Wbps,Vbps	2 Tera, Peta,Exa,Zetta,etc
$2e^{255}$-1	255	$X^{247}+x^{255}+1$	2^{255}-1=5.7896044E+76	1Tera, 1 Peta,1 Exa, 1Zetta 1Yotta, 1 Xona 1 Weka, 1 VHz	1Tbps,Pbps,Ebps,Zbps,Ybps,Xbps,Wbps,Vbps	2 Tera, Peta,Exa,Zetta,etc

III. HDL Design Procedure
[III] HDL Software Description
[A] PRBS Transceiver RTL DUT

```
        module prbs_data_transceiver#(parameter N6 = 48,N7=52, N8 = 64,N9 = 128, N10 = 256
)(clock,reset,prbs_sel,tx_in,rx_out,tx,rx);
//Declaration of data seriaize de serialize ios ,signals
input clock,reset;
input tx_in;
input [3:0]prbs_sel;
output reg rx_out;
output reg[N8-1:0] tx,rx;
bit zetta_clock;
bit [69:0] zetta_count =
70'b0000000000000000000000000000000000000000000000000000000000000000000000;
reg [N6-1:0]tx_prbs48,rx_prbs48;
reg [N7-1:0]tx_prbs52,rx_prbs52;
reg [N8-1:0]tx_prbs64,rx_prbs64;
reg [N9-1:0]tx_prbs127,rx_prbs127;
reg [N10-1:0]tx_prbs255, rx_prbs255;

reg tx_out;
//reg rx_out;
//PRBS based Data Serializer Deserialize function block
always@(posedge clock or reset)
begin
if(reset)
zetta_count = 70'b0000000000000000000000000000000000000000000000000000000000000000000000;
else
begin
zetta_count = zetta_count+5.90295810E+20;
end
zetta_clock = zetta_count[69];
end

always@(posedge zetta_clock or reset)
begin
tx_prbs48 = 48'h000000000000;
rx_prbs48 = 48'h000000000000;
tx_prbs52 = 52'h0000000000000;
rx_prbs52 = 52'h0000000000000;
tx_prbs64 = 64'h0000000000000000;
rx_prbs64 = 64'h0000000000000000;
tx_prbs127 = 128'h00000000000000000000000000000000;
rx_prbs127 = 128'h00000000000000000000000000000000;
tx_prbs255 = 255'h000000000000000000000000000000000000000000000000000000000000000000000000000;
rx_prbs255 = 255'h000000000000000000000000000000000000000000000000000000000000000000000000000;

end
else
begin
case(prbs_sel)
0:begin
tx_prbs48[N6-1:1] = tx_prbs48[N6-2:0];
tx_prbs48[N6-N6] = tx_prbs48[N6-6]^tx_prbs48[N6-1]^tx_in;
tx = tx_prbs48;
tx_out = tx_prbs48[N6-48];
rx_prbs48[N6-1:1] = rx_prbs48[N6-2:0];
rx_prbs48[N6-N6] = rx_prbs48[N6-6]^rx_prbs48[N6-1]^tx_out;
rx = rx_prbs48;
```

```
rx_out = rx_prbs48[N6-48];
//ser_out = rx_out;
$display($time,"prbs48 tapped seq transmitter input and receiver out tx_in = %b,rx_out = %b",tx_in,rx_out);
$display($time,"prbs48 tx and rx parallel out tx = %b, rx = %b",tx,rx);
end
1:begin
tx_prbs52[N7-1:1] = tx_prbs52[N7-2:0];
tx_prbs52[N7-N7] = tx_prbs52[N7-4]^tx_prbs52[N7-1]^tx_in;
tx = tx_prbs52;
tx_out = tx_prbs52[N7-N7];
rx_prbs52[N7-1:1] = rx_prbs52[N7-2:0];
rx_prbs52[N7-N7] = rx_prbs52[N7-4]^rx_prbs52[N7-1]^tx_out;
rx = rx_prbs52;
rx_out = rx_prbs52[N7-N7];
//ser_out = rx_out;
$display($time,"prbs52 tapped seq transmitter input and receiver out tx_in = %b,rx_out = %b",tx_in,rx_out);
$display($time,"prbs52 tx and rx parallel out tx = %b, rx = %b",tx,rx);
end
2:begin
tx_prbs64[N8-1:1] = tx_prbs64[N8-2:0];
tx_prbs64[N8-N8] = tx_prbs64[N8-6]^tx_prbs64[N8-1]^tx_in;
tx = tx_prbs64;
tx_out = tx_prbs64[N8-N8];
rx_prbs64[N8-1:1] = rx_prbs64[N8-2:0];
rx_prbs64[N8-N8] = rx_prbs64[N8-6]^rx_prbs64[N8-1]^tx_out;
rx = rx_prbs64;
rx_out = rx_prbs64[N8-N8];
//ser_out = rx_out;
$display($time,"prbs64 tapped seq transmitter input and receiver out tx_in = %b,rx_out = %b",tx_in,rx_out);
$display($time,"prbs64 tx and rx parallel out tx = %b, rx = %b",tx,rx);
end
3:begin
tx_prbs127[N9-1:1] = tx_prbs127[N9-2:0];
tx_prbs127[N9-N9] = tx_prbs127[N9-6]^tx_prbs127[N9-1]^tx_in;
tx = tx_prbs127;
tx_out = tx_prbs127[N9-N9];
rx_prbs127[N9-1:1] = rx_prbs127[N9-2:0];
rx_prbs127[N9-N9] = rx_prbs127[N9-6]^rx_prbs127[N9-1]^tx_out;
rx = rx_prbs127;
rx_out = rx_prbs127[N9-N9];
//ser_out = rx_out;
$display($time,"prbs127 tapped seq transmitter input and receiver out tx_in = %b,rx_out = %b",tx_in,rx_out);
$display($time,"prbs127 tx and rx parallel out tx = %b, rx = %b",tx,rx);
end
4:begin
tx_prbs255[N10-1:1] = tx_prbs255[N10-2:0];
tx_prbs255[N10-N10] = tx_prbs255[N10-8]^tx_prbs255[N10-1]^tx_in;
tx = tx_prbs255;
tx_out = tx_prbs255[N10-N10];
rx_prbs255[N10-1:1] = rx_prbs255[N10-2:0];
rx_prbs255[N10-N10] = rx_prbs255[N10-8]^rx_prbs255[N10-1]^tx_out;
rx = rx_prbs255;
rx_out = rx_prbs255[N10-N10];
//ser_out = rx_out;
$display($time,"prbs255 tapped seq transmitter input and receiver out tx_in = %b,rx_out = %b",tx_in,rx_out);
$display($time,"prbs255 tx and rx parallel out tx = %b, rx = %b",tx,rx);
end
default: begin
tx_prbs64[N8-1:1] = tx_prbs64[N8-2:0];
```

```
tx_prbs64[N8-N8] = tx_prbs64[N8-6]^tx_prbs64[N8-1]^tx_in;
tx = tx_prbs64;
tx_out = tx_prbs64[N8-N8];
rx_prbs64[N8-1:1] = rx_prbs64[N8-2:0];
rx_prbs64[N8-N8] = rx_prbs64[N8-6]^rx_prbs64[N8-1]^tx_out;
rx = rx_prbs64;
rx_out = rx_prbs64[N8-N8];
//ser_out = rx_out;
end
endcase
end
//$display("PRBS Data Serializer De_serialized output ser_in = %b, ser_out = %b", ser_in,ser_out);
end
endmodule
```

[B] PRBS Transceiver Test Bench

```
module prbs_data_ser_deser_tb;
//Declaration of PRBS Data Serailizer De serializer ios
reg clock,reset;
reg tx_in;
reg [3:0]prbs_sel;
wire tx,rx;
wire rx_out;

// Declaration PRBS Data Serialise Deserialise DUT instance
prbs_data_transceiver prbs_DUT(clock,reset,prbs_sel,tx_in,rx_out,tx,rx);
// prbs_data_transceiver prbs_DUT(.*);
//clock
initial
begin
clock = 1'b0;
repeat(140)
#5 clock = ~clock;
end

//reset
initial
begin
#5 reset = 1'b1;
#5 reset = 1'b0;
end
// Seletion of prbs
initial
begin
#5 prbs_sel = 0;
#50 prbs_sel= 1;
#50 prbs_sel= 2;
#50 prbs_sel= 3;
#50 prbs_sel= 4;
end
//serial input
initial
begin
#5 tx_in = 1'b1;
#10 tx_in = 1'b0;
#10 tx_in = 1'b1;
#10 tx_in = 1'b1;
---
#10 tx_in = 1'b1;
```

```
#10 tx_in = 1'b1;
end

initial
begin
$dumpvars(0,prbs_data_ser_deser_tb);
$dumpfile("dump.vcd");
end
endmodule
```

II. Result

[A] Display

CPU time: .302 seconds to compile + .371 seconds to elab + .416 seconds to link Chronologic VCS simulator copyright 1991-2021 Contains Synopsys proprietary information.

Compiler version S-2021.09; Runtime version S-2021.09; Dec 1 07:38 2023 10prbs48 tapped seq transmitter input and receiver out tx_in = 1,rx_out = 1 10prbs48 tx and rx parallel out tx = 0000000000000000000000000000000000000000000000000000000000000001, rx = 0000000000000000000000000000000000000000000000000000000000000001
15prbs48 tapped seq transmitter input and receiver out tx_in = 0,rx_out = 0 15prbs48 tx and rx parallel out tx = 0000000000000000000000000000000000000000000000000000000000000010, rx = 0000000000000000000000000000000000000000000000000000000000000010
35prbs48 tapped seq transmitter input and receiver out tx_in = 1,rx_out = 1 35prbs48 tx and rx parallel out tx = 0000000000000000000000000000000000000000000000000000000000000101, rx = 0000000000000000000000000000000000000000000000000000000000000101
55prbs52 tapped seq transmitter input and receiver out tx_in = 1,rx_out = 1 55prbs52 tx and rx parallel out tx = 0000000000000000000000000000000000000000000000000000000000000001, rx = 0000000000000000000000000000000000000000000000000000000000000001
75prbs52 tapped seq transmitter input and receiver out tx_in = 1,rx_out = 1 75prbs52 tx and rx parallel out tx = 0000000000000000000000000000000000000000000000000000000000000011, rx = 0000000000000000000000000000000000000000000000000000000000000011
95prbs52 tapped seq transmitter input and receiver out tx_in = 0,rx_out = 0 95prbs52 tx and rx parallel out tx = 0000000000000000000000000000000000000000000000000000000000000110, rx = 0000000000000000000000000000000000000000000000000000000000000110

515prbs255 tx and rx parallel out tx = 0000000000000000000000000000000000000000000000001101110111011101, rx = 0000000000000000000000000000000000000000000000001101110111011101
535prbs255 tapped seq transmitter input and receiver out tx_in = 1,rx_out = 1 535prbs255 tx and rx parallel out tx= 0000000000000000000000000000000000000000000000011011101110111011, rx = 0000000000000000000000000000000000000000000000011011101110111011
555prbs255 tapped seq transmitter input and receiver out tx_in = 1,rx_out = 1 555prbs255 tx and rx parallel out tx= 0000000000000000000000000000000000000000000000110111011101110111, rx = 0000000000000000000000000000000000000000000000110111011101110111
575prbs255 tapped seq transmitter input and receiver out tx_in = 0,rx_out = 0 575prbs255 tx and rx parallel out tx = 0000000000000000000000000000000000000000000001101110111011101110, rx = 0000000000000000000000000000000000000000000001101110111011101110
595prbs255 tapped seq transmitter input and receiver out tx_in = 1,rx_out = 1 595prbs255 tx and rx parallel out tx = 0000000000000000000000000000000000000000000011011101110111011101, rx = 0000000000000000000000000000000000000000000011011101110111011101
V C S S i m u l a t i o n R e p o r t
Time: 700 ns
CPU Time: 0.600 seconds; Data structure size: 0.0Mb
Fri Dec 1 07:38:03 2023

[B] Simulation Waveform

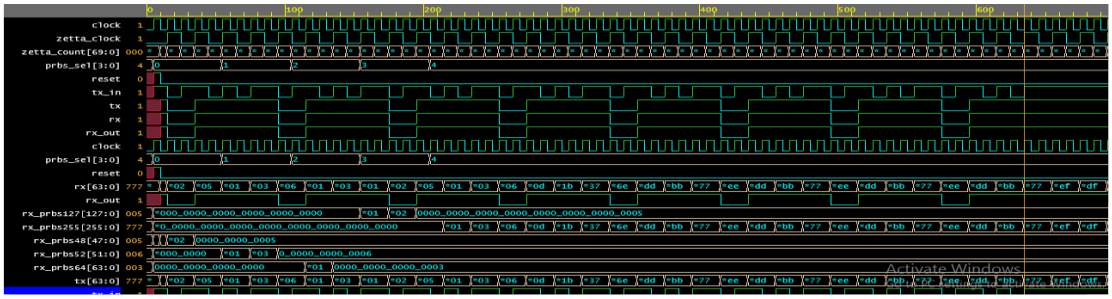

Figure 5. PRBS Transceiver Simulation

[C] PRBS TxRx-FPGA Logic Synthesis Placed Layout

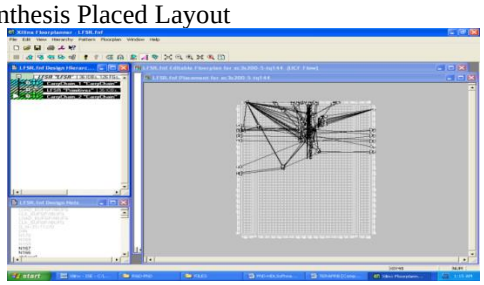

Figure 6. PRBS Transceiver FPGA Layout

[D] PRBS TxRx-FPGA Logic Synthesis Routed Layout

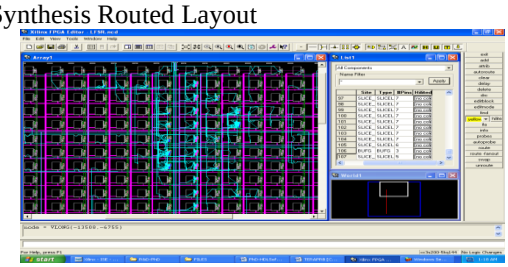

Figure 7. PRBS Transceiver FPGA Routed Layout

III. Conclusion

The RTL Design and Verification of PRBS Transceiver designed using long Periodicity PRBS Pattern Seed words-are $2e^{48}$-1, $2e^{51}$-1, $2e^{63}$-1, $2e^{127}$-1, $2e^{255}$-1 for ultra high long distance space/satellite distance applications/products. The Aim of design for generate effective high frequency modulation and demodulation for long distance wireless communication applications as well improve ment of system Bandwidth.

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