

## Design Arithmetic Circuits Using Quaternary Logic

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**Abstract:** Arithmetic circuits play a really important role in each all-purpose and application specific procedure circuits. Multiple Valued Logic (MVL) provides the key good thing about the next density per computer circuit space compared to ancient 2 valued binary logic. Quaternary (Four-valued) logic conjointly offers the good thing about simple interfacing to binary logic as a result of base four (=2<sup>2</sup>) permits for the utilization of straight forward encoding/decoding circuits. The purposeful completeness is well-trieed with a collection of basic quaternary cells. The library of cells supported the Supplementary Symmetrical Logic Circuit Structure (SUSLOC) square measure designed, simulated, and accustomed build many quaternary fixed-point arithmetic circuits like adders, multipliers. These SUSLOC circuit cells square measure valid mistreatment SPICE models and also the arithmetic architectures square measure valid mistreatment System Verilog models for purposeful correctness. Quaternary (radix-4) twin quantity secret writing principles square measure applied to optimize power and performance of adder circuits mistreatment common place cmos gate technologies.

**Index Terms:** Multiple-valued logic, Quaternarylogic, Modulo-n addition, subtraction and multiplication, Galois.addition and multiplication.

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### I. Introduction

The outstanding increase within the density of terribly massive Scale Integrated (VLSI) circuits is that the results of advanced Integrated Circuits (IC) fabrication processes and therefore the development of machine-controlled style tools. because the range of devices accommodated on VLSI chips will increase, several issues additionally arise. for example, the interconnection between devices within and out of doors a chip becomes considerably sophisticated and therefore the space occupied by interconnections will increase hastily. Aggressive interconnect scaling following Moore's law introduces several challenges in integration, performance and responsibility. Inappropriate routing ends up in a bigger chip size and cause temporal order and cross-talk issues. In deep submicron styles these issues square measure of outstanding importance.

The partial solutions to the present downside in today's VLSI circuits square measure to use many metal layers, flip-chips and different ways. though improvement in metal stack material have enabled business to scale back interconnect resistance in slim lines and at a similar time changes in layer nonconductor (ILD) material have down the road to line capacitance leading to Resistor-Capacitor (RC) delay improvement and so interconnect power consumption, however, deep submicron technology introduces formidable integration and responsibility challenges like higher slim Cu line resistance, higher current density and inferior thermo-mechanical properties that should be overcome. it's acknowledge that the binary system of numeration is that the leading alternative for standard voltage-mode style of digital systems. However, in a very typical binary system of numeration based mostly VLSI circuit regarding seventy p.c of chip space is occupied by interconnections that occupy an oversized portion of physical space even once it's not in use. thus the interconnections are going to be additional economical if many levels of logic square measure injected into one wire, as in multiple valued logics. Dissimilar to binary logic, multiple valued logics need quite 2 distinct levels of logic signals and permit quite 2 logical ideas to exist in a very logic system. Thus, the direct good thing about such logics is that the improved overall data potency. it's as a result of every r-valued signal will carry times additional data than a binary signal will. As a result the routing space is reduced on a exponent scale- -as r will increase. This reduction in range of interconnections and space of a chip is known by concerning Figure one.1. As is seen, the routing space of a 4-valued logic style is 2 times smaller than the corresponding binary logic system. two log r log r<sup>2</sup> the selection of the foremost favorable logic number in term of implementation price has been additionally studied by some researchers. the circuit implementation price is decreasing with increasing logic number and in step with C.M. Allen and D. Gioven, the optimum number is bigger than Euler constant, . Since in apply the number r is Associate in Nursinging whole number, it comprehends that the additional advantageous number should be a minimum of three or in different words ternary logic. On the opposite hand conversion with binary is best if special radices square measure chosen in such how that no data is lost or left unused  $e \approx 2.7$ .

### II. Objective

- 1) Use of deep metric linear unit technology for quaternary arithmetic circuit style.
- 2) Low power and space economical style needs to be done.
- 3) Static power and dynamic power is main objective of style.

- 4) Quaternary arithmetic circuit style are through with modulo logic and Galois field logic. variety of gates needed for Galois field are less as compared to modulo.
- 5) Use of single pin to get a quaternary logic levels.
- 6) 3 DLC with mux are needed for quaternary to binary conversion and one DLC is needed for binary to quaternary conversion.
- 7) Different manufactory file needs to be designed for various DLC.

### III. Literature Survey

Vasundara Patel & Gurumurthy projected a low-power, high-speed, minimum space. They designed quaternary full adder mistreatment binary logic gates and number convertor. Simulation done by mistreatment HSPICE and COSMOS tools. They used 180nm technology.[1]

In M. Thoidis paper[11], the projected circuits were static and operate in voltage mode. The reported no static power dissipation because the circuits were static in nature[11].

Economic expert designed a netruly full adder quaternary circuit mistreatment three power offer lines and multi-Vt transistors. Ricardo has designed quaternary electronic device (MUX) 4:1 with 4quaternary inputs and one quaternary output and used this MUX as a building block to construct full adder projected technique advantages giant scale circuits since the abundant power dissipation with enhanced speed will cause the event of extraordinarily low energy circuits whereas sustaining the high Performance needed for several applications[7].

The implementation of Quaternary Signed Digit addition was bestowed in paper[5] . The take a look at confirms the superior performance of the QSD adder implementation over alternative adders. owing to the carry – free addition theme. The complexness of the QSD adder was linearly proportional to the quantity of digits, that ar of a similar order because the simplest adder, the ripple carry adder. This QSD adder is used as a building block for alternative arithmetic operations such Multiplication, division, root, etc. With the QSD addition theme, some well-known arithmetic algorithms is directly enforced[5] .

### IV. Implimentation

#### Implementation of binary to quaternary conversion:-

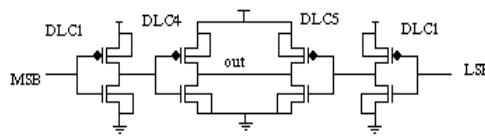


Fig: circuit diagram of binary to quaternary conversion

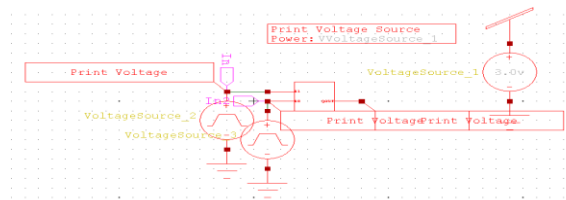


Fig1: schematic of binary to quaternary conversion

A basic binary to quaternary circuit consists of 2 PMOS and 2 NMOS transistors that type 2 inverters and 2 DLC one circuits. LSB and MSB of 2 bit binary varieties are given to 2 DLC1 circuits and output of two inverters can give quaternary number.

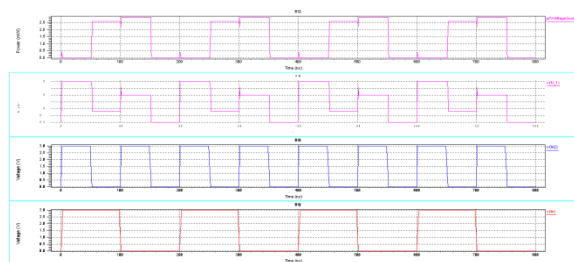


Fig2: waveform of binary to quaternary conversion

**Implementation of quaternary to binary conversion:-**

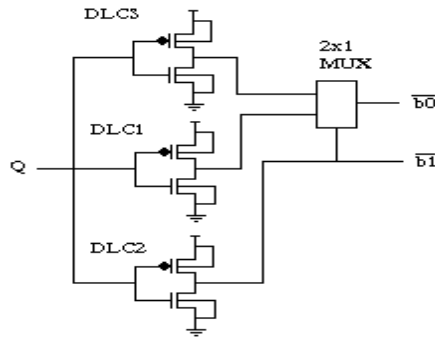


Fig: circuit diagram of quaternary to binary conversion

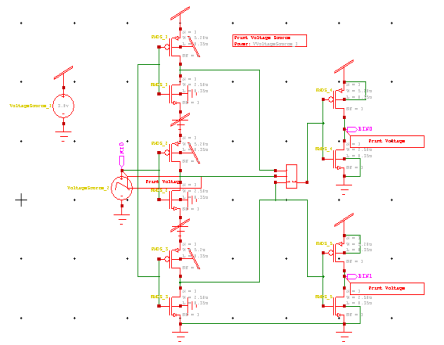


Fig3: schematic quaternary to binary conversion

A basic Quaternary to binary converter uses three down literal circuits DLC1, DLC2, DLC3 and 2:1 multiplexer. Q is the quaternary input varying as 0, 1, 2 and 3 which is given to three DLC circuits. The binary out puts thus obtained will be in complemented form and are required to pass through inverters to get actual binary numbers.

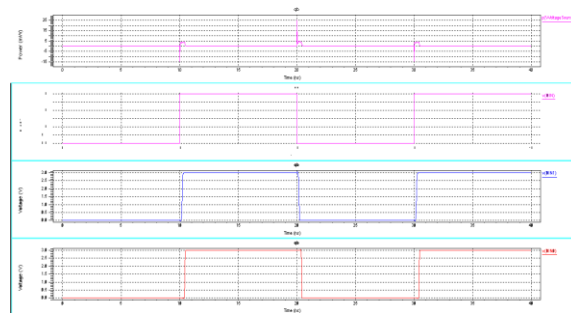


Fig4: waveform quaternary to binary conversion

**Implementation of modulo-4 adder:-**

		$X_1X_2$			
		0	1	2	3
$Y_1Y_2$	0	0	1	2	3
	1	1	2	3	0
	2	2	3	0	1
	3	3	0	1	2

Modulo-4 addition

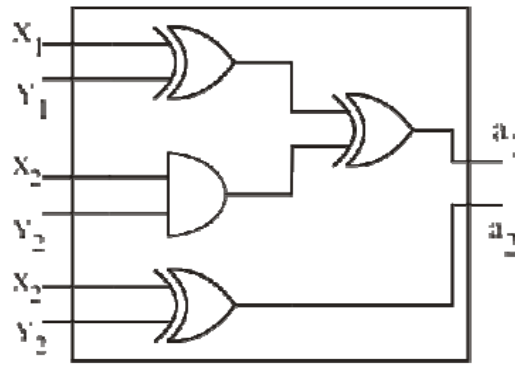


Fig: circuit diagram of modulo-4 adder

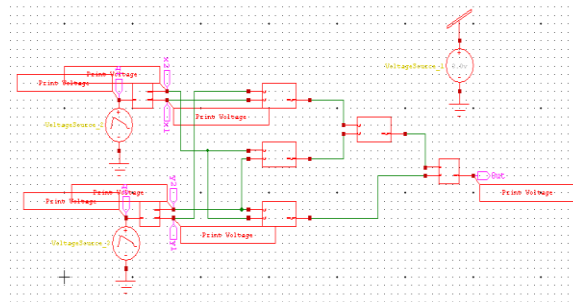


Fig5: schematic of modulo-4 adder

Modulo-4 addition circuit is shown in figure5. During this Circuit, to induce input and output in quaternary kind, quaternary to binary circuit is connected to the input of the modulo-4 addition circuit and binary to quaternary circuit is connected to the output of the modulo-4 addition circuit. Here during this figure giving input in quaternary kind and obtaining output in quaternary kind. This output satisfies the modulo-4 addition table as shown in table . stripped-down functions are obtained from the Karnaugh diagrams for the addition table shown in table and so simplified the maximum amount as attainable victimization all attainable gate varieties. Stripped-down functions obtained from the stripped-down polynomials extracted from the Karnaugh diagrams square measure shown below. Let  $x_1$   $x_2$  and  $y_1$   $y_2$  be the binary illustration of quaternary numbers that should be more. For addition:

$$a_1 = (x_1 \oplus y_1) \oplus (x_2 \cdot y_2) \quad (3) \quad a_2 = (x_2 \oplus y_2)$$

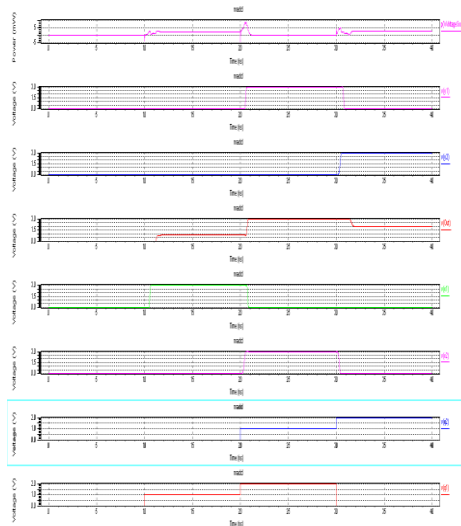


Fig6: waveform of modulo-4 adder

Implementation of Galois field adder:-

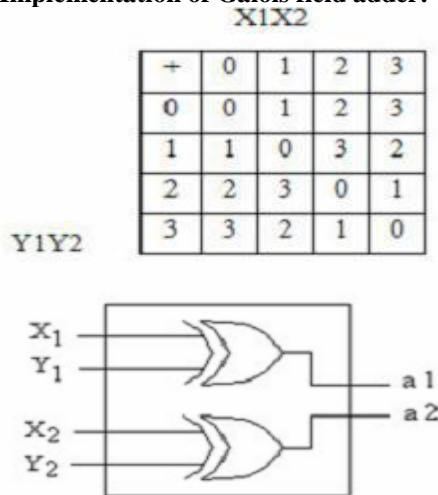


Fig: circuit diagram of Galois field adder

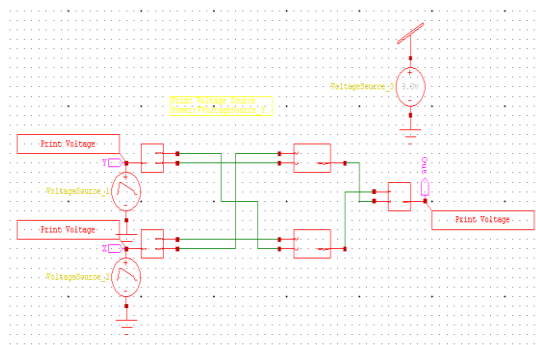


Fig7: schematic of Galois field adder

Galois addition table in Figure is employed in Karnaugh diagrams to get minimum operate. Minimal functions obtained from the minimal polynomials extracted from the Karnaugh diagrams for GF (4) addition is shown below. Let  $x_1 x_2$  and  $y_1 y_2$  be the binary illustration of 2 quaternary numbers that have to be compelled to be accessorial.  $a_1$  and  $a_2$  are the 2 bit results of addition between  $x_1 x_2$  and  $y_1 y_2$ .

$$a_1 = (x_1 \oplus y_1)$$

$$a_2 = (x_2 \oplus y_2)$$

Above equation shows that addition in GF (4) needs solely 2 gates and depth of web is reduced to at least one. this is often a really sensible style among four circuits. Logical implementation of the circuit is shown in figure .

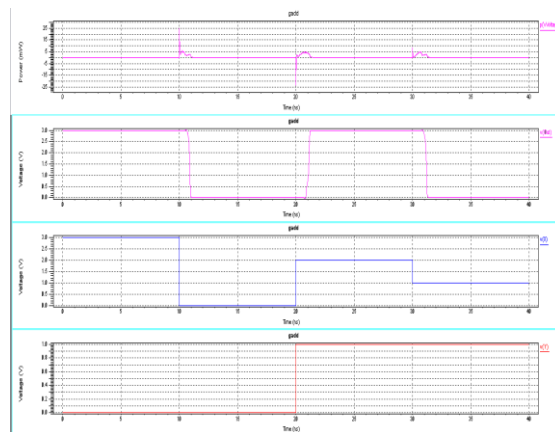


Fig8: waveform of Galois field adder

## V. Result

TSPICE transient analysis simulation is done to verify the functionality of the circuits. 50nm technology files are used for simulations. Simulation result of quaternary to binary and binary to quaternary are shown in figure and figure respectively. Simulation results of Modulo-4 addition , Galois Field addition are shown above. There result of polynomials shown in equations obtained by K map reduction. These circuits consume less number of transistors and shows high performances.

## VI. Conclusion

Binary to quaternary and quaternary to binary converters are designed using down literal circuits. Implementation of the circuit shows higher performance than circuits using two variable representations. Circuits for Modulo-4 addition, and require only 4 gates. Galois addition requires two xor gates which is most optimized one among other circuits while implementing in VLSI.

With the help of quaternary logic levels, we have reduced the interconnections. We have also used less number of gates and hence less area for Galois and modulo-4 arithmetic operations. Proposed circuits are suitable for implementing in VLSI with less number of interconnections and less area.

NAME	VOLTAGE	NO.OF MOSFET	POWER	CURRENT
MODULO ADDER	3V	94	9mW	281.33nA
GALOIS ADDER	3V	76	25mW	89.47nA
BINARY TO QUATERNARY	3V	8	420.90 nW	140.3032nA
QUATERNARY TO BINARY	3V	22	210.89nW	70.2991nA

## VII. Future Work

Modulo multiplier & subtractor and galois multiplier & subtractor will simulated using quaternary logic and also different application can be implimented .

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