Design and Simulation of RADAR Transmitter and Receiver using Direct Sequence Spread Spectrum

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Abstract : *DSSS (Direct Sequence Spread Spectrum) is one of the main technique of spread spectrum system and is the most common version use for military communication. In this paper, I have designed and implemented RADAR (Radio Wave Detection and Ranging) transmitter and receiver using direct sequence spread spectrum for range estimation. Most challenging part in RADAR system is to be getting better accuracy and resolution. In this paper, we mainly concentrates on direct sequence spread spectrum because it has some inherent merits like accuracy of ranging, sensitivity of power estimation, interference suppression than other types of spread spectrum. MATLAB simulink tool is used for designing and simulating of RADAR transreceiver using DSSS to obtain parameter and to test the influence of the signals on the system.*
Keywords: *BPSK, DSSS, PN Sequence, RADAR Transmitter and Receiver*

I. Introduction

DSSS system is widely used in wireless and military applications because it is very effective at suppressing interference. The interference can create from many reasons. One reason could be an adversary deliberately jamming the communication channel and other reason is the result of multiple access techniques. In multiple access technique many users simultaneously share the same transmission bandwidth thereby interfering with each other. Spread spectrum techniques can be used to hide a signal by transmitting it at low power [1]. Radar systems are largely used nowadays in verity of applications like air traffic control, astronomy, air defense systems, ocean surveillance, ground penetrating radars for geological observations, flight control systems, and automotive radar for Intelligent Transport Systems (ITS) etc. [2]. Spread spectrum systems have some good properties which make them an excellent candidate for radar applications. Some primary motivations for implementing spread spectrum in radar are accuracy of ranging, sensitivity, and target-separation, accuracy of power estimation and interference separation [3].

In this paper, the focus is on analyzing a radar system based on direct sequence spread spectrum modulation technique. The goal is to detect target at a very short distance with high resolution and calculate range of target with high accuracy. The system is developed in MATLAB simulink. Simulink is a software package for modeling, simulating, and analyzing dynamic systems at any point.

Section 2 gives design of radar transmitter and receiver using DSSS for range calculation. Section 3 gives simulation of each part of the radar transmitter and receiver systems. Section 4 gives results of the systems. Finally, the conclusion is mentioned in section 5.

II. Design of Radar Transmitter and Receiver

Fig.1 is block diagram of transmitter and receiver of RADAR system using DSSS. Transmitter part consists of binary message signal (Bernoulli Signal), spreading the message signal using PN sequence and its BPSK modulation. The output of BPSK modulation signal is proceeding to RF transmitter system. RF transmitter consists of RF mixer, power amplifier for up conversion of signal and transmits through the antenna [4].

At the side of receiver, received signal is reflected from the target model and received through the receiver antenna. First, received signal is down converted to the IF level in RF receiver part. RF receiver signal passed to the synchronization consists of acquisition, tracking and search and lock control block and voltage control oscillator (VCO). Then, RF signal is despread with the local PN sequence which to be generated from synchronization system. The output of demodulator represents the received signal. Using receiver and input message signals, calculates the delay between the transmitter and receiver and also calculates the bit error rate [5].
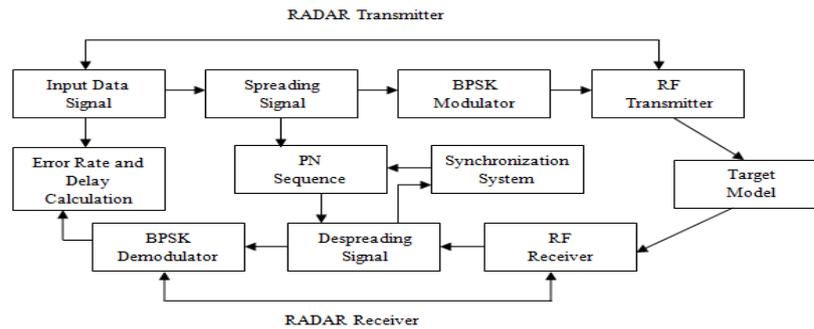
Fig.1. Block Diagram of RADAR Transmitter and Receiver

III. Dsss System Simulation using Matlab Simulink

The DS/SS is designed by using MATLAB simulink version because it is an attractive simulation tool provides the designer many facilities to rapidly design implement and test the desired system. Also, gives the designer a clear imagination to the system parameters, which is required to complete the design. The waveforms and spectra at any point of design can be obtained by using scope or frequency spectrum, this is very necessary to check design. Communication tool box, DSP tool box and SimRF tool box used for the simulation [6] [7] [8].

3.1 RADAR TRANSMITTER
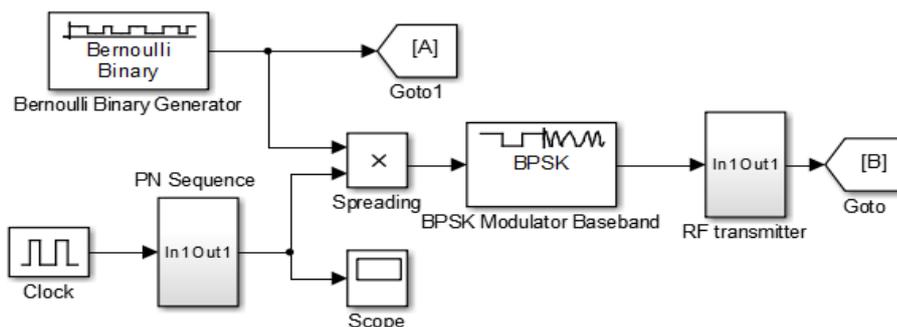
Fig.2. Simulation Diagram of RADAR Transmitter

Fig. 2 above shows the simulation diagram of radar transmitter which contains binary data generator, PN sequence generator, mixer (multiplier), BPSK modulator and RF transmitter block. In the following subsections, brief information about each subsystem will be explained.

3.1.1 GENERATING BINARY DATA STREAM

Binary message signal of 250bps generated by using binary data generator (Bernoulli Binary) from communication tool box with a probability of zero 50% and 50% ones.

3.1.2 PN Code Generator

Fig. 3 shows the block diagram of implementing a PN sequence generator. PN sequence is generated as maximal linear code with a polynomial $f(x) = 1+x+x^3$, the sequence is generated by using four stages D flip flops with a two feedback taped (x^3, x), Ex-OR to the input of the first stage D flip flop, in order to get 15 bits sequence and clock is gotten from digital clock is 4Kbps [9].
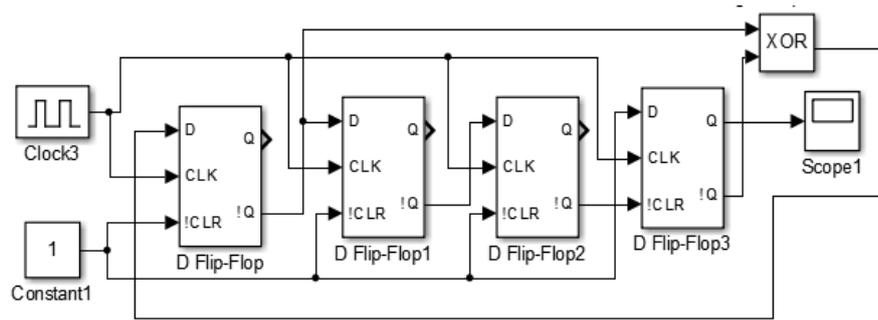
Fig.3. Block diagram of PN Sequence Generator

3.1.3 BPSK Modulator
The spread signal is modulated by using BPSK modulator baseband block in the communication tool box. Adjust phase offset and samples per symbol parameter in this block [10].
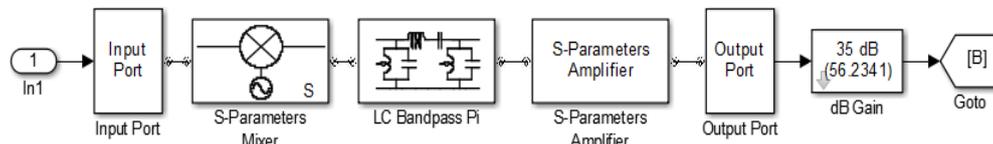
3.1.4 RF Transmitter

Fig.4. RF Transmitter Subsystem

Fig. 4 shows the RF transmitter of system which consist of mixer, band pass-pi filter and s parameter amplifier from SimRF tool box. Mixer convert the BPSK baseband modulated signal to IF frequency. Then, RF signal is band limited using band pass-pi filter. The band limited signal is then amplified by using s-amplifier. The output of RF transmitter is then transmitted using antenna [11].

3.2 Target Model
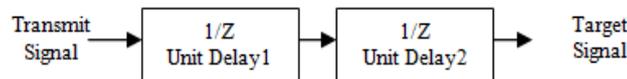
Fig.5. Target System using Delay Function

Fig. 5 shows the target model design using delay blocks. Target model depending on the target range, the transmitted signal is delayed and the signal power is attenuated. Then, signal is reflected towards the receiver. In the target, changed in target cross section, range and accordingly the reflected power towards the receiver.

3.3 Radar Receiver
Fig. 6 shows the simulation diagram of radar receiver, it consists of RF receiver system, active correlator, synchronization and baseband BPSK demodulator.
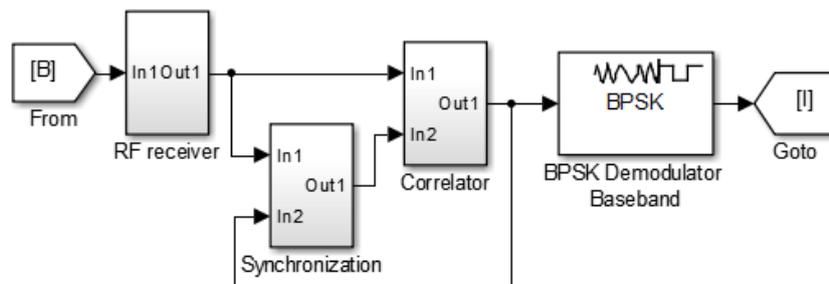

Fig.6. Simulation Diagram of RADAR Receiver
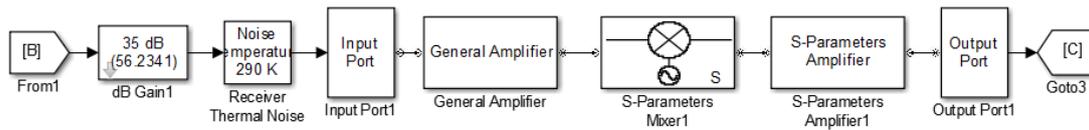
3.3.1   RF Receiver System

Fig.7. RF Receiver System

Fig.7 shows the RF receiver system. First, received signal from the antenna is amplified by general amplifier and proceed to the mixer for conversation of RF signal to IF signal and once again amplifier by s-parameter amplifier [12].
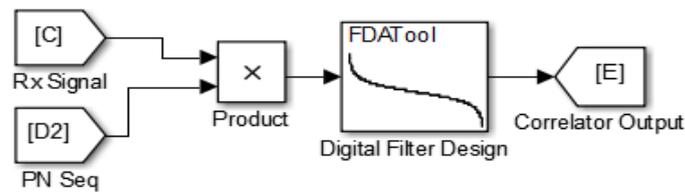
3.3.2   Correlator

Fig.8. Simulation Diagram of Correlator

Fig. 8 is correlator which contains mixer (multiplier) and digital filter from DSP tool box. In correlator received signal is despreaded only when received PN code and locally PN generated have the same phase and the cutoff frequency of digital LPF same as the data rate.

3.3.3   Synchronization Unit

It consists of acquisition, tracking, search/lock control unit and voltage controlled oscillator (VCO). Operation starts from acquisition, first output of correlator is compared to a preset threshold level in acquisition subsystem. If the threshold exceeds than there will be no delay in PN code and initial synchronization will be covered otherwise local PN code clock is delayed by half chip and acquisition process is repeated, after completion of acquisition, the SLCU enables the tracking loop [13]. The content of the synchronization unit are as follows.
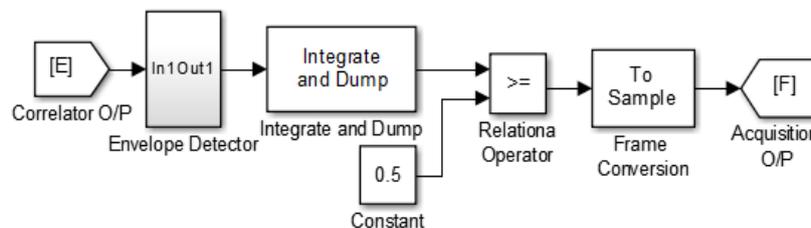
3.3.3.1   Acquisition Subsystem

Fig.9. Acquisition Subsystem

Fig. 9 shows the simulation diagram of acquisition subsystem. It uses a serial search of an acquisition method (dwell single time scheme). It contains square law (envelop detector) and integrator and dump to detect the correlated signal energy at constant test intervals (dwell time). The output of integrator and dump is compared with a preset threshold voltage. If the threshold is exceeded, then the phase of local PN code is corrected and tracking is initiated, otherwise a phase update signal is generated by SLCU for the next phase test operation.
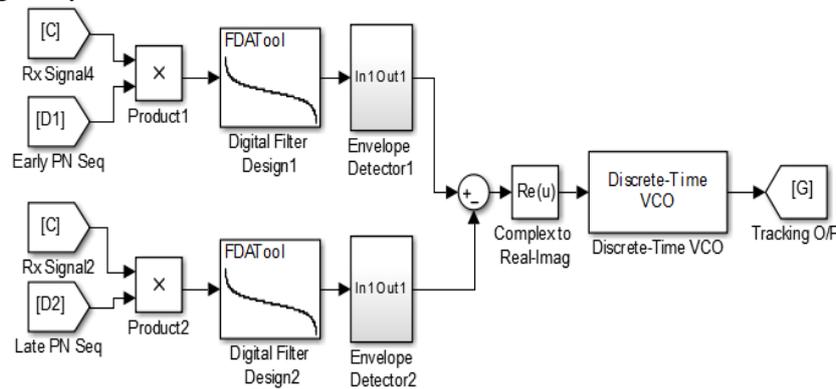
3.3.3.2   Tracking Subsystem

Fig.10. Tracking Subsystem

Fig.10 shows the simulation diagram of tracking subsystem. It uses a delay locked loop (DLL) method. The tracking subsystem consists of two branches; the common input to the branches is the received (DSSS) signal Rx, the second input to the upper branch is the output of the local PN code generator (Early), while the second input to the lower branch is the output of the local PN code generator (Late). Each branch consists of mixer (multiplier), digital LPF and square law (envelop detector). The cutoff frequency of low pass filter is the same as data rate, and the overall responses of this filter. The detected energy from both branches is subtracted to generate an error signal to excite the voltage control oscillator (VCO) to correct the local clock frequency (4MHz).
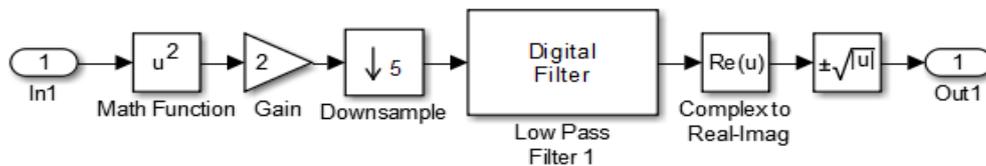
3.3.3.3   Envelope Detector

Fig.11. Envelope Detector

Fig.11 shows the envelope detector by squaring the signal and low pass filtering. The signal's envelope is equivalent to its outline and an envelope detector connects all the peaks in this signal. Envelope detection has numerous applications in the fields of signal processing and communications, one of which is amplitude modulation (AM) detection. This envelope detection method is easy to implement and can be done with a low-order filter, which minimizes the lag of the output.

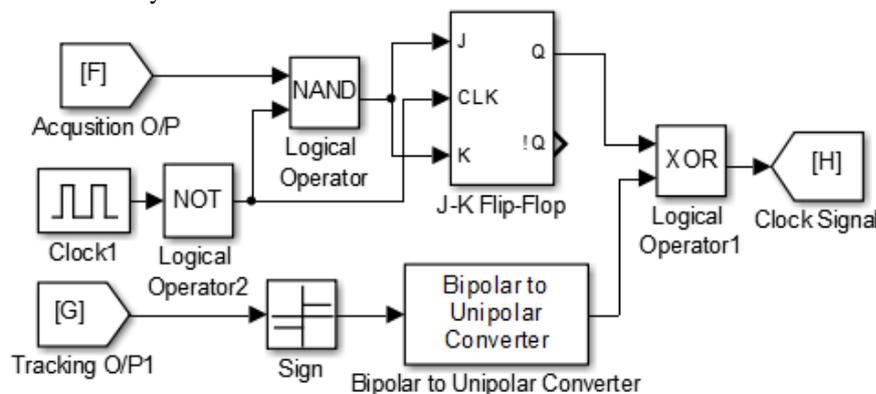### 3.3.3.4   Search / Lock Control System

Fig.12. Search/Lock Control Subsystem

Fig.12 shows the simulation diagram of search /Lock control unit subsystem. The pulse generator, generates a pulse width equal half chip period, after inversion this pulse is NANDed with output of acquisition subsystem to check the acquisition status. The VCO output is polar, it must be converting to unipolar format to

satisfy the requirement of XOR gate which produce the final local PN clock. However, local PN code is faster than the received PN code.

3.3.4 BPSK Demodulator
The baseband BPSK demodulator is taken from communication tool box, the despreading signal is demodulated.

IV. System Results
From the overall DS/SS system design during the simulation process after (100ms) simulation time, the performance of the system design can be tested as follows:-

4.1 At the Transmitter End
The following figure shows simulation results for RADAR transmission system. The results are displayed in the form of snapshots of scope signals. From these figures we can know easily what happened exactly inside a RADAR transmitter.
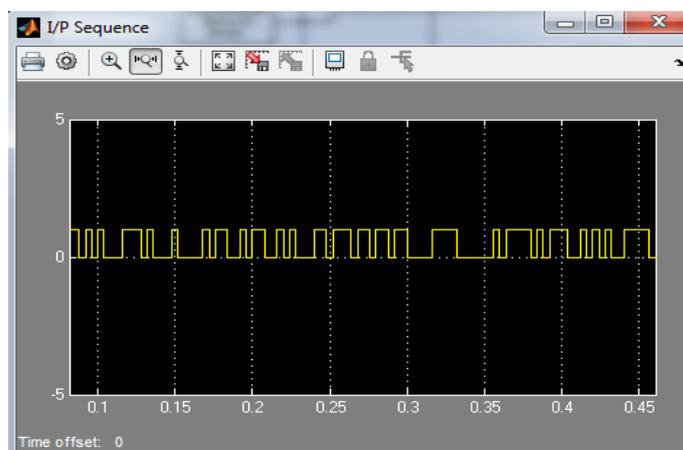

Fig.13. Binary Input Data

Fig.13 show that binary input data generated from a Bernoulli generator. Data rate of binary input message signal is 250bps.
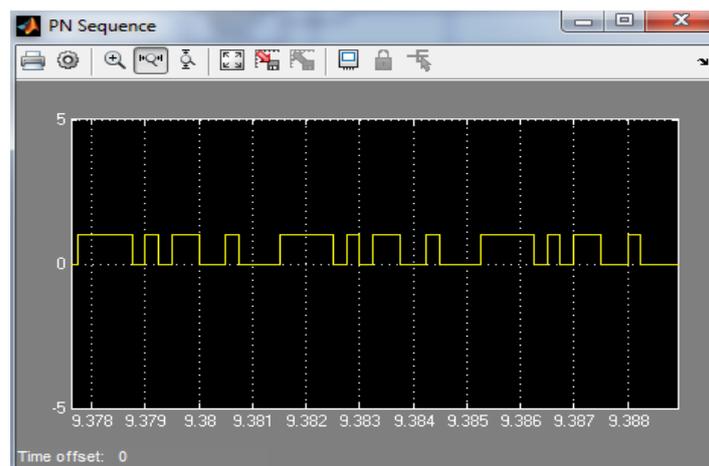

Fig.14. PN Sequence

Fig.14 is pseudo noise code generated from PN sequence generator block. The data rate of PN sequence is 4Kbps.
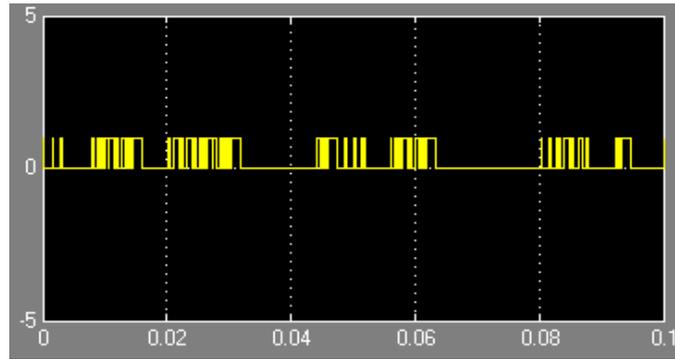
Fig.15. Spreading Signal

Fig.15 is spreading signal waveform generated from multiplication of PN sequence with input message signal.
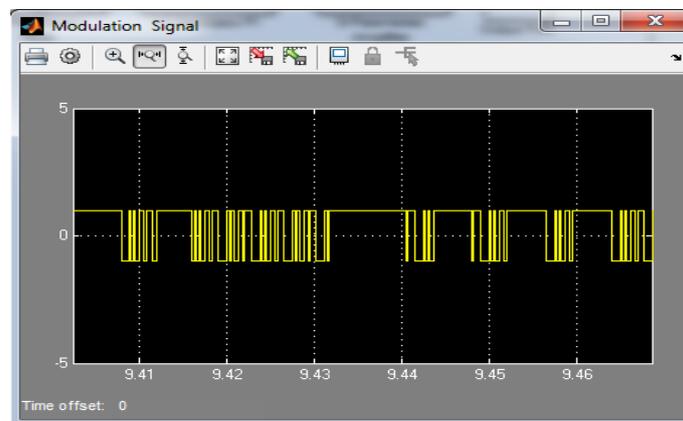

Fig.16. Modulation Signal

Fig.16 is modulation signal generated from the BPSK modulation block. A modulation data type is double.

Fig.17. RF Transmitter Signal

Fig.17 shows that the RF transmitter signal generated from the RF mixer and amplifier. This signal is transmit thorough the antenna in space.

4.2   At the Receiver End
        The following figure shows simulation results for RADAR receiver system. At receiver end we also calculate the delay for range estimation and error rate calculation.
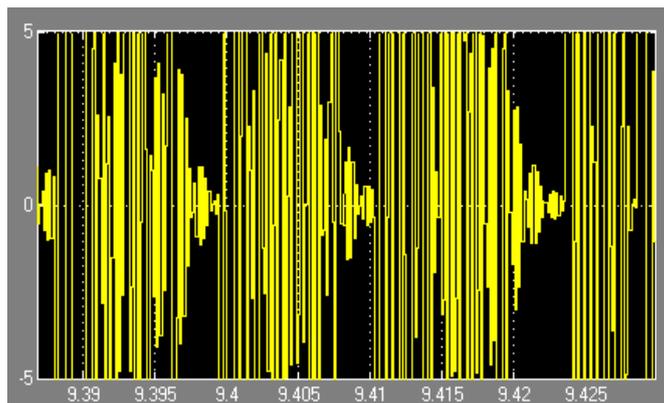
Fig.18. Correlator Signal

Fig.18 is the correlator signal generated from the multiplication of local PN sequence and received signal. Cut off frequency of digital low pass filter is same as the data rate.
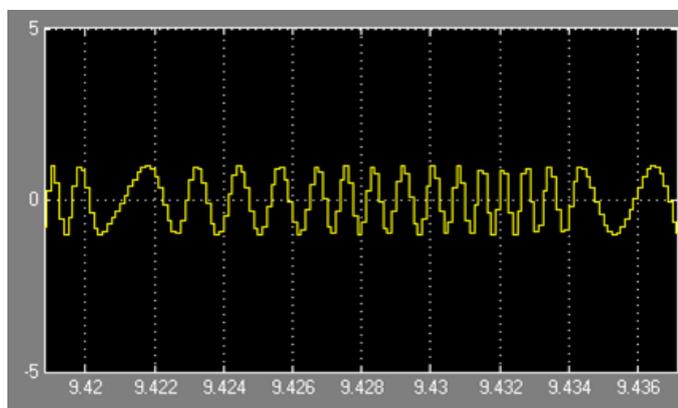

Fig.19. Tracking Signal

Fig.19 shows the Tracking output signal. It is error signal (subtracted energy) generated from the two branches.
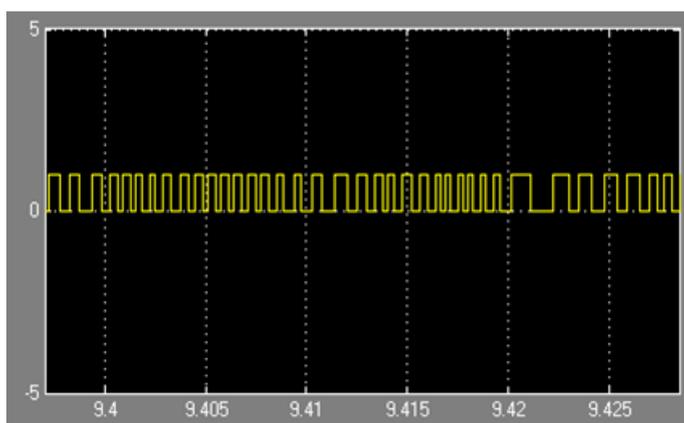

Fig.20. Clock Signal

Fig.20 shows that local clock signal generated from the search and lock control circuit. It is nothing but the xor operation between the tracking signal and acquisition signal.
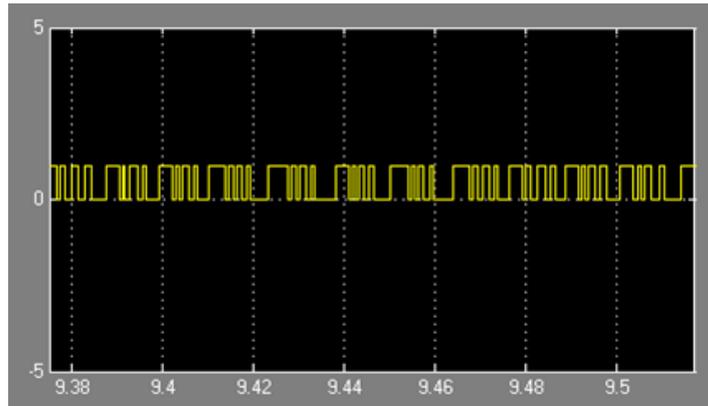
Fig.21. Early PN Sequence

Fig.21 shows that the early local PN sequence signal generated from the local clock frequency of 4 KHz.
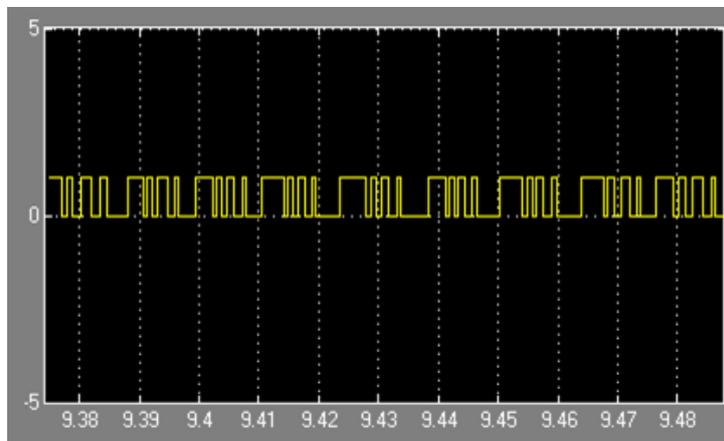

Fig.22. Late PN Sequence

Fig.22 shows that the let local PN sequence of 4 KHz frequency generated from the four stages D flip flops circuitry.
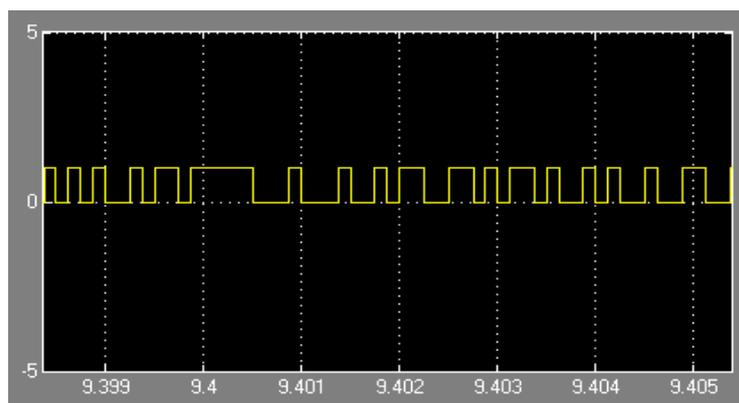

Fig.23. Demodulation Signal

Fig.23 shows the demodulation received output signal generated after the BPSK demodulation in RADAR receiver system.

4.2.1   Delay Calculation
        Compared the received data from BPSK demodulator with respect to the transmitted data for the delay calculation using align signal block (from communication system tool box) [14]. Delay factor is important for

range calculation. It is observed that if target introduces a delay of five clock cycles, there is a delay of 0.2ms between transmitted and received DSSS signal. The delay can be multiplied to the velocity of light to obtain the distance of target from the radar [15].
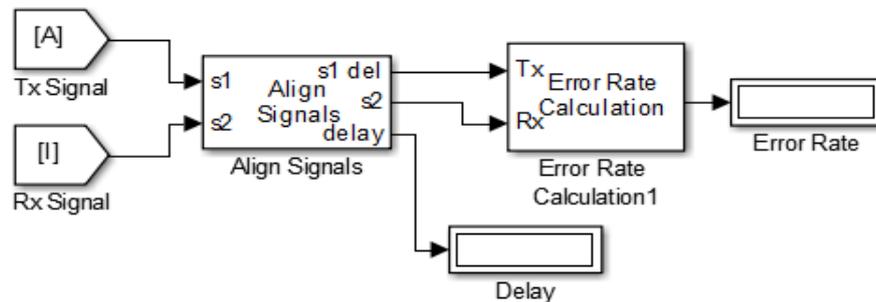

Fig.24. Delay and Error Rate Calculation using Align Signals Block

4.2.2   Error Rate Calculation
Using error rate calculation block (from simulation tool box), calculate the bit error rate which to be depended upon SNR of the system. During the simulation process after 100ms simulation time, the number of bits is 26 bits and the bite error rate was found 0.4615 at SNR equal (10 dB).

V.   Conclusion

The work presented here gives design and implementation of transmitter and receiver of radar system for range calculation using MATLAB/Simulink. The performance evaluation was tested by simulating the design to get the received data which compared with transmitted data. It is observed that the system is more accurate in computing the distance of the target towards the maximum range and also calculate bit error rate (BER). It is noted as the signal to noise ratio (E_b/N_o) increases the bit error rate decreases. Align signal block represents the target available and calculate delay represents target distance from the transmitter. The system developed has virtues such as high accuracy, good efficiency, interference suppression and low power consumption etc.

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