

Low Power CMOS Data Converter with SNDR analysis for High Speed System On Chip Applications

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Abstract: In modern era of advanced VLSI design the transistor sizing and scaling has an considerable impact. There are very essential two constrains, which needs serious attention to the VLSI chip designer are high speed and low power consumption. Therefore in this paper an 8-bit 3 Gs/sec flash analog-to-digital data converter (ADC) in 45nm CMOS technology is presented for low power and high speed system-on-chip (SoC) applications. This low power 8-bit flash Analog to Digital data converter comprises 255 comparators and one thermometer to binary encoder. This flash ADC design is an extended research work of the earlier work related to ADC design using CMOS process technology. The schematic simulation of ADC is done in Tanner-Spice Pro (S-Edit) and layout simulation is done in Tanner-Spice Pro (L-Edit) V.15.14. The Simulated result shows the power consumption in Flash ADC is $41.78\mu W$. The Threshold Inverter Quantization (TIQ) technique is proposed to get $WPMOS/WNMOS < 1$ for transistors to keep the power consumption as low as possible. It is also observed that the ADC consumes $41.78\mu W$ of peak power and $6.45\mu W$ of average power at full speed while it operates on a power supply voltage of $0.6V$. Compared with the earlier work, this project consumes less power and high speed with proposed TIQ technique gives an edge in SoC based VLSI design. Finally the Signal to Noise Distortion analysis is done to obtain more precise data conversion results. The SNDR was found $31.9dB$ for ultimate precise data conversion using 45nm CMOS process technology.

Keywords: System-on-chip based design, flash ADC, Threshold Inverter Quantization technique, Modern VLSI design, SNDR, CMOS process technology.

I. INTRODUCTION

At present scenario, analog to digital converters find applications in communications, high-definition television set top boxes, video projectors, etc. ADCs are interfaced with digital circuits in mixed signal integrated chips, where digital signal processing is performed. The supply voltage for digital devices is decreasing rapidly as the technology scales. Analog to digital converters are required to be operating with these devices, preferably at the same voltages. If the analog and digital components on a chip are not operating at the same supply voltage, then level converters need to be incorporated. There are major two constrains of VLSI/ASIC design. Firstly the circuit should be able to operate at as low voltage as possible, to minimize the power consumption. Secondly the circuit design should be functional at nanometer feature sizes. At such low feature sizes, large device integration is possible. The proposed design meets both criteria.

In this paper, we have successfully implemented a 8-bit low power flash ADC at 45nm CMOS technology. The comparators in the flash ADC have been designed using the threshold inverter quantization (TIQ) technique. While designing these comparators, many transistors have been sized such that $WPMOS/WNMOS < 1$ in order to keep the power consumption as low as possible. The advantage of using these TIQ based comparators over a conventional differential comparator is that a resistor ladder network is not required for providing the reference voltages for the comparators and the comparison speed is faster. In addition, process matching issues are eliminated. This makes the proposed ADC ideal for use in low power and high speed SoCs.

II. RELATED EARLIER WORK

Some related earlier research works of designing flash ADC using CMOS technology are listed as follows. The TIQ technique has been used to design a flash ADC [1]. The focus is on low voltage and high speed design, with supply of $1.8V$ and a conversion rate of 1.3 Gs/sec [2]. A capacitive interpolation technique is employed for a low power design which eliminates the need for a resistor ladder [3]. The next work presents use of digital techniques instead of analog techniques to overcome comparator offset [4]. In 2002 an average termination circuit is proposed [5] to reduce the number of over-range amplifiers, hence reducing the power consumption. An ADC [6] is designed for disk-drive read-channel applications. The authors use a current interpolating technique to design an ADC operating at $1V$ power supply [7]. In another edition [8] the authors have addressed the problem of meta-stability which becomes important when operating at high sampling speeds. They propose a gray encoded ROM as the solution. In the year 2006, it has been shown that the static

nonlinearity presents in the track and hold circuit [9] can be reduced. In 2004, a complementary average value technique has been proposed in which the input signal is pre-processed before comparing it with a fixed voltage reference level in order to simplify the comparator design [10].

III. DESIGN OF 8-BIT FLASH DATA CONVERTER

In this section the proposed 45nm CMOS technology based 8-bit flash analog to digital converter is described. The 8-bit flash (ADC) Analog to Digital Data Converter consists of following blocks: i) comparator bank, ii) 1-out of n-code generators and iii) 255 x 8 NOR ROM.

A. System Specifications: The block schematic diagram is shown in the figure 1 below.

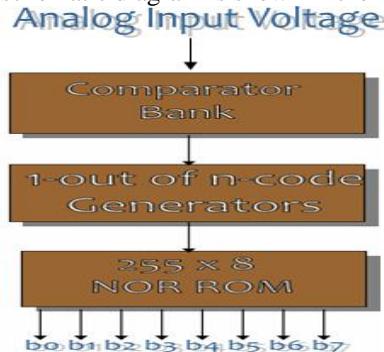


Figure 1. Block diagram of a 8-bit flash ADC

The set of comparator circuit accepts an analog input such as current or voltage and provides an n-bit binary number at the output. Among various analog to digital converters, the flash type ADC is always preferred for the low power and high speed applications. The proposed ADC is designed which meets the specifications shown in table 1 where VLSB denotes the quantization step value of the ADC.

Parameter	Specifications
Resolution	8 Bit
CMOS Technology	45 nm
Architecture	Flash
Power Supply (V_{DD})	0.6 V
V_{LSB}	500 μ V
Speed (Samples /sec.)	3 G
Power Consumption	41.78 μ W
Signal to Noise Distortion Ratio	31. 9 dB

Table 1. Design Specifications of 45nm Flash ADC

B. Proposed Design Approach: The design of an n-bit flash ADC requires the design of $2^n - 1$ comparators, 1-out of n code generators and a $(2^n - 1 \times n)$ NOR ROM. As shown in figure 2, a 4-bit ADC is designed which need 15 comparators, 1-out of 15 code generators and a 15 x 4 NOR ROM. Similarly, for a 8 bit ADC, we designed 255 TIQ based comparators, 1-out of 255 code generators and 255 x 8 NOR ROM. As discussed earlier, the TIQ based technique does not require a resistive ladder circuit like a conventional flash ADC circuit because the switching voltages for the TIQ comparators are determined by the sizes of the PMOS and NMOS transistors in the comparator. Hence the design is much simpler, faster and suitable for low power, low voltage and high speed System-on-chip applications.

Figure 2 shows the circuit diagram for a 4-bit flash ADC based on the TIQ technique. Each of the comparators is designed to switch at a specific reference voltage. We need 24-1 i.e., 15 comparators. As the input analog voltage increases the comparators start turning on in succession from comparator 0 (COMP_0) to comparator 15 (COMP_15). Thus, we get a thermometer code at the output of the comparators. The point where the code changes from one to zero is the point where the input signal becomes smaller than the respective comparator reference voltage levels. This is known as thermometer code encoding, so named because it is similar to a mercury thermometer, where the mercury column rises to the appropriate temperature and no mercury is present above that temperature. The thermometer code is converted to a binary code in two steps. First, the thermometer code is converted into a 1-out of n code using the 1-out of n code generators. This code is subsequently converted to binary code using a NOR ROM. Therefore the input analog voltage is represented by a binary code at the output.

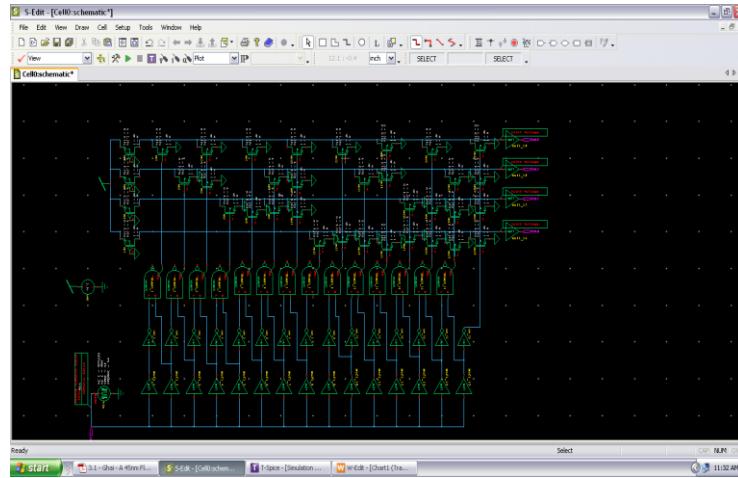


Figure 2. Schematic diagram of a 4-bit flash ADC

A 8-bit flash ADC design is carried out, which consists of such (fig. 2) two sub-circuit blocks of 4-bit flash ADC. Using the SUBCKT Netlist coding the two 4-bit flash ADCs can be merged in Tanner S-Edit full custom schematic design.

IV. DESIGN OF TIQ COMPARATOR

To ensure a high-quality product, the comparator circuit is modified with Threshold Inverter Quantization technique for low power applications.

A. Working Principle: In this paper the Threshold Inverter Quantization (TIQ) technique is used especially for low power applications. The TIQ comparator circuit consists of four cascaded inverters as shown in figure 3. In order to provide sharp switching along with full voltage swing such comparators are very essential.

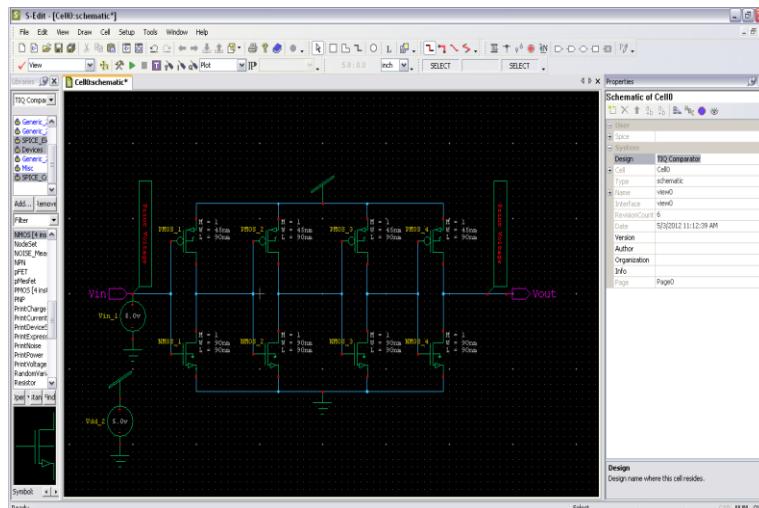


Figure 3. Schematic diagram of a TIQ comparator

The sizes of the PMOS and NMOS transistors in a comparator are the same, but they are different for different comparators. They depend upon the switching voltage they are designed for. The mathematical expression [11] used for deciding these switching voltages is given as:

$$V_{switching} = \sqrt{\frac{\mu_p W_p}{\mu_n W_n}} (V_{DD} - |V_{tp}|) + V_m$$

$$1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}$$

Where, W_p = PMOS width, W_n = NMOS width, V_{DD} = supply voltage, V_m = NMOS threshold voltage, V_{tp} = PMOS threshold voltage, μ_n = the electron mobility, μ_p = the hole mobility, and also assuming that the PMOS length = NMOS length. The sizes of the NMOS and PMOS transistors used in the proposed 8-bit flash ADC corresponding to the minimum and maximum switching voltages are shown in Table 2 below.

TIQ comparator switching voltage(s)	W/L ratio(s) of CMOS used	
248.572 mV	PMOS = 45nm/90nm	NMOS = 90nm/90nm
335.936 mV	PMOS = 120nm/90nm	NMOS = 90nm/90nm

Table 2. Transistor Sizing for Different Switching Voltages

For determining these sizes of the PMOS and NMOS transistors in the comparator a DC parametric sweep is used. The DC voltage was varied from 0 to 0.6V in steps of 500 μ V with NMOS transistors having W/L=90nm/90nm. The length of PMOS transistor was also kept at 90nm, and the width was given a parametric sweep. Therefore 255 switching voltage levels were obtained as shown in figure 4.

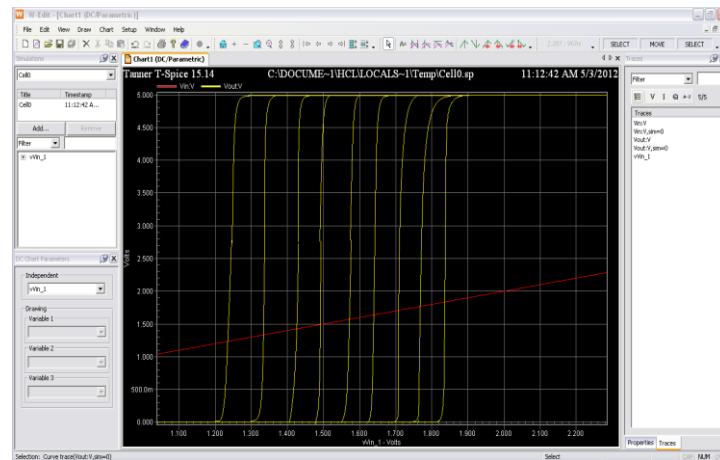


Figure 4. DC sweep analysis of a TIQ comparator

B. Encoder Design: The output of the comparators in a flash ADC is a thermometer code. This thermometer code is converted to a binary code using an encoder in two steps. The thermometer code is first converted into a 1-out-of-n code [12] using 1-out of n code generators, which generates a '01' code. This '01' code is converted into a binary code using a NOR ROM. A NOR ROM consists of PMOS pull-up and NMOS pull-down devices. The PMOS and NMOS sizes for the NOR ROM are 45nm/90nm (W/L) and 90nm/90nm, respectively. We have taken WPMOS < WNMOS to achieve a good voltage swing [13] because a NOR ROM consists of pseudo NMOS NOR gates put together. The logic is that the pull-up network (PMOS) should be narrow enough so that the pull-down devices (NMOS) can still pull down the output safely.

V. SIMULATION RESULTS

In this section the experimental results are analyzed and the functional simulation results are discussed. The following result analysis concludes its performance for low power applications and suitability for high speed. The design simulation and characterization is done using Tanner EDA Tools Pro V.15.14 software [14].

A. Transient Analysis of 8-bit Flash ADC:

A transient analysis of 8-bit flash ADC is performed. A sinusoidal AC signal was generated, going from 248.572 mV to 335.936 mV (which is the full scale range of the 8-bit ADC). The digital codes were obtained correctly, going from 0 to 255 at the output, indicating that the flash ADC was functionally correct. The waveform of 8-bit flash ADC is shown in figure 5 below. The PMOS are of W/L=45nm/90nm and NMOS are of W/L=90nm/90nm. The waveforms of 4 bits are shown below. The total 8-bits are of different voltage levels (binary form). The transient analysis of the 8-bit flash ADC is designed and simulated to prove the functional correctness of the circuit.

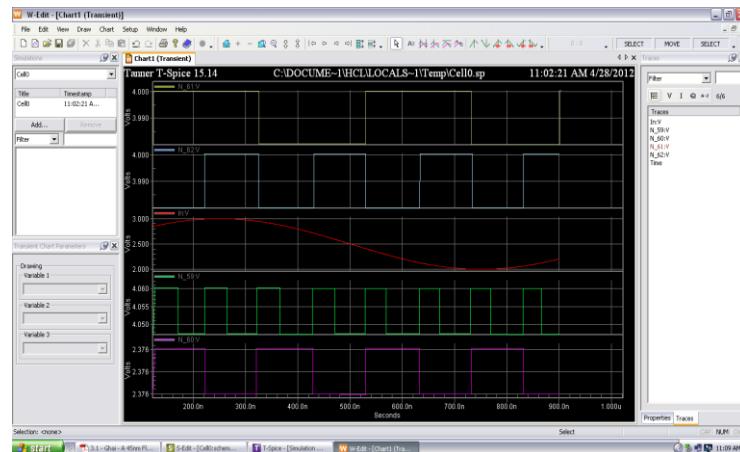


Figure 5. Transient Analysis of 8-bit Flash ADC

B. SPICE Netlist Results: The Tanner SPICE also provides simultaneously the backend Netlist coding along with SPICE Netlist results in 45nm CMOS technology. Figure 6 shows the simulation Netlist result of the flash ADC.

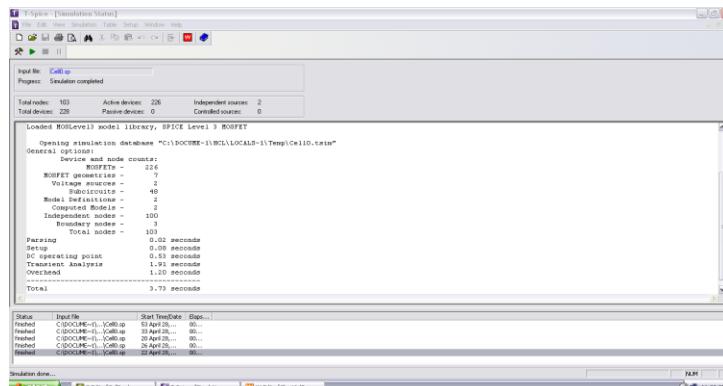


Figure 6. Simulation Netlist Result of 8-bit Flash ADC

C. Power Analysis of Flash ADC: The Threshold Inverter Quantization (TIQ) technique is used with WPMOS/WNMOS < 1 for transistors to keep the power consumption as low as possible. It is also observed that the ADC consumes 41.78 μ W of peak power and 6.45 μ W of average power at full speed while it operates on a power supply voltage of 0.6V. Figure 7 illustrates the detailed power analysis of 8-bit flash ADC.

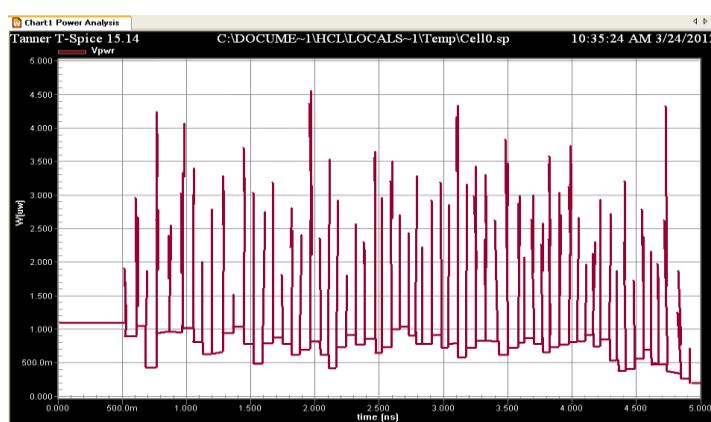


Figure 7. Power Analysis of 8-bit Flash ADC in 45nm CMOS technology

D. Full Custom Layout of 8-bit Flash ADC: Finally the 8-bit flash ADC is analyzed by designing the full custom layout [15] of the target object (ADC). It includes total 255 TIQ based comparators, 1-out of 255 code generators and 255 x 8 NOR ROM. The detailed layout is designed (figure 8) by Tanner Pro L-Edit V15.14 software. Each of all mask layers are clearly classified and verified for the exact output results.

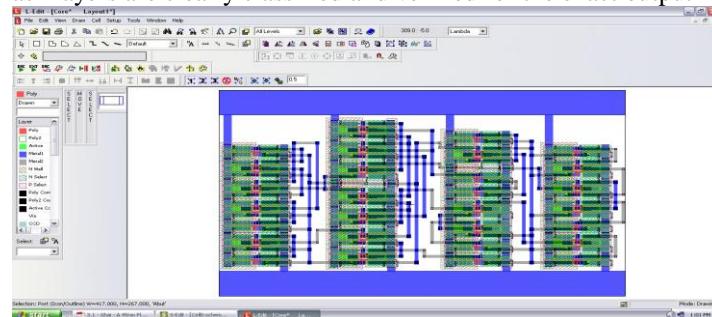


Figure 8. Full Custom Layout of 45nm 8-bit Flash ADC

E. Noise Analysis of proposed Flash ADC: The proposed flash ADC has been also characterized for the differential non-linearity (DNL), integral non-linearity (INL) and the Signal to Noise Distortion Ratio (SNDR).

i) Differential Non-Linearity (DNL): A Verilog-A block has been used to test the DNL. The Verilog-A block generates a slowly varying full scale range ramp to be given as input to the flash ADC, which completes the full scale range in 4096 steps. The flash ADC has 256 codes, so ideally there should be 256 hits per code. But for the transistor level implementation, this is typically not the case. The number of hits per code is recorded, and the DNL is calculated from that. The results show that the ADC exhibits a maximum DNL of 0.70 LSB, which is within the acceptable limits. A DNL error specification of less than or equal to 1LSB guarantees a monotonic transfer function with no missing codes. An ADC's monotonicity is guaranteed when its digital output increases (or remains constant) [Maxim 2000] with an increasing input signal, thereby avoiding sign changes in the slope of the transfer curve. The DNL is calculated from the formula:

$$DNL = |(V_{D+1} - V_D)/(V_{LSB-IDEAL}) - 1| \text{ LSB}$$

Where V_D is the analog value corresponding to the digital output code D and $V_{LSB-IDEAL}$ is the ideal spacing for two adjacent digital codes. For an ideal ADC, $DNL = 0$ LSB.

ii) Integral Non-Linearity (INL): Similar to DNL, a Verilog-A block has been used to test the INL that generates a slowly varying full scale range ramp to be given as input to the flash ADC in 4096 steps. The INL is calculated from the number of hits per code, of course ideally there should be 256 hits per code. The results show that the ADC exhibits a maximum INL of 0.46LSB. The INL is calculated from formula [Maxim 2000]:

$$INL = |(V_D - V_0)/(V_{LSB-IDEAL}) - D| \text{ LSB}$$

Where V_D is the analog value represented by the digital output code D , V_0 is the minimum analog input corresponding to an all-zero output code and $V_{LSB-IDEAL}$ is the ideal spacing for two adjacent output codes.

iii) Signal to Noise Distortion Ratio (SNDR): The ideal formula for SNDR calculation for an ADC is [Maxim 2001]:

$$SNDR = 20 \log_{10} (A_{RMS, \text{Signal}} / (A_{RMS, \text{Noise + Harmonics}})) \text{ dB}$$

Where $A_{RMS, \text{signal}}$ and $A_{RMS, \text{noise+harmonics}}$ are the root mean square (RMS) amplitude for the signal and the noise, respectively. Here, signal means the fundamental amplitude signal, and the noise includes the significant harmonics, which are usually from the second to the fifth highest amplitudes. The signal to noise and distortion ratio (SNDR) of the designed ADC has been measured at an input frequency of 500 KHz. The Flash ADC is fed a sinusoidal input (frequency: 500 KHz) which covers the entire full scale range and the output of the ADC if fed to an ideal digital to analog converter (DAC, modeled as a Verilog-A block). Thus, the output of the DAC is a reconstructed, digitized sine wave at 500 KHz. The FFT of this sine wave is plotted from which the SNDR is calculated. The SNDR was found to be 31.9 dB. The FFT plot is shown in figure 9.

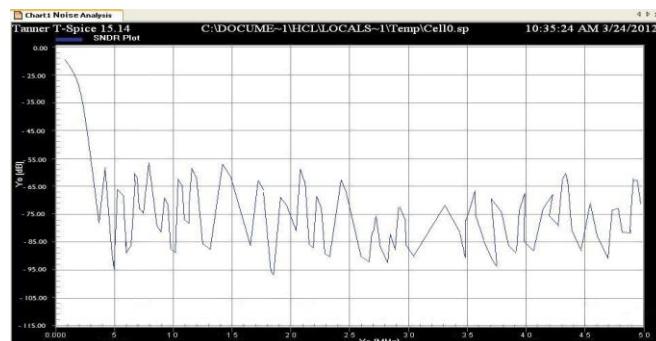


Figure 9. FFT Plot of flash ADC at input frequency of 500 KHz for SNDR Calculation

VI. Future Scope

The design and simulation results of a 8-bit flash ADC using the 45nm CMOS Technology Model has been presented. The design is suitable for low voltages ($0.6V_{DD}$) and high speed (3 Gs/sec) System-on-Chip applications. The ADC consumes a peak power of $41.78\mu W$ and an average power of $6.45\mu W$ and SNDR of 31.9dB. Therefore this flash ADC is successfully designed which is functional at nano-scale CMOS technologies. The layout of 32nm CMOS technology based design is under progress. This project is successfully designed with a layout for a 45nm process. This project can be extended further with the new advent of upcoming 32nm CMOS process technology.

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