IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)
e-ISSN: 2278-2834,p- ISSN: 2278-8735. Volume 5, Issue 4 (Mar. - Apr. 2013), PP 07-14
www.iosrjournals.org

Column decoder using PTL for memory

M.Manimaraboopathy[1], S.Sivasaravanababu[2], S.Sebastinsuresh[3] A. Rajiv[4]
[1, 2, 3&4] *Assitant Professor/ECE, Veltech HighTech DrRangarajan Dr Sakunthala Engineering college -India*

Abstract: *Nowadays memory forms an important and necessary part of every system. In order to make the system more compact and faster, optimization of memory in terms of area, power and speed is to be made. In this paper column decoder has been implemented to minimize the power and area. The memory architecture is simulated using Laker-ADP schematic tool. The number of sense amplifiers required for MxN memory is reduced in ratio 4:1.*
Keywords: *Laker-ADP schematic tool, decoder, memory*

I. Introduction

A conceptual memory array organization is shown in Figure 1. The data storage structure, or core, consists of individual memory cells arranged in an array of horizontal rows and vertical columns. Each cell is capable of storing 1-bit of binary information. In this structure, there are 2^N rows, also called *word lines*, and 2^M columns, also called *bit lines*. Thus, the total number of memory cells in this array is 2^N x 2^M.

To access a particular memory cell, i.e., a particular data bit in this array, the corresponding word line and corresponding bit line must be activated (selected) according to the address coming from the outside of the memory array. The row and column selection operations are accomplished by row and column decoders, respectively. The row decoder circuit selects one out of 2^N word lines according to an *N*-bit row address, while the column decoder circuit selects one out of 2^M bit-lines according to an M-bit column address. The performance of the chip interface circuit determines a measure portion of the total memory speed, especially in high performance SRAMs.

II. Memory Architecture

Architecture consists of 6 transistor bit-cell, precharge circuit, sense amplifier, row decoder, column decoder, control logic.

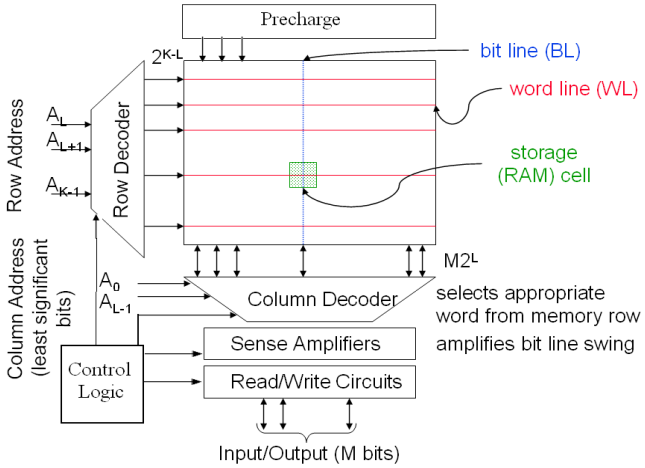


Figure 1 Memory Architecture

2.1 Transistor Memory Cell

The basic cell for static memory design is based on 2 cross-coupled inverters with 2 pass transistors. [1] The memory cell shown in Figure 2 forms the basis for most static random-access memories (SRAM) in CMOS technology. It uses six transistors to store and access one bit. The four transistors in the center form two cross-coupled inverters. Due to the feedback structure, a cell will store either 0 or 1 value. In actual devices, these transistors are made as small as possible to save chip-area, and are very weak. The two lines between the inverters are connected to two separate bit lines via two n-channel pass-transistors (left and right of the cell). The gates of those transistors are driven by a word line.

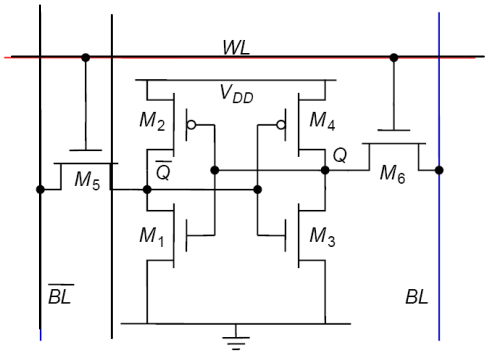


Figure 2 Six-transistor SRAM memory cell [4]

2.2Read Operation

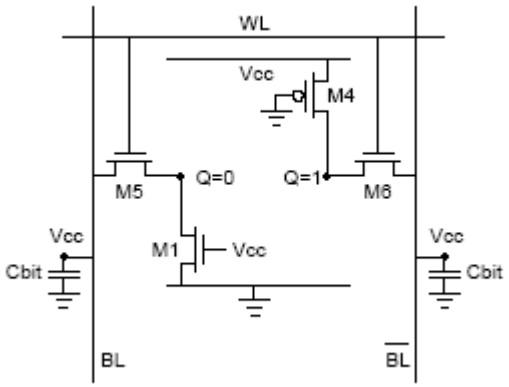


Figure 2a: Six-transistor (6T) SRAM cell at the onset of read operation [4]

The 6T SRAM cell has a differential read operation. This means that both the stored value and its inverse are used in evaluation to determine the stored value. Before the onset of a read operation, the wordline is held low (grounded) and the two bitlines connected to the cell through transistors M5 and M6 (see Figure 2a) are precharged high (to VCC). Since the gates of M5 and M6 are held low, these access transistors are off and the cross-coupled latch is isolated from the bitlines.

If a '0' is stored on the left storage node, the gates of the latch to the right are low. That means that transistor M3 is initially turned off. In the same way, M2 will also be off initially since its gate is held high. This results in a simplified model, shown in figure 3.2, for reading a stored '0' (reading '0').

In the figure the capacitors Cbit represents the capacitances on the bitlines, which are several magnitudes larger than the capacitances of the cell. The cell capacitance has here been represented only through the value held by each inverter (Q=0 and Q=1 respectively).

The next phase of the read operation scheme is to pull the wordline high and at the same time release the bitlines. This turns on the access transistors (M5 and M6) and connects the storage nodes to the bitlines. It is evident that the right storage node (the inverse node) has the same potential as BL and therefore no charge transfer will be take place on this side.

The left storage node, on the other hand, is charged to '0' (low) [4] while *BL* is precharged to *VCC*. Since transistor *M5* now has been turned on, a current is going from *Cbit* to the storage node. This current discharges *BL* while charging the left storage node. As mentioned earlier, the capacitance of *BL* (*Cbit*) is far greater than that of the storage node. This means that the charge sharing alone would lead to a rapid charging of the storage node, potentially destroying the stored value, while the bitline would remain virtually unchanged. However, *M1* is also turned on which leads to a discharge current from the storage node down to ground. By making *M1* stronger (wider) than *M5*, the current flowing from the storage node will be large enough to prevent the node from being charged high.

After some time of discharging the bitline, the bitline signal is given to a specialized detection circuit called Sense Amplifier (see Figure 4) through MUX.

2.3Write Operation

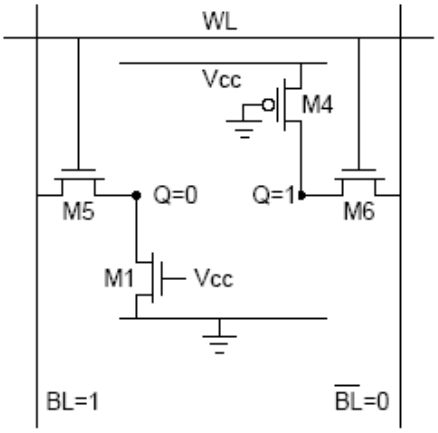


Figure 2b: Six-transistor SRAM cell at the onset of write operation [4] (writing '0'-'1').

For a standard 6T SRAM cell, writing is done by lowering one of the bitlines to ground while asserting the wordline. To write a '0' BL is lowered, while writing a '1' requires BL to be lowered.

In the write operation (Figure 2b) the bitlines no longer are released. Instead they are held at VCC and gnd respectively. If we look at the left side of the memory cell (M1-M5) it is virtually identical to the read operation (figure 3.2). When the wordline is raised M6 is turned on and current is drawn from the inverse storage node to BL. At the same time, however, M4 is turned on and, as soon as the potential at the inverse storage node starts to decrease, current will flow from VCC to the node. In this case M6 has to be stronger than M4 for the inverse node to change its state. The transistor M4 is a PMOS transistor and inherently weaker than the NMOS transistor M6. Therefore, making both of them minimum size, according to the process design rules, will assure that M6 is stronger and that writing is possible. When the inverse node has been pulled low enough, the transistor M1 will no longer be open and the normal storage node will also flip, leaving the cell in a new stable state. [4]

2.4 Precharge Circuit

Precharge plays an important role in decreasing the delay while writing bits into the memory or reading the bits from memory. [1] Precharge circuit makes both, bit line and bit bar line to charge to precharge voltage before carrying out either read operation or write operation. The advantage of precharging the lines lies in the fact that only one line, either bit or bit bar is to discharge compared to the one line charged and other discharged.

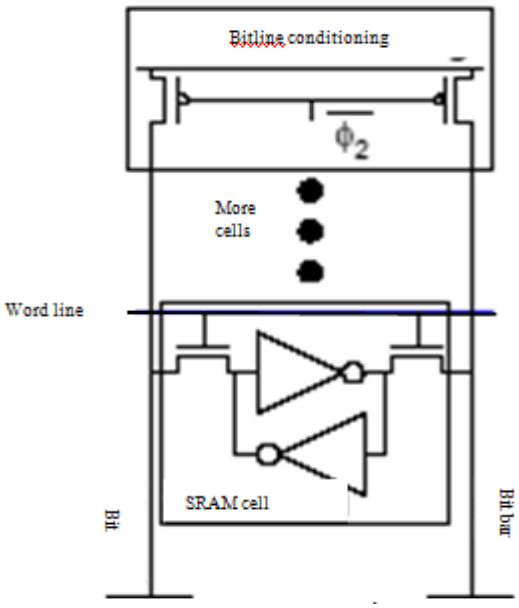


Figure 3 SRAM cell with precharge circuit [5]

Safe read and write operations require a modification of the memory array and timing sequence, based on a precharge circuit. The usual voltage of precharge is VDD/2. Before reading or writing to the memory, the bit lines are tied to VDD/2 using appropriate pass gates. When reading, the *BL* and *~BL* diverge from VDD/2 (Figure 3) and reach the "1" and "0" levels after a short time.

2.5 Sense Amplifier

The sense amplifier (Figure 4) is an important circuit to regenerate the bit-line signals in a memory design. The sense amplifier can be also applied to the receiving of long interconnection signal with large RC delay and large capacitive load signal. Moreover, the complexity of the differential logic circuit can be enhanced by combining the sense amplifier with differential logic networks to reduce the delay time. [3]

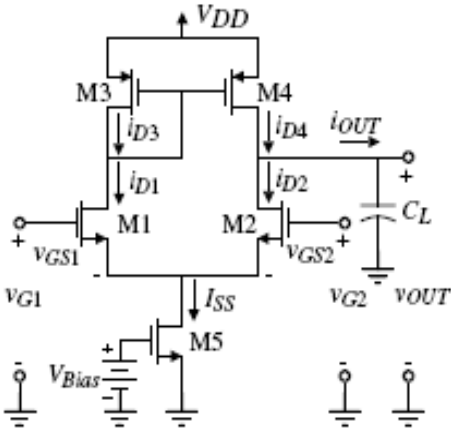


Figure 4 Sense Amplifier

Due to large arrays of SRAM cells, the resulting signal, in the event of a Read operation, has a much lower voltage swing. To compensate for that swing a sense amplifier is used to amplify voltage coming off Bit Line and Bit bar Line.

In order to read out the value of a given bit of a word in this type of memory, the bit-cell voltage, or the magnitude of its charge, needs to be sensed, and the results of this sense operation must be delivered to the rest of the circuit.

2.5 Row Decoder Circuit

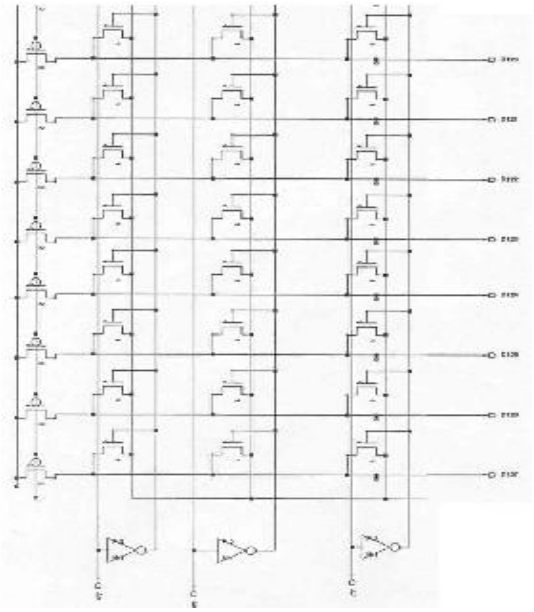


Figure 5 Row decoder [4]

The block diagram of the N:2N row decoder and its associated circuitry is as shown above. Basically, the decoder selects one of 2^N lines, as per the address lines. The output of the decoder is fed to the rows of

SRAM cells. The row decoder selects one of those rows, depending on the N-bit address given to it. A normal decoder can be built using logic gates as we have studied in digital design courses. However, the normal decoder built using logic gates has drawbacks.

2.6 Column Decoder Circuit

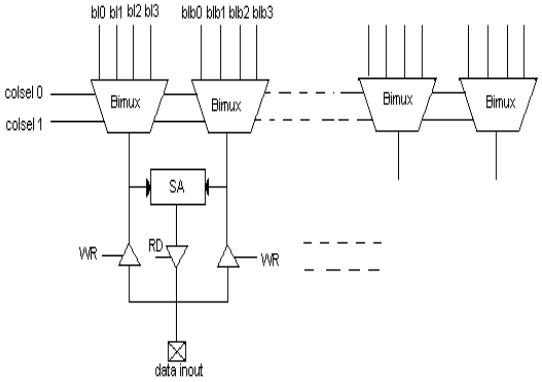


Figure 6 Column Decoder

The column decoder selects a particular column in the memory array for reading the contents of the selected memory cell (Figure 6) or to modify its contents. The column selector is based on the same principles as those of the row decoder. The major modification is that the data flows both ways, that is either from the memory cell to the Data Out signal (Read cycle), or from the Data In signal to the cell (Write cycle).

2.7 Multiplexer (MUX)

The Multiplexing circuit is used to route the data to & from the memory depending on the column address. The inputs to this block are- Output of the column decoder, Input data to be written, read/write (rwb) signal. Here the bidirectional MUX is realized using PTL logic. (Figure 7) As it uses less number of transistors (only NMOS) helps in reducing area and power consumption.

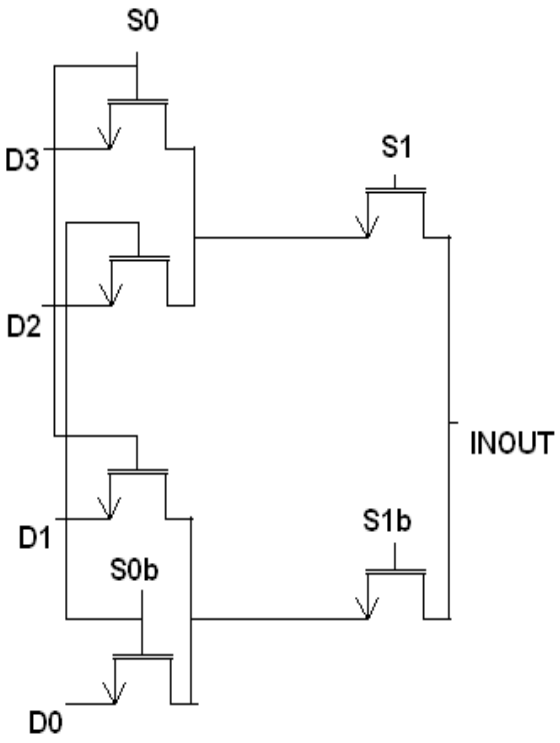


Figure 7 Multiplexer

2.8 Control Logic

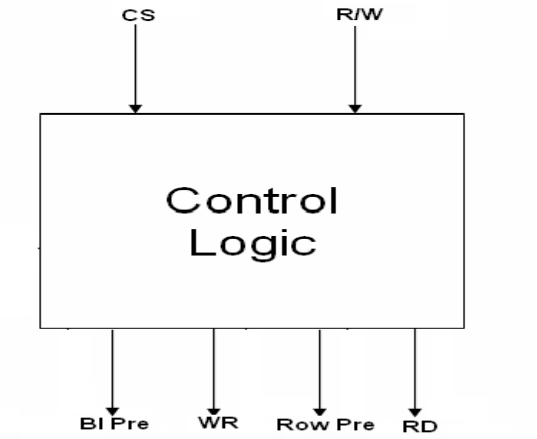


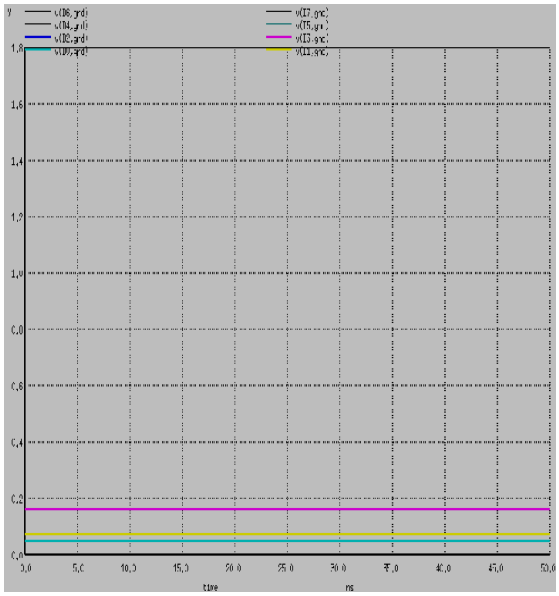
Figure 8 Control Block

Control logic is the most important block (Figure 8) in the Memory. It senses any changes in external signals and issues internal signals based on whether it is a read or write operation. These signals are generated in an order and with accuracy. These signals are routed to memory modules which performs different operation. It also serves as a bi-directional data bus controller. Inputs to the control logic are the chip select signal, read/write signal. The control logic will generate the signals like precharge signal, read enable or write enable, row and column decoder enable.

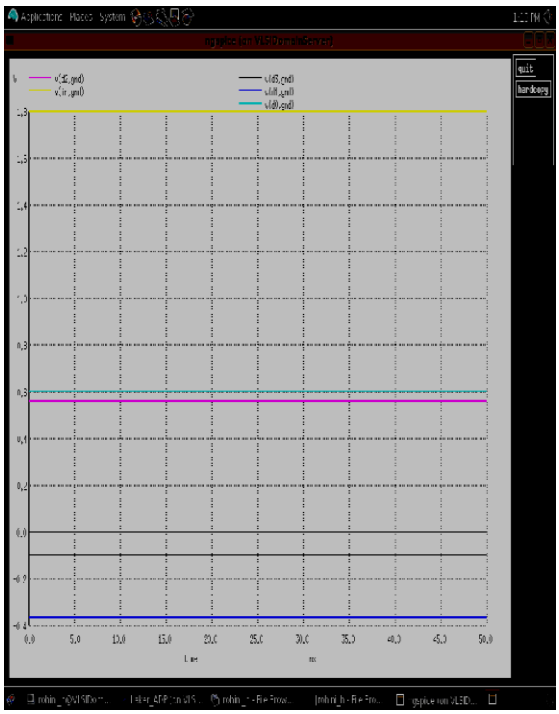
III. Results

Simulation is carried out using Laker-ADP schematic editor to verify the read and write cycle of memory. Main concentration was in reducing area of the memory by reducing area of bimux using PTL logic and even reducing number of sense amplifier required by the ratio 4:1 and still maintaining the performance of the memory. Simulation results for bit cell with sense amplifiers, bidirectional MUX, read cycle are shown below.

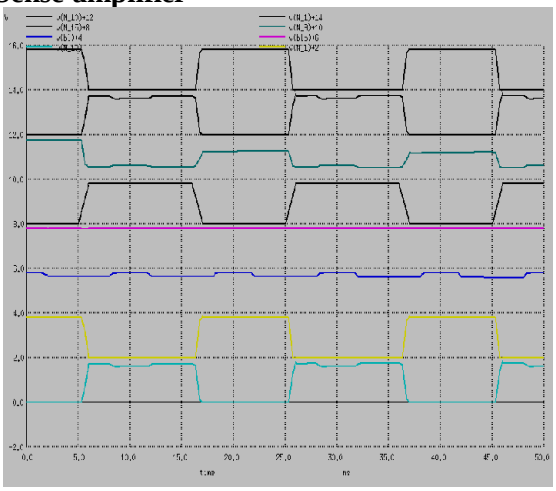
3.1 Output waveforms of Column decoder



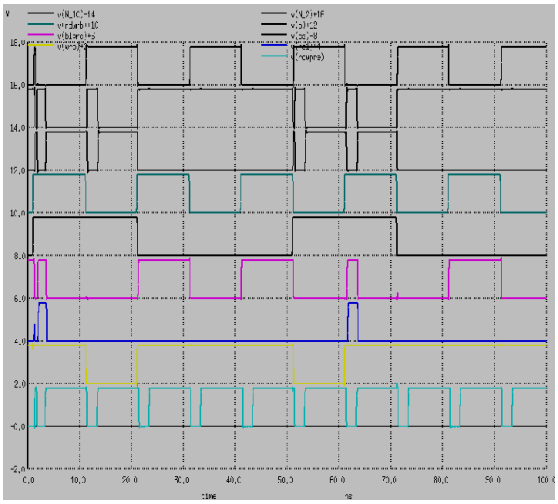
3.2 Output waveforms of Bimux



3.3 Output waveforms of Sense amplifier



3.4 Output waveforms of Control waveform



IV. Conclusion

Today technology has been changing rapidly to meet requirements like speed, area and power. Attempt is made to reduce the area by implementing bidirectional MUX using PTL reducing number of transistors required, which in turn helps in reducing the power.

References

[1] Jan M. Rabaey, Anantha Chandraprakasan, Borivoje Nikolic, "Digital integrated circuits, a design perspective," second edition.
[2] Allen & Holberg "CMOS Analog Circuit Design" Second edition, Oxford University press, 2003.
[3] http://www.cedcc.psu.edu/khanjan/vsrow.htm
[4] Ingvar Carlson, "Design and Evaluation of High Density 5T SRAM Cache for Advanced Microprocessors," Master's thesis performed in Electronic Devices, Ingvar Carlson Reg nr: LiTH-ISY-EX-3481-2004, 23rd March 2004
[5] Ramon Canal CTD – Master, "Memory Structures," CANS Slides based on: Introduction to CMOS VLSI Design, D. Harris