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A Novel Flipflop Topology for High Speed and Area Efficient Logic Structure Design

[1].R.Murugasami,Assistant Professor,[2].B.RekhaStudent of M.E,
[3].Dr.C.N.Marimuthu,
Dean, Nandha Engineering College,Erode-52.

Abstract: *In high speed data path network flop is one of the major functional elements to store intermediate results and data at different stages. But the most important problem is huge power utilization due to switching activity and increase in clock period that is Timing Latency; causes the performance of data path in digital design is decreased. The existing works implement various Flipflop topology in data path structure design such as conventional Transmission Gate Based Master Slave Filpflop (TGMS FF), Write Port Master Slave Flip-flop (WPMS) and Clocked Complementary Metal Oxide Semiconductor (C^2MOS). In WPMS method, area is minimized but delay is increased. In C2MOS technique Power consumption and delay is reduced, but there is a definite scope to reduce Power, area and delay. In this paper a Modified Clocked Complementary Metal Oxide Semiconductor Latch (mC^2MOS Latch) is proposed and delay, power is again reduced up to 60% and the area of the circuit is also reduced while comparing with previous methods.*

Index Terms: *Circuit enhancement, flip-flops (FFs), high-speed, logical effort, master–slave, transmission-gate.*

I. Introduction

Flipflop is a data storage element. The operation of the flipflops is done by its clock frequency [1]. When multistage FF is operated with respect to clock frequency, then it process with high clock switching activity and increased time latency is occurred. Therefore it affects the speed and energy performance of the circuit [2] [3].Whereas in optimal flipflop design is based on automated algorithms that embedded directly into simulators[1][3][4]. While using this algorithm, it optimizes the speed, energy consumption, or energy-delay products, even for complicated flipflops design.

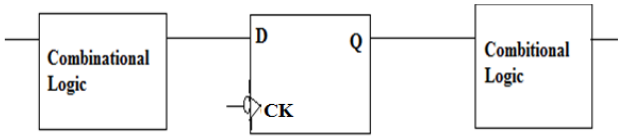
An LE approach is used only when flipflops are in critical path its small output delay can be optimized with its circuit speed [5]. This method is useful for designers to calculate the speed performances of a circuit. LE design is need to optimize the delay with respect to energy and forms the energy-delay products with quite larger.

Transmission gate (or pass-transistors) based master slave (TGMS) flipflops are among the most popular and simplest flipflop topologies and many of them has been proposed in the past. Their features include a small area occupation, few internal nodes to be charged and discharged, during the absence of precharged. Then these factors leads to a small dissipation and thus TGMS FFs can be effectively used for energy-efficient microprocessors [10] [11].

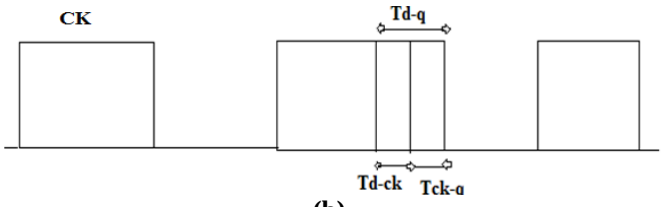
LE optimization is carried on by looking at the whole circuit as a unique uninterrupted path [1].The problem of delay minimization has to be looked at from a different perspective by resorting to a novel approach, which gets inspiration from preliminary considerations [5]. TGMS FFs are split into two overlapping sections and two different paths that are separately optimized [10]. Also energy consumption and area occupation of the resulting designs are always significantly lower than those obtained with the traditional LE method.

II. Timing Behavior For TGMS FFs

A generic stage of a data path structure made up by a negative edge-triggered flipflop is inserted between two combinational blocks as shown in Figure 1 a. The signal CK, clocking the flipflop is reported in Figure.1 b, which uses the falling edge of the clock, during which data is transferred from node D to node Q



(a)



(b)

Figure 1.Pipeline structure. (a) Clock signal (b) FF timing.

The overall timing is introduced by flipflop and affecting the clock period duration is the sum of the above contributions, i.e., the data-to-output delay. To reduce the influence of flipflop timing on pipeline speed performances and the parameter has to be minimized. Hence, it represents the actual figure of merit for flipflop speed.

Flip flops can be basically split into two topological categories: Pulsed FlipFlops and Master Slave FlipFlops (Master Slave).Pulsed FlipFlops: is internally or externally generated time window during which the FF is transparent to the input data. Such a time window implies: 1) a flat minimum region in the $\tau_{D\text{-}Q}$ versus $\tau_{D\text{-}CK}$ curve; 2) a negative $_{set\text{-}up}$ and 3) a continuous topological path from to since is the actual critical input when considering as the figure of merit.

Whereas, Master Slave FlipFlops: are constituted by two latches that are alternately transparent according to the value. This implies: 1) a high to sensitivity in the minimum region; 2) a positive; and 3) the presence of two distinct paths from the input node to the boundary node between master and slave sections, and from this node to the output.

III. Structure Of Transmission Gate

Let us consider the generic structure of a transmission-gate (TG) [or pass-transistor (PT)]-based MS (TGMS) FF is shown in Figure 2.The node X is the boundary between the master and slave sections and the paths relative to $\tau_{D\text{-}CK}$;$\tau_{CK\text{-}Q}$ and $\tau_{D\text{-}Q}$, and delays are depicted with gray lines [1].When $\tau_{D\text{-}CK}$ is sufficiently large, the input signal traverses the master latch and stops at node X, waiting for the slave TG to be enabled by the falling clock transition. After that, the input is transferred to the output.

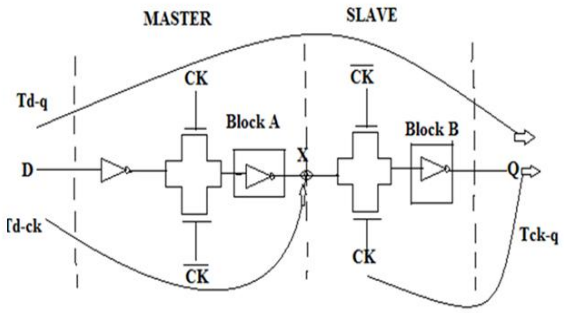


Figure 2. Structure of Transmission Gate Based FlipFlop

When $\tau_{D\text{-}CK}=t_{set\text{-}up}$, the last gate in the master section transfers its input nearly contemporarily to the enabling of the TG in the slave section. However, it will be shown in following, traditional assumption of an uninterrupted path from D to Q is not consistent [10].

IV. Existing Methods

A. Modified Version Of Power Pc 603 For TGMS FF

Consider the typical TGMS FF shown in Figure.3 introduced in [7].In this modified version PowerPC 603 is mainly used for low-power processor. Here, an inverter is added to isolate the D input and provide better noise immunity. The input is transferred to the output with inverted polarity Qb, and simple gates are employed[6].

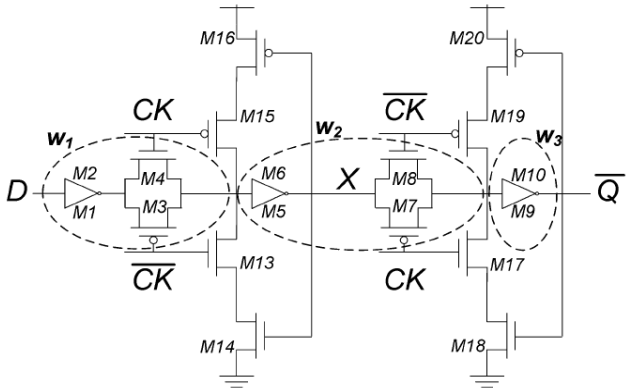


Figure 3. Schematic of TGMS FlipFlop

In particular, the first INV+TG block in the master (M1-M4) has the width W_1 given by the FF input capacitance specifications. Blocks A and B correspond to (M5-M8) are identified by a width W_2, while INV is identified by a width.

The Elmore delay model is applied to determine the expressions of delays of blocks (M1–M4) and (M5–M8) capacitive terms are between parentheses and are multiplied by the resistances from each node to (V_{DD})/ (GND). Diffusion capacitance introduced by each transistor is equaled to its gate capacitance under the same width (it has been verified that they are nearly equal).

The resistance reduction exhibited by stacked transistors due to velocity saturation is neglected in the existing 65-nm technology; it is nearly compensated by strong channel length modulation and DIBL effects. Regarding the parameters of the second stage, they are derived by averaging out two different cases, given here: (i) input of INV M5–M6 is considered as the critical signal. (ii)Enabling TG M7–M8 is considered as the critical signal.

The first delay is the Elmore model and is applied to estimate the delay up to node X, while concerning the second delay, the capacitance at node X is assumed as already charged or discharged through M5–M6.The application of conditions to both paths leads to

$g_{1\text{-}1}\, h_{1\text{-}1} = g_{1\text{-}2}\, h_{1\text{-}2} = \sqrt{F_1} = \sqrt{G1B1H1}$ (1)

$g_{2\text{-}1}\, h_{2\text{-}1} = g_{2\text{-}2}\, h_{2\text{-}2} = \sqrt{F_2} = \sqrt{G2B2H2}$ (2)

$G_1 = g_{1\text{-}1} g_{1\text{-}2}$ / $G_2 = g_{2\text{-}1} g_{2\text{-}2}$ (3)

Where

$g_{i\text{-}j}(h_{i\text{-}j})$ is the logical (electrical) effort of the j_{th} stage in the i_{th} path.

Above equations have to be satisfied the minimized $t_{set\text{-}up}$ and $\tau_{CK\text{-}Qmin}$. Practically by substituting a single variable equation comes out and can be easily identified.

B. Write-Port Master-Slave FF

The Write-Port Master Slave Flip flop (WPMS FF) [8], [9] is shown in Figure.4. It is similar to the FF analyzed in the previous section (TGMS FF) but replaces transmission gates with Pass Transistors (PT) to reduce the clock load, employs partially non-gated keepers and introduces additional logic to speed up the operation of the keepers that have to recover the threshold loss due to pass transistors.

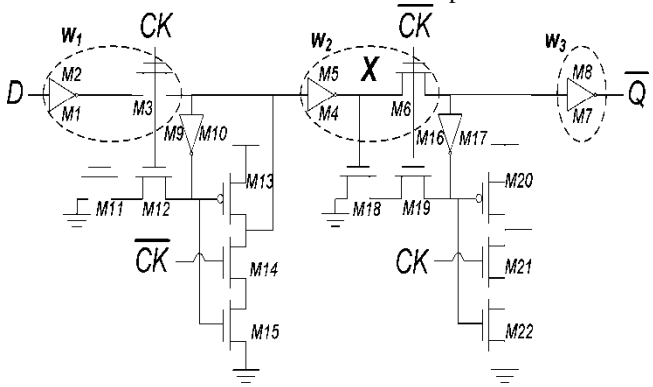


Figure 4. Schematic View of Write Port Master Slave Flip Flop

The resistance of the pass transistors M3 and M6 is considered equal to 1/W when transferring logic "0" and equal to 2/W when transferring a logic "1" This two values are combined thus leading to an average resistance for pass transistors M3 and M6. PMOS transistors M2, M5 and M8 have widths 2W1, 2W2 and 2W3 respectively.

C. C²MOS based Master Slave FF

The C²MOS based Master Slave Flipflop is shown in Figure 5.

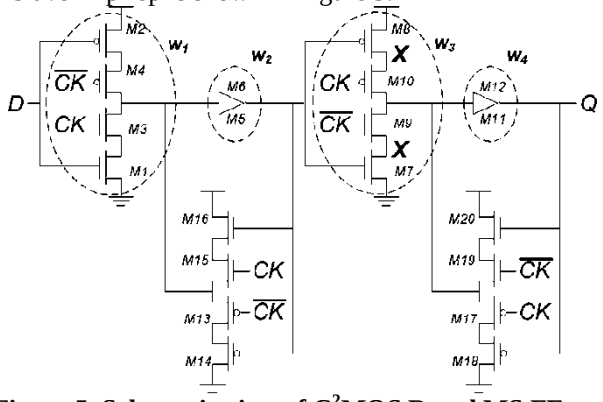


Figure 5. Schematic view of C²MOS Based MS FF

It reconsiders full transmission gates simply with clocked gating transistors.Formally C²MOS is not a pure transmission gate (or Pass Transistor) based flipflop has the gated inverter is actually derived from an inverter plus Transmission Gate and hence the C²MOS can be considered as a topology belonging to the class of Transmission Gate (or Pass Transistor) enables Master Slave FlipFlop.

V. Proposed Method

A. Modified C²MOS based Master Slave Latch

The transmission gate latch and C²MOSlatch is shown in Figure 6A.

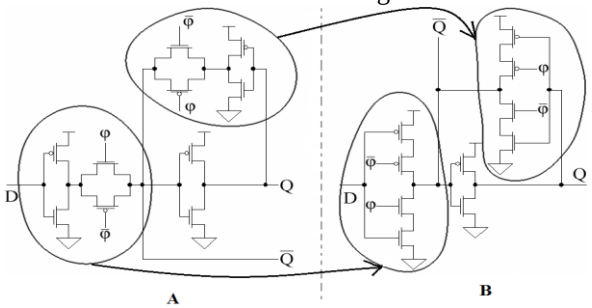


Figure 6A.Transmission gate latch and C²MOS latch

By eliminating the connections at the confluence of the inverter and transmission gate for transmission-gate based

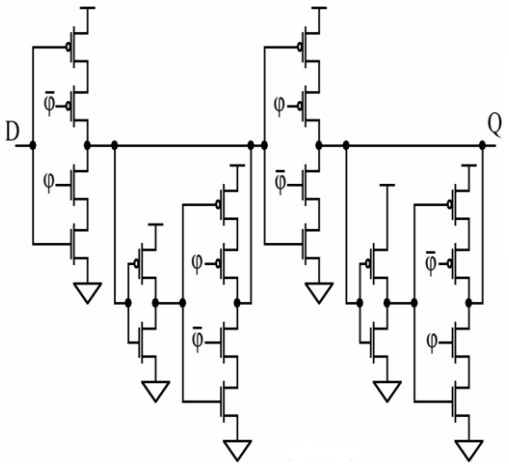


Figure 6B. mC ²MOS latch

latches (Figure A), the latch in (Figure B) may be constructed without loss of functionality. This eliminates a metal connection, resulting in a smaller latch. This structure is called modified C²MOS latch because of the clocked inverters used in it. Flip-flop constructed using mC²MOS latch is shown in Figure 6B. Unlike transmission gate flip-flop, this structure is insensitive to overlap of the clocks.

VI. Results & Discussions

Outputs of these above mentioned FFs was simulated using Tanner software. Outputs of several FF are shown:

A. TGMS FF

Table 1 Working Principle of TGMS FlipFlop

D	CLK	CLKb	Qb
1	1	0	0

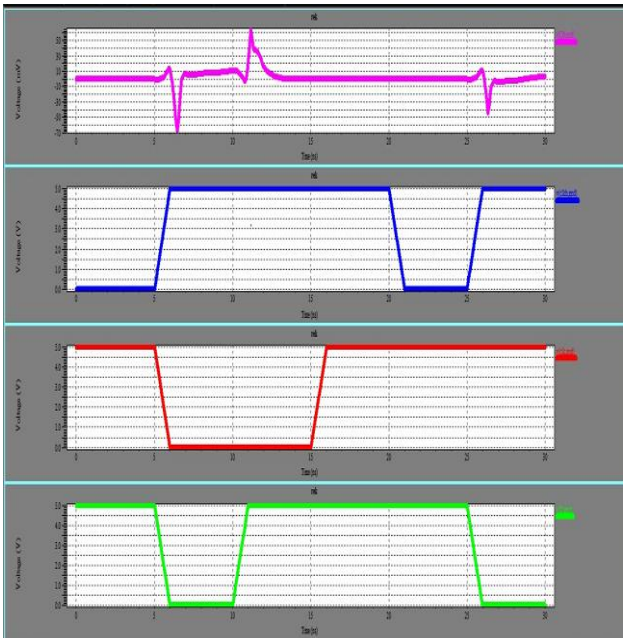


Figure 7. Simulated Output of TGMS FF

In Figure 7 and Table 1 represents to working principle of TGMS FlipFlop circuit and to give Data is 1 at a time clock as 1 then the output generates 0.The average, maximum, and minimum Power consumption of TGMS flipflop is shown in Figure 8.

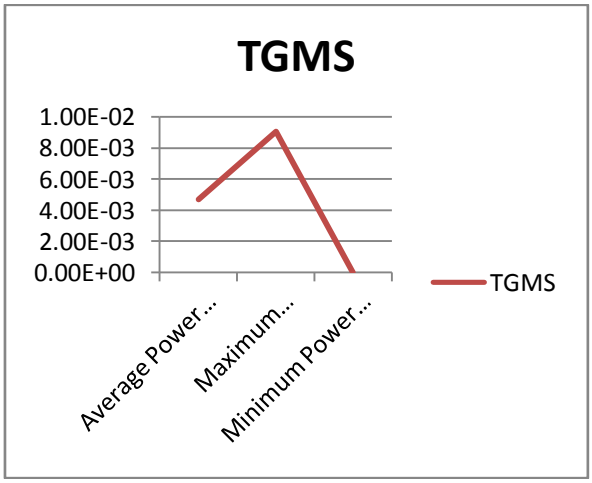


Figure 8. Power Chart of TGMS

The average, maximum, and minimum Power consumption of TGMS flipflop is shown in Figure 8.

B. *WPMS FF*

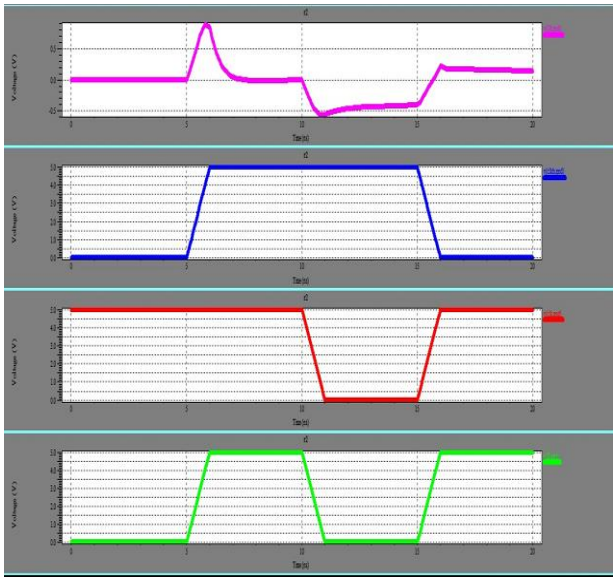


Figure 9. Simulated Output of WPMS FF

Table 2 Working Principle of WPMS FlipFlop

D	CLK	CLKb	Qb
1	1	0	0

In Figure 8 and Table 2 represents to working principle of WPMS FlipFlop circuit and to give Data is 1 at a time clock as 1 then the output generates 0.

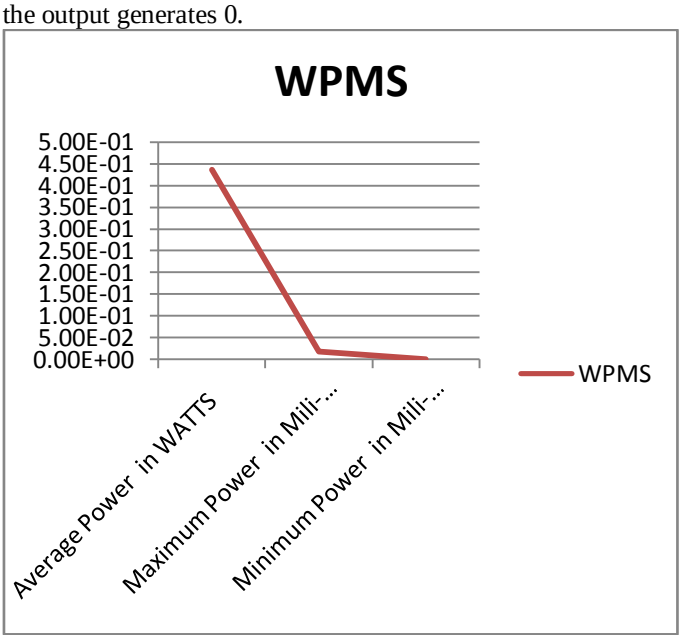


Figure 10. Power Chart of WPMS

The average, maximum, and minimum Power consumption of WPMS flipflop is shown in Figure 10.

C. C²MOS Based MS FF

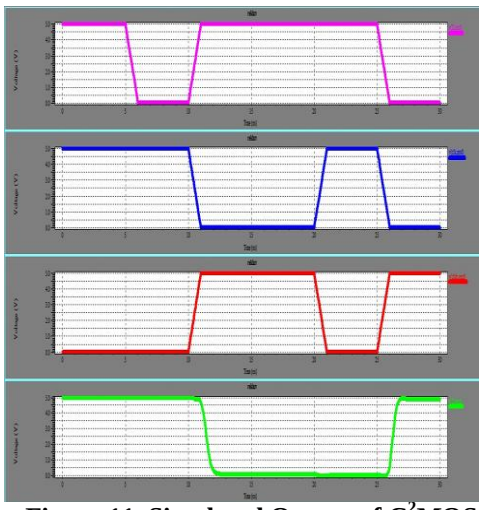


Figure 11. Simulated Output of C²MOS

Table 3 Working Principle of C²MOS

D	CLK	CLKb	Q
1	1	0	1

In Figure 11 and Table 3 represents to working principle of C²MOS based Master Slave FlipFlop circuit and to give Data is 1 at a time clock 1 then the output generates 1.

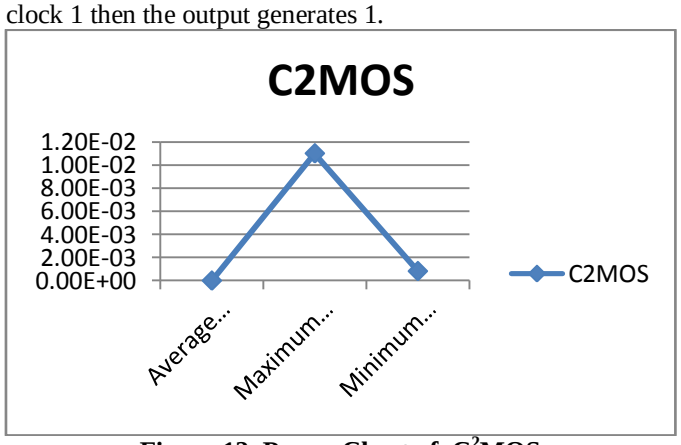


Figure 12. Power Chart of C²MOS

The average, maximum, and minimum Power consumption of C²MOS flipflop is shown in Figure 8.

D. Modified C²MOS

Figure 13. Simulated Output of mC²MOS

Table 4 Working Principle of mC^{2}MOS

D	CLK	CLKb	Q	Qb
1	1	0	1	0

In Figure 13 and Table 4 represents to working principle of WPMS FlipFlop circuit and to give Data is 1 at a time clock as 1 then the output generates 1.Power chart of mC^{2}MOS is shown in Figure 14.

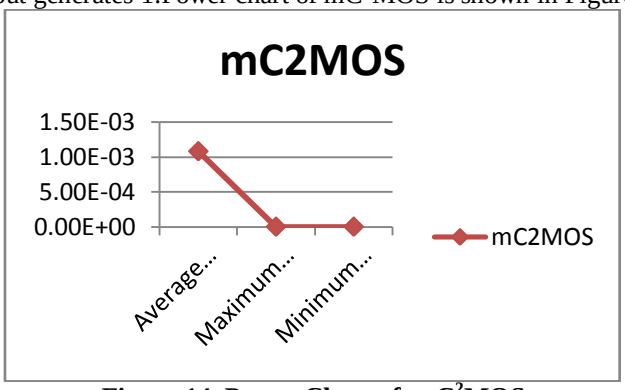


Figure 14. Power Chart of mC^{2}MOS

E. Area Comparison between C^{2}MOS and mC^{2}MOS

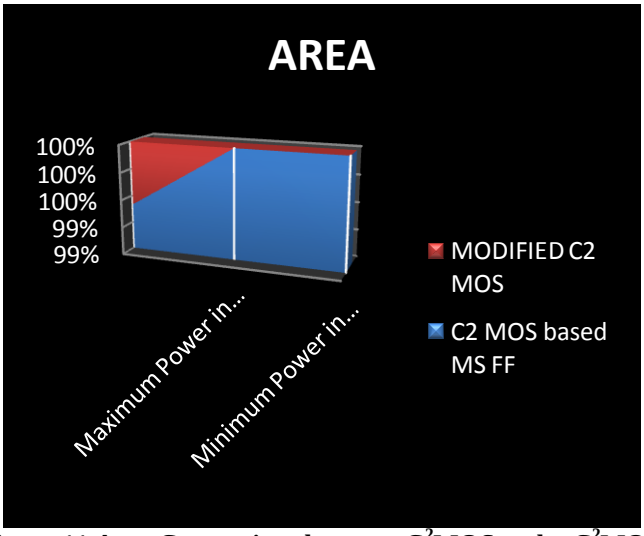


Figure 11.Area Comparison between C^{2}MOS and mC^{2}MOS

F. Power Analysis

Power Comparison Table

In Table 5 shows the power analysis using SPICE tool of TGMS FF and its different topologies such as WPMS, C^{2}MOS and mC^{2}MOSthe average, maximum, minimum power is determined.

Table 5 Power Comparison Table

POWER	TGMS	WPMS	C^{2}MOS	mC^{2}MOS
Average Power in WATTS	4.6e-03	4.3e-01	2.29e-01	1.68e-03
Maximum Power inMili-WATTS	9.3e-03	8.8e-02	8.51e-01	7.08e-07
Minimum Power inMili-Watts	1.2e-05	1.7e-06	2.33e-01	2.12e-05

With this Comparison tablemC^{2}MOS performs better than other latches.

POWER COMPARISON CHART

The Figure 11 show the power analysis shows the power analysis of TGMS FF and its different types such as WPMS, C^2MOS and mC^2MOS with a MOS transistor to determine an average, maximum, minimum power in watts.

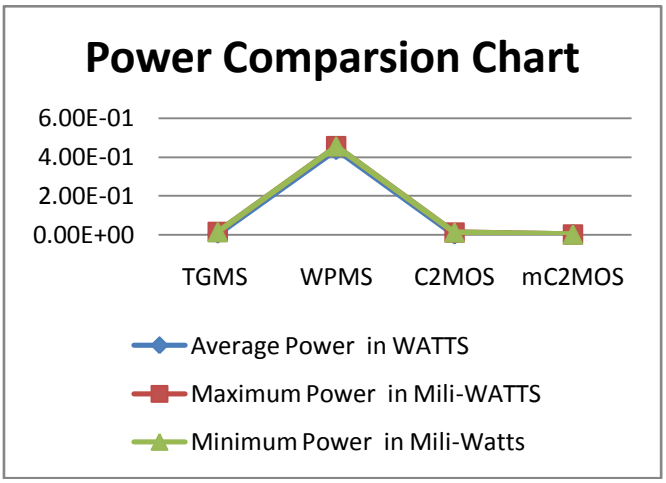


Figure 12. Power Comparison Chart

The power analysis of different flip flop topologies is shown in figure 12. From thiscomparison table mC^2MOS based Master Slave latches preserve 60% power performs better than other existing topologies.

VII. Conclusion

In this work, data path structure is designed using Modified Clocked Complementary Metal Oxide Semi-conductor (mC2MOS) latches. In proposed method existing Flipflop topologies such as TGMS,WPMS and is replaced into a mC2MOS latches and power minimization is done by splitting the whole structure in two different paths and its design is made by two separate LE optimizations are carried out and then merging its result. Such a methodology has been applied on SPICE technology and compared the results with traditionally considering the FlipFlops as whole uninterrupted paths. This method has to achieve better area diminution and preserve energy upto 45% and 60%compared with existing methods. It allows to push the design towards a proper handling of the actual path effort of such structures and hence, to improve the performance when designing for high-speed.

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