

Implementation of an Efficient SRAM for Ultra-Low Voltage Application Based on ST for Better Read Stability and Write Ability

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Abstract: Operation of standard 6T static random access memory (SRAM) cells at sub or near threshold voltages is unfeasible, predominantly due to degraded static noise margins (SNM) and poor robustness. We analyze Schmitt-Trigger (ST)-based differential-sensing static random access memory (SRAM) bitcells for ultralow-voltage operation. The ST-based SRAM bitcells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bitcell. The ST operation gives better read-stability as well as better write-ability compared to the standard 6T bitcell. In this paper we are going to propose a new SRAM bitcell for the purpose of read stability and write ability by using 90nm technology, and less power consumption, less area than the existing Schmitt trigger based SRAM. Design and simulations were done using DSCH and Microwind.

Index Terms: read stability, write ability, Schmitt trigger.

I. Introduction

PORTABLE electronic devices have extremely low power requirement to maximize the battery lifetime. Various device-/circuit-architectural-level techniques have been implemented to minimize the power consumption. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage power reduces linearly (to the first order). However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases. This limits the circuit operation in the low-voltage regime, particularly for SRAM bitcells employing Minimum-sized transistor. These minimum geometry transistors are vulnerable to interdie as well as intradie process variations. Intradie process variations include random dopant fluctuation (RDF) and line edge roughness (LER). This may result in the threshold voltage mismatch between the adjacent transistors in a memory bitcell, resulting in asymmetrical characteristics. The combined effect of the lower supply voltage along with the increased process variations may lead to and increased memory failures such as read-failure, hold-failure, write-failure, access-time failure. Moreover, it is predicted that embedded cache memories, which are expected to occupy a significant portion of the total die area, will be more prone to failures with scaling.

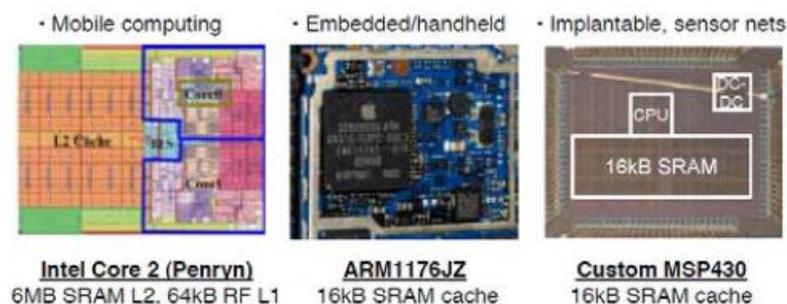


Figure 1. Demonstration of ultra low power SRAM significance from three state-of-the-art examples targeting energy constrained applications.

II. Previous Sram Bitcell Research

Several SRAM bitcells have been proposed having different design goals such as bit density, bitcell area, low voltage operation and architectural timing specifications. In the four transistor (4T) loadless bitcell, pMOS devices act as access transistors. The design requirement is such that pMOS OFFstate current should be more than the pull-down

nMOS transistor leakage current for maintaining data "1" reliably. With increasing process variations and exponential dependence of the subthreshold current on the threshold voltage, satisfying this design requirement across different process, voltage, and temperature (PVT) conditions may be challenging. 5T bitcell

consists of asymmetric cross coupled inverters with a single bitline. Separate bitline precharge voltages are used for read and write operations. The intermediate read bitline precharge voltage requires a dc–dc converter. Tracking the read precharge voltage across PVT corners would require additional design margins in bitcell sizing and may limit its applicability. A 6T bitcell comprises of two cross-coupled CMOS inverters, the contents of which can be accessed by two nMOS access transistors. The 6T bitcell is the “de facto” memory bitcell used in the present SRAM designs. A single-ended 6T bitcell uses a full transmission gate at one side.

Write-ability is achieved by modulating the virtual-VCC and virtual-VSS of one of the inverters. The single-ended 7T bitcell proposed separately by Tawfik *et al.* and Suzuki consists of single-ended write operation and a separate read port. Single-ended write operation in this 7T bitcell needs either asymmetrical inverter characteristics or differential VSS/VCC bias. Takeda *et al.* have proposed another single-ended 7T bitcell in which an extra transistor is added in the pull-down path of one of the inverters. During read mode, the extra transistor is turned OFF, isolating the corresponding storage node from VSS. This results in read-disturb-free operation. In a differential 7T bitcell, the feedback between the two inverters is cut off during the write operation. Successful write operation necessitates skewed inverter sizing, resulting in asymmetrical noise margins. In a single-ended 8T bitcell, extra transistors are added to the conventional 6T bitcell to separate read and write operation. Liu and Kursun have proposed a 9T

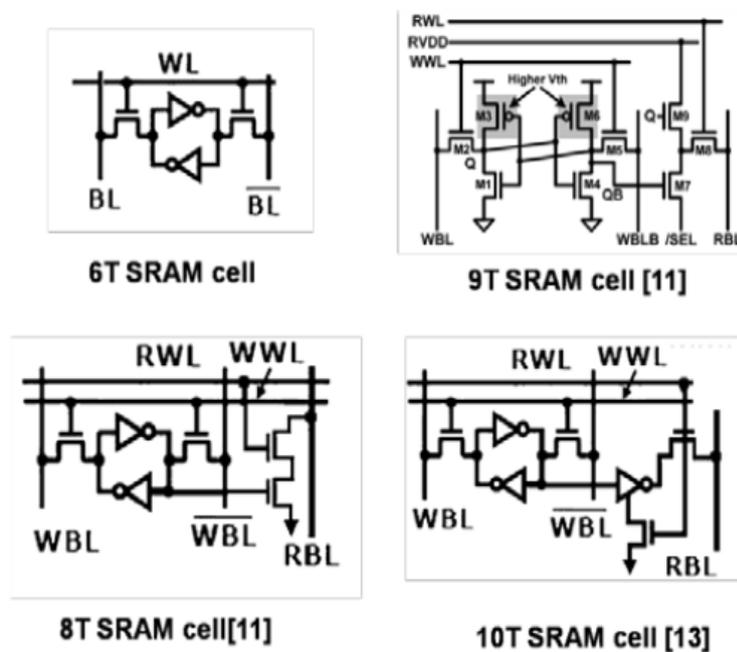


Fig2:circuit diagram of some of sram structures.

III. Need Of Schmitt Trigger Based Sram Designs

In order to resolve the conflicting read versus write design requirements in the conventional 6T bitcell, the Schmitt Trigger (ST) principle for the cross-coupled inverter pair is applied. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. In the existing ST SRAM bitcells, the feedback mechanism is used only in the pull-down path, as shown in figure1. During input transition, the feedback transistor (NF) tries to preserve the logic “1” at output node by raising the source voltage of pull-down nMOS (N1). This results in higher switching threshold of the inverter with very sharp transfer characteristics. Since a read-failure is initiated by a input transition for the inverter storing logic “1,” higher switching threshold with sharp transfer characteristics of the Schmitt trigger gives robust read operation.

For the input transition, the feedback mechanism is not present. This results in smooth transfer characteristics that are essential for easy write operation. Thus, input-dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write-ability of the SRAM bitcell. To maintain the clarity of the discussion, the ST bitcell in [10][11] is termed the “ST-1” bitcell while the other ST bitcell is termed the “ST-2” bitcell shown in the Figures3 and 4 respectively.

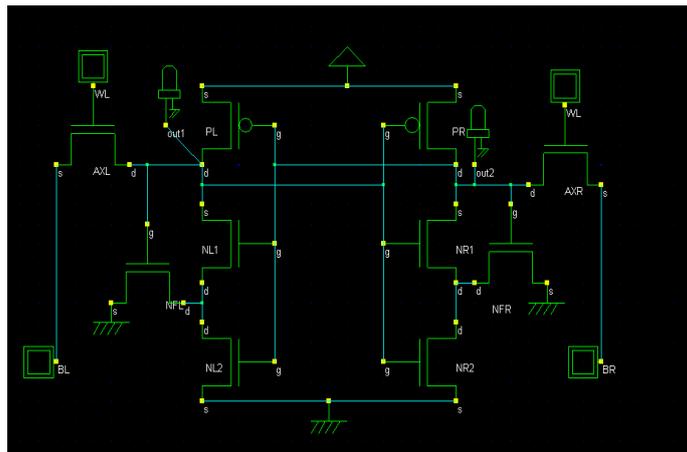


Fig3:st-1 cell

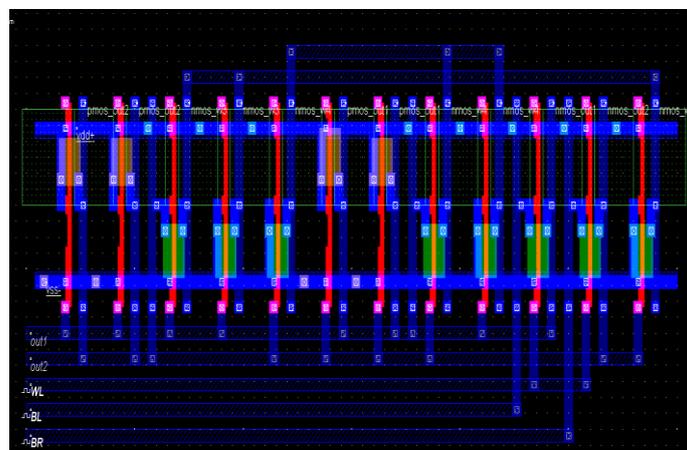


Fig4:layout of st-1 cell

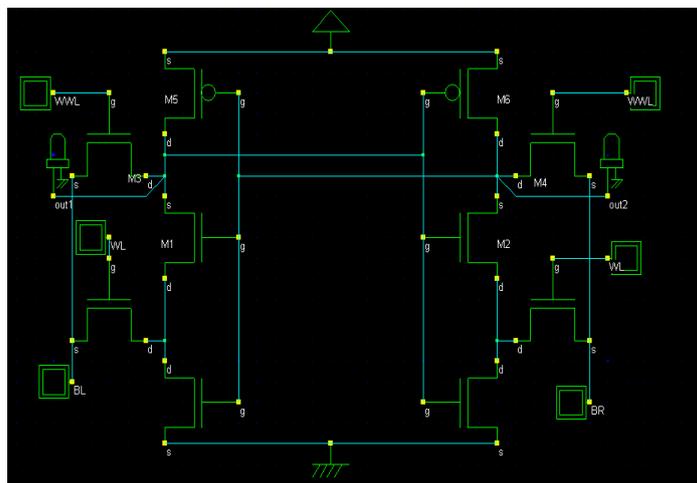


Fig4:st-2 cell

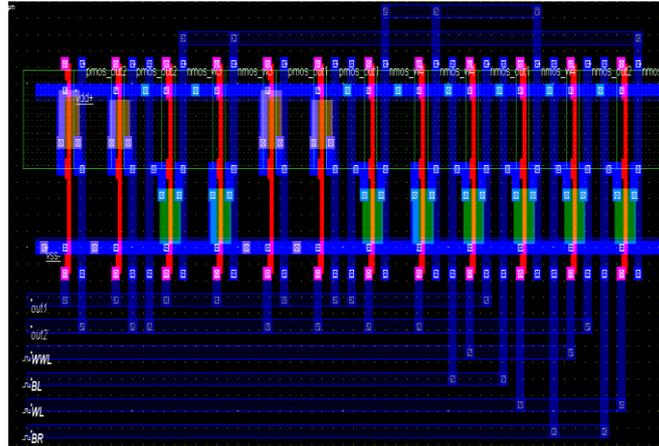


Fig5:st-2 layout diagram

IV. Performance Analysis Of Sram Architectural Co-Design

This section presents the performance analysis of SRAM bitcells such as 6T, 8T, 9T, and 10T with PVT variations. The simulations are carried out in microwind using 90nm technology.

(i) FOUR BIT SRAM CELL DESIGN:

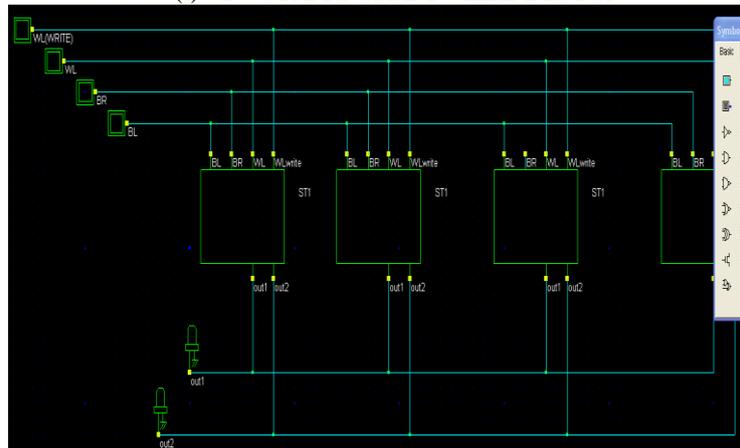


Fig6-fourbit sram cell design for st-1

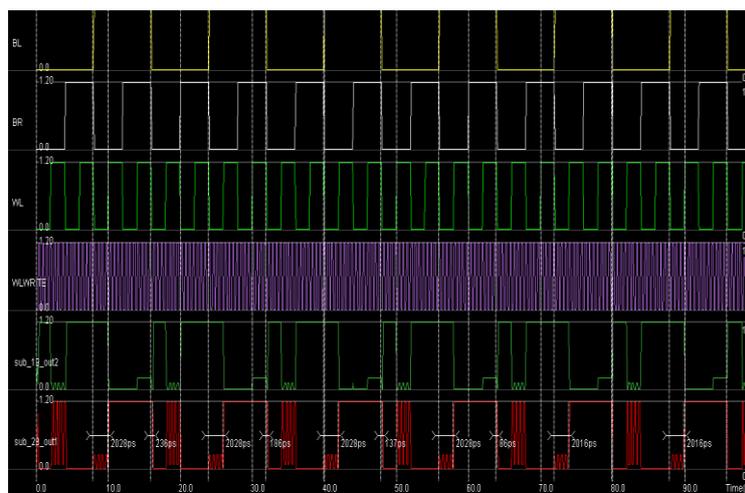


Fig7: waveform of st-1 sram cell

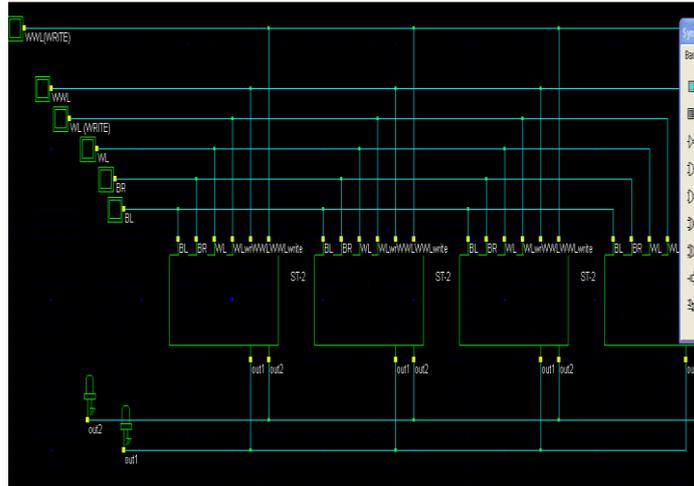


Fig8: fourbit sram cell design fot st-2

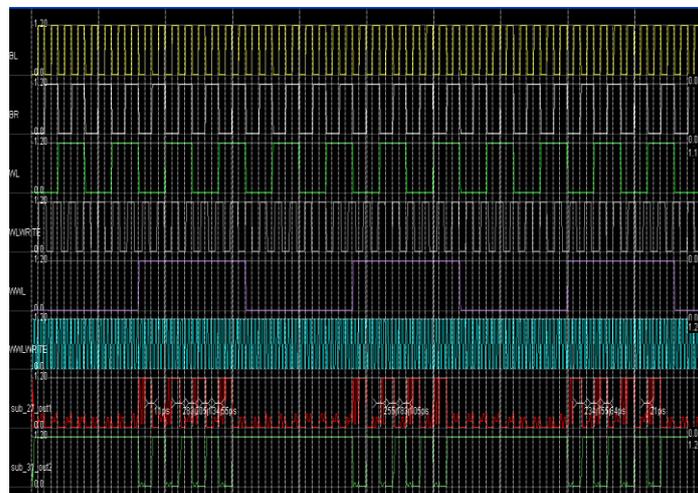
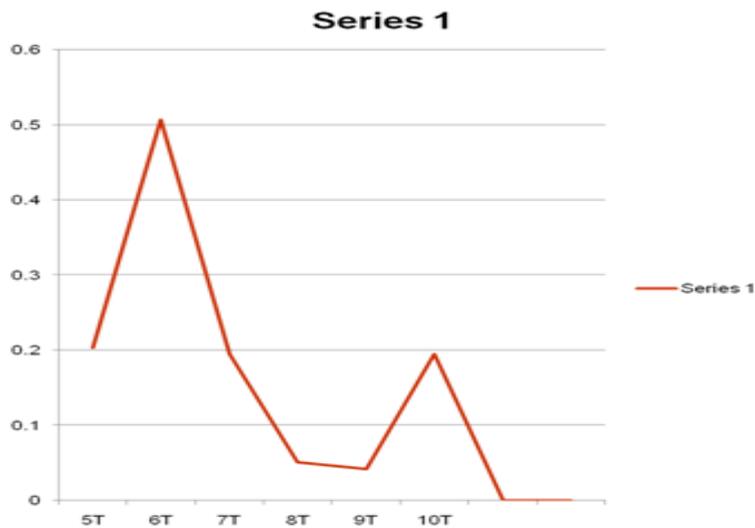


Fig9: waveform of st-2 sram cell



Power graph analysis for 4t to 10t sram design cells



Power graph analysis for ST cells based design

V. Conclusions

Performance comparison of various SRAM bit cells such as 8T, 9T, 10T with the conventional 6T SRAM cell is performed. It has been shown that in terms of leakage power reduction and energy, ST SRAM cell has the best performance in comparison to 8T and 9T cells and 10T. In terms of robustness to variation in temperature.

References

- [1] K. Roy and S. Prasad, *Low Power CMOS VLSI Circuit Design*, 1st ed. New York: Wiley, 2000.
- [2] N. Yoshinobu, H. Masahi, K. Takayuki, and K. Itoh, "Review and future prospects of low-voltage RAM circuits," *IBM J. Res. Devel.*, vol. 47, no. 5/6, pp. 525–552, 2003.
- [3] A. Bhavnagarwala, X. Tang, and J. Meindl, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 658–665, Apr. 2001.
- [4] Jawar Singh, D.K.P., Simon Hollis, and Saraju P. Mohanty, "A single ended 6T SRAM cell design for ultra-low-voltage applications," *IEICE Electronics Express*, 2008.5(18): p. 750-755.
- [5] Mizuno, H. and T. Nagano, "Driving source-line cell architecture for sub-1-V high-speed low-power applications," *Solid-State Circuits, IEEE Journal of*, 1996.31(4): p. 552-557.
- [6] A. Bhavnagarwala, X. Tang, and J. Meindl, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 658–665, Apr. 2001.
- [7] S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS," *IEEE Trans. Comput. Aided Des.*, vol. 24, no. 12, pp. 1859–1880, Dec. 2005.
- [8] H. Kawaguchi, Y. Itaka, and T. Sakurai, "Dynamic leakage cutoff scheme for low-voltage SRAMs," in *VLSI Circuits Symp. Dig.*, Jun. 1998, pp. 140–141.
- [9] J. P. Kulkarni, K. Kim, and K. Roy, "A 160mV robust schmitt trigger based subthreshold SRAM," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.
- [10] R. Aly, M. Faisal, and A. Bayoumi, "Novel 7T SRAM cell for low power cache design," in *Proc. IEEE SOC Conf.*, 2005, pp. 171–174.