

Hardware Implementation of OFDM system to reduce PAPR using Selective Level Mapping on FPGA

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Abstract : OFDM is a modulation as well as multiplexing technique which is widely used in various high speed mobile and wireless communication systems because of its capacity of ensuring high level robustness against interference. In this paper the design and implementation of OFDM system along with SLM implementation to reduce PAPR[6] is illustrated and a detailed simulation of the OFDM system with 16-QAM. OFDM transceiver is implemented using FPGA Spartan6 kit. The hardware results show a detailed study of RTL schematics and Test Bench. In this paper, the software simulation results show 2dB reduction in the peaks.

Keywords - Field Programmable Gate Array, Matlab Simulink, Orthogonal Frequency Division Multiplexing, Peak-to-Average Power Ratio, Selective level Mapping and Xilinx

I. INTRODUCTION

Orthogonal Frequency Division Multiplexing (OFDM) is an attractive multicarrier technique for mitigating the effects of multipath delay spread of radio channel, and hence accepted for several wireless standards as well as number of mobile multimedia applications. Alongside its advantages such as robustness against multipath fading, spectral efficiency and simple receiver design, OFDM has two major limitations.

One of these is its sensitivity to carrier frequency offsets (CFO) caused by frequency differences between the local oscillators in the transmitter and the receiver, phase noise and the other is high peak to average power ratio (PAPR). This high PAPR is due to the summation of sinc-pulses and non-constant envelope. Therefore, RF power amplifiers (PA) have to be operated in a very large linear region. Otherwise, the signal peaks get distorted, leading to intermodulation distortion (IMD) among the subcarriers and out-of-band radiation. A simple way to avoid is to use PA of large dynamic range but this makes the transmitter.

The paper aims at successful implementation of the transceiver on a FPGA which would pave a way towards developing an OFDM system which resolves the issue of high PAPR. Simulation results using System Generator and Matlab/Simulink and XILINX tools have been given. Finally it aims at development of a complete system which then results in robust, maximum throughput, highly scalable wireless LAN network.

II. OFDM, PAPR AND SLM

2.1 General OFDM Block Diagram Descriptions

2.1.1 OFDM Transmitter

The model considered for the implementation of the OFDM transmitter is the shown below and basically consist of [13]

Serial to parallel converter, Constellation modulator, IFFT block, Parallel to serial converter, Digital to Analog converter, Selective Level Mapping

2.1.2 OFDM Receiver

OFDM receiver is the shown below and basically consist of [13]

Analog to digital converter, Serial to parallel converter, Cyclic prefix removal, FFT block, M-QAM decoder, Parallel to serial converter.

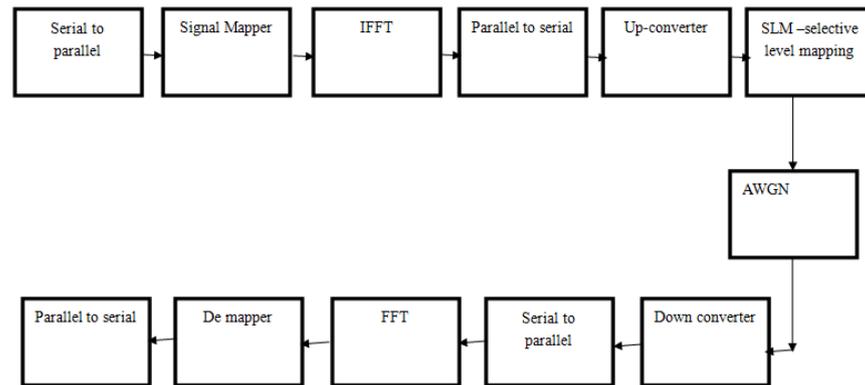


Fig 2.1. Block diagram of an OFDM system

2.2 Peak- to- average Power ratio-PAPR

The major disadvantage of using several subcarriers in parallel using IFFT is the highly non-constant envelope of the transmit signal, making OFDM very sensitive to nonlinear components in the transmission path. A key component is the high power amplifier (HPA). Due to cost, design and most importantly power efficiency considerations, the HPA cannot resolve the dynamics of the transmit signal and inevitably cuts off the signal at some point causing additional in-band distortions and adjacent channel interference. The power efficiency penalty is certainly the major obstacle to implement OFDM in low-cost applications. Moreover, in power-limited regimes determined by regulatory bodies, the average power is reduced compared to single-carrier systems reducing in turn the range of transmission. The power control problem motivates further research since it touches on many of the advantages that originally made OFDM transmission popular, i.e. spectral efficiency and implementation issues.

In OFDM systems, a fixed number of successive input data samples are modulated and then jointly correlated together by use of IFFT at the transmitter side. IFFT processes signals to produce orthogonal data sub-carriers . Mathematically, IFFT combines all the input signals to produce each one of the output symbols.

. The signal processing by IFFT in the OFDM transmitter changes the statistical distribution of signals from uniform-to-Gaussian. Therefore, the dynamic range of the OFDM output envelope is most often higher than that of the single-carrier systems. However, PAPR is widely used to evaluate the dynamic range of the output envelope. The PAPR (in dB) is defined by the following equation [14]

$$PAPR=10\log_{10} \left\{ \frac{P_{peak}}{P_{avg}} \right\} = 10\log_{10} \frac{\max[|x(n)|^2]}{E[|x_n|^2]} \tag{1}$$

where P_{peak} represents peak output power, $P_{average}$ is average output power. $E[\bullet]$ denote the expected value, x_n represents the transmitted OFDM signals which are obtained by taking IFFT operation on modulated input symbols X_k . x_n is also expressed as[12]

$$x_n = \frac{1}{\sqrt{N}} \sum_{K=0}^{N-1} X_k W_N^{nk} \tag{2}$$

2.3 Selective Level Mapping - SLM

Selective level Mapping (SLM)[6] was first proposed in 1996 to reduce PAPR in OFDM systems. The system block diagram of SLM is shown below. At first, the input information is divided into OFDM data block X, which consists of N symbols, by the serial-to parallel (S/P) conversion and then data block X is multiplied carrier wise with each one of the U different phase sequences B(u), resulting in a set of U different OFDM data. In the SLM[8] algorithm the data source denoted as X, is multiplied by the U different sets of phase factors/masks, element-wise to produce U different copies of X,

$$X_u = B_u X \quad u= 1, 2, \dots, U \tag{3}$$

where U is the design parameter in SLM. In general, more reduction in PAPR is likely to achieved when U increases.[12]. In addition, B_u is defined as:

$$B_u=[B_{u,1} B_{u,2} B_{u,3} \dots B_{u,(N-1)}] \tag{4}$$

Then all U alternative data blocks (one of the alternative sub-carrier sequences can be the unchanged original one) are transformed into time domain to get transmit OFDM symbol where N represents the number of subcarriers in IFFT and $B_{u,k}$ is given by:

$$B_{u,k} = e^{j\theta_{u,k}} \quad k = 0, 1, 2, \dots, N - 1 \quad (5)$$

After multiplying X with the phase factors, each X_u is processed by IFFTs and its PAPR is then computed and compared with the others. The resulting signal that yields the lowest PAPR is subsequently chosen for transmission. In addition, the B_{opt} which implies the optimal B_u that produces the lowest PAPR has to be transmitted to receiver as a side information[14]. The receiver will then use B_{opt} to recover the data source, X[6].

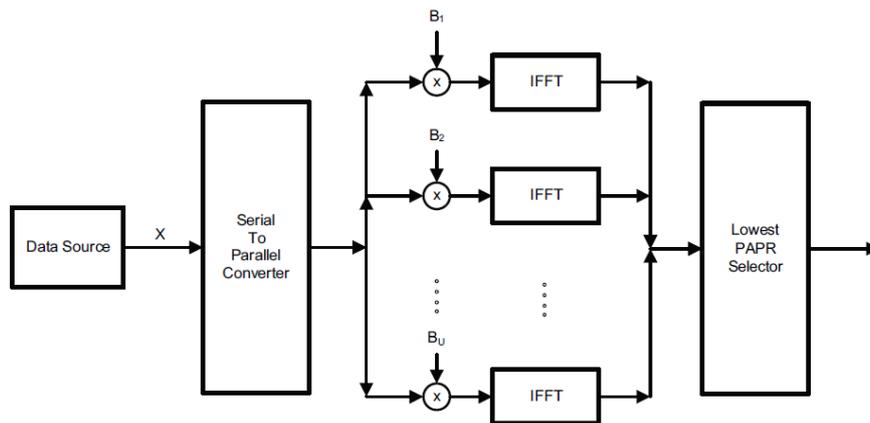


Figure 2.2 Block diagram of SLM[6]

III. IMPLEMENTED OFDM MODEL

Transmitter Design

In the design presented, block length of 8 points and 4 different phase sequences are used. Transmitter subsystem design contains 4 independent OFDM modulators. In the modulator, the input data is multiplied by a look-up table from ROM before giving it to actual OFDM modulation process. This lookup table holds the phase sequences for each block. The output of each block is given to a PAPR calculator and selector. It transmits the data block with lowest PAPR and also transmits the selected block number.

Receiver Design

The receiver is a normal OFDM receiver with a phase sequence selector block. The data stream is first given to FFT block for decoding. Then the data stream is passed to a lookup table multiplier which multiplies data with a phase sequence as indicated by the selected block number from transmitter.

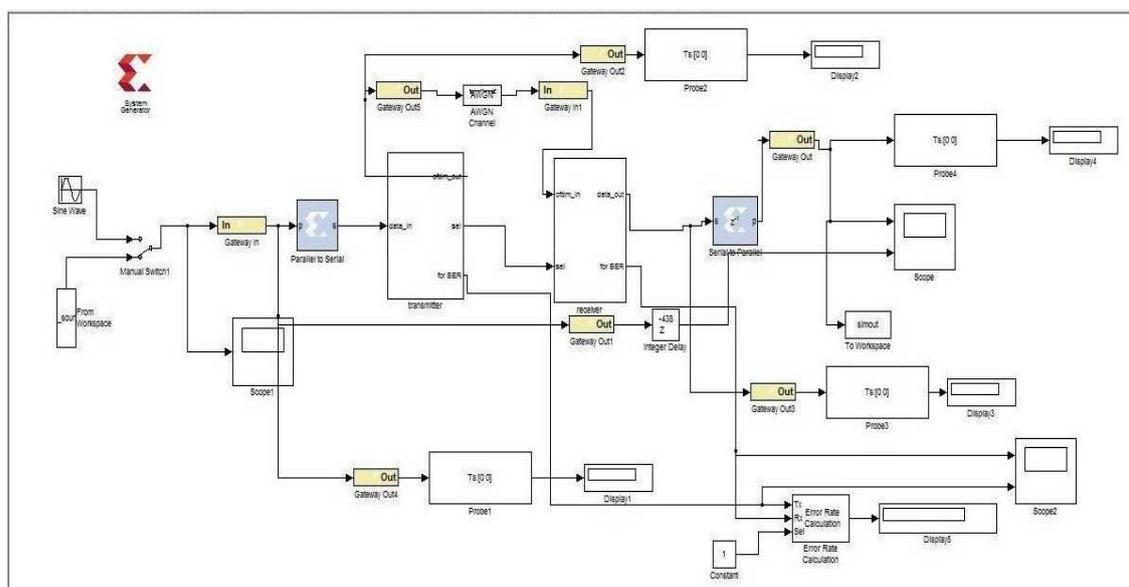


Figure 3.1 Block diagram of the designed system

IV. Simulation Results

Table 4.1 indicates PAPR values with SLM and without SLM. Last column shows Crest Factor(\sqrt{K}). It is evident from the table that PAPR reduction of about 2 dB is obtained using 64 carriers. Varying difference in PAPR is obtained using 2,4,8 and 64 number of carrier. PAPR reduction of nearly 1.6dB is obtained using 2 carriers. Higher reduction of PAPR is obtained using 8 carriers

TABLE 4.1 PAPR obtained with and without SLM, CREST FACTOR

Number of Sub-carriers	PAPR (K) without SLM in dB	PAPR(K) with SLM in dB	Difference in PAPR	Crest Factor $=\sqrt{\text{PAPR}}$ $=\sqrt{K}$
2	12.61	11.01	1.6	1.264
4	25.22	24.01	1.21	1.1
8	37.83	35.03	2.77	1.67
16	50.45	48.89	1.56	1.24
32	63.06	62.01	1.59	1.024
64	75.76	73.76	2	1.414

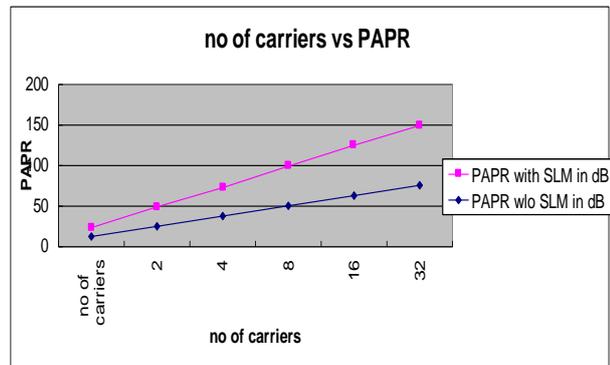


Fig 4.1 Number of carriers v/s PAPR

As number of subcarriers increase the PAPR increases. Implementing the proposed technique PAPR can obtain reduction in PAPR.

V. Hardware Implementation

The hardware simulation[24] of the model was carried out in step by step manner. Small models of the components of the model were made and their outputs on the wavescope were observed. RTL logic and test benches of the intermediate models were obtained.

The detailed description of the intermediate blocks is shown below:

5.1 Experiment No.1 - Serial to Parallel

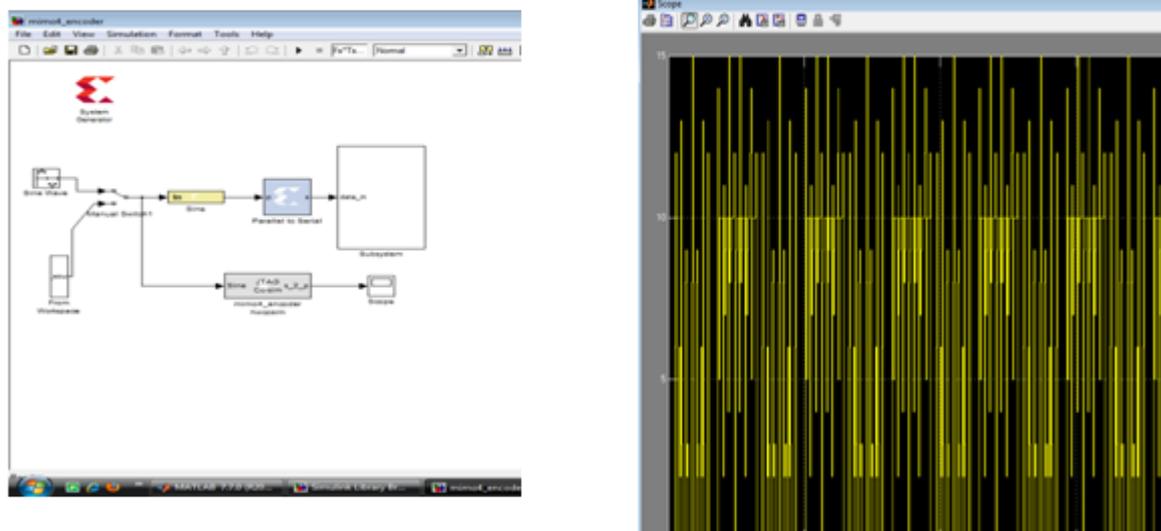


Fig 5.1 (a) hardware model of serial to parallel (b) wavescope results of FPGA simulations

Fig 5.1 (a) hardware model of serial to parallel (b) wavescope results of FPGA simulations The hardware model using JTAG is shown in fig 5.1(a) and the wavescope results of the same is shown in fig 5.1(b) . The RTL schematic for the above model is as shown below.

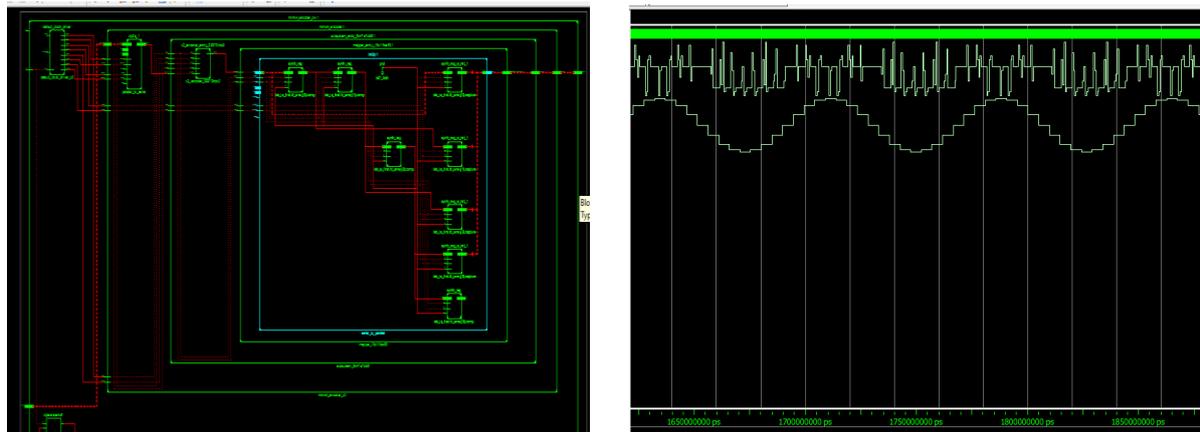


Fig 5.2 (a) RTL Schematic (b) Test Bench

This completes the hardware simulation of serial to parallel

5.2 Experiment no. 2 - FFT block

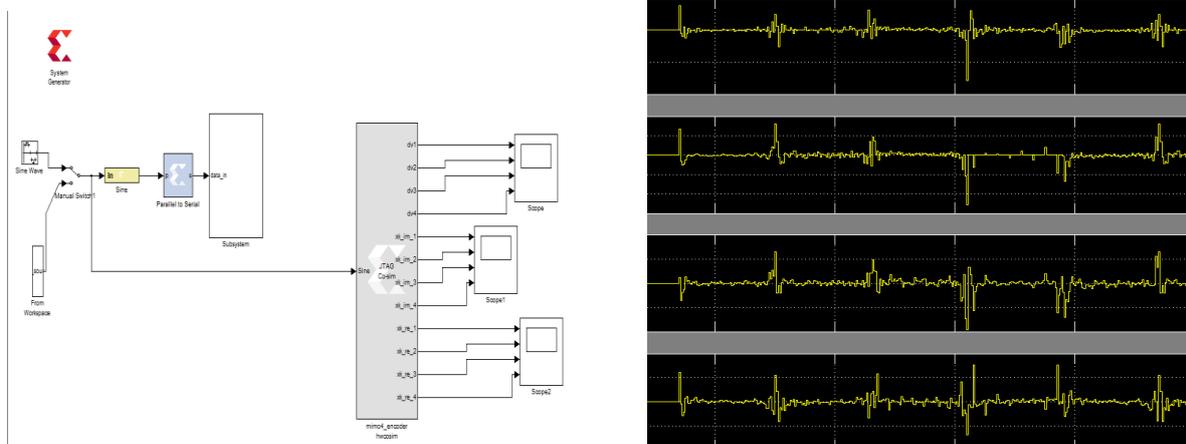


Fig 5.3 (a) hardware model of FFT (b) wavescope results of FPGA simulations

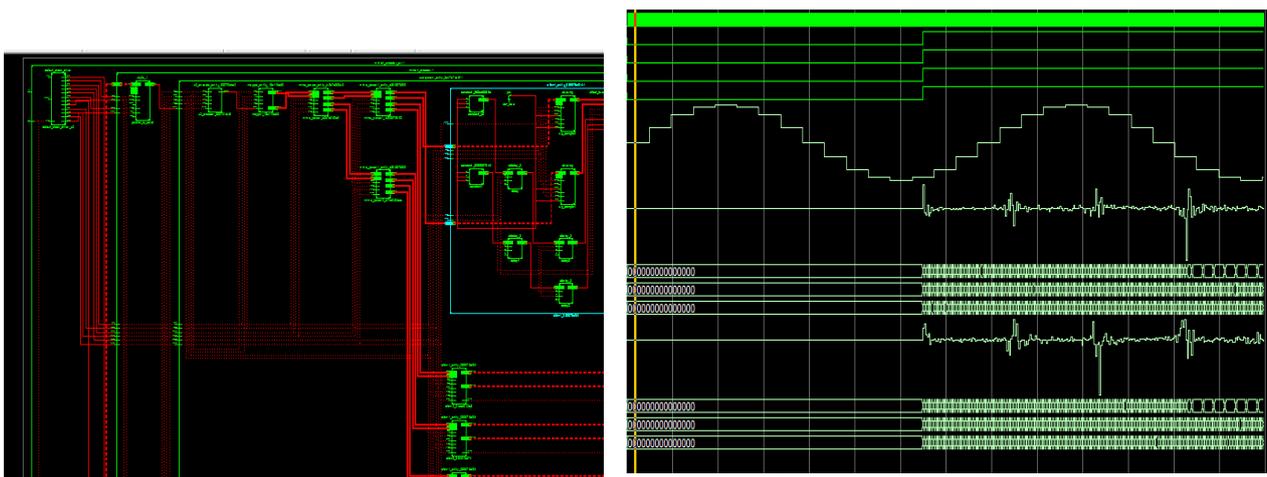


Fig 5.4 (a) RTL Schematic (b) Test Bench

1.3 Experiment No. 3 - Hardware Simulation of Entire Model

Using XILINX and modelsim the developed simulink model is converted into its JTAG equivalent.[2]

Internal simulator of XILINX, i-sim can also be used in place of modelsim.[20]

The hardware implementation of the simulink model is done using JTAG. The process of developing such a hardware is called Hardware-In-Loop.

VI. Conclusion

OFDM is a very attractive technique for wireless communications. One of the serious drawbacks of OFDM is its high PAPR when the input sequences are highly correlated. The PAPR obtained without SLM for OFDM system is 12dB and with SLM is 10dB resulting in overall reduction of 2dB. Thus SLM technique has the potential to reduce PAPR for OFDM systems and improve its performance in terms of low PAPR high SNR and improved BER.

Xilinx System Generator combined with Matlab Simulink provides an easier and efficient way of developing the FPGA system design and simulating it. Also the hardware co-simulation feature of the software enables easier way to test and debug the design effectively on the actual hardware

The hardware co-simulation, RTL Schematics, Test Bench and VHDL codes, are also obtained for the implemented OFDM system. First the model is created in the Matlab/Simulink environment. The Matlab Simulations were carried out and necessary modifications were done. The hardware co-simulation was done to run the model on the hardware platform. The VHDL code, RTL Schematics and Test Bench were generated for the model. Test Vectors are passed through the test bench to verify functionality of the each block of the model. At the end complete functionality of the model is verified using Matlab Simulations, Test Bench/Modelsim Simulations and Hardware co-simulations.

VII. FUTURE SCOPE

The paper deals with reduction of PAPR in a SISO OFDM. The concept of reduction of PAPR can be implemented in MIMO technology. If such a model is implemented it shall give the advantages of low PAPR as well as high data rate, which is an advantage of MIMO.

Different modulation techniques such as QPSK or QAM accommodating number of subcarriers as 1024 or up to 4096 can be experimentally tried to achieve data rates in multiple of 100 Mbps or more.

The new system model can emphasis on performance of Signal to Noise Ratio, Bit Error Rate, CDF and CCDF with respect to channel capacity.

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