# **CDMA Transmitter and Receiver Implementation Using FPGA**

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**Abstract:** Code Division Multiple Access (CDMA) is a spread spectrum technique that uses neither frequency channels nor time slots. With CDMA, the narrow band message (typically digitized voice data) is multiplied by a large bandwidth signal that is a pseudo random noise code (PN code). All users in a CDMA system use the same frequency band and transmit simultaneously. The transmitted signal is recovered by correlating the received signal with the PN code used by the transmitter. The DS - CDMA is expected to be the major medium access technology in the future mobile systems owing to its potential capacity enhancement and the robustness against noise. The CDMA is uniquely featured by its spectrum-spreading randomization process employing a pseudo-noise (PN) sequence, thus is often called the spread spectrum multiple access (SSMA). As different CDMA users take different PN sequences, each CDMA receiver can discriminate and detect its own signal, by regarding the signals transmitter and receiver is implemented in VHDL for FPGA.

Modelsim 6.2(MXE) tool will be used for functional and logic verification at each block. The Xilinx synthesis technology (XST) of Xilinx ISE 9.2i tool will be used for synthesis of transmitter and receiver on FPGA Spartan 3E.

Keywords: CDMA, DSSS, BPSK, GOLD code.

# I. Introduction

Cellular technology has grown tremendously both in terms of traffic and the services it offers. The mobile telecommunication industry facing the problem providing technology that be able to support a variety of services ranging from voice communication with a bit rate of few Kbps to wireless multimedia in which bit rate up to 2 Mbps. This tremendous growth has also been fuelled by the recent improvements in the capacity of wireless links due to the use of multiple access techniques. The idea is to transmit signals simultaneously through a linear band limited channel without inter channel or inter symbol interference. To design multi channel transmission must concentrate on reducing cross talk between adjacent channels. One of the most promising cellular standards is IS-95A code division multiple access (CDMA) system. The advantages Of IS-95A CDMA standard over other standards are optimum subscriber station power management, bandwidth recycling, efficient power control, multilayer diversity and compatibility. The forward link frequency is in the range of (869-894) MHz and reverse link frequency is in the range of (824- 849) MHz In the mobile communication transmission from the base station are on the reverse link.

In the recent years the CDMA on FPGA platform has attracted attention of academic research and industry. The Spartan TM-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically broadband designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates. Because of their exceptionally low cost, Spartan -3E FPGAs are ideally suited to a wide range of consumer electronics applications, including access, home networking, display/projection, and digital television equipment.

# II. Background

Code division multiple access (CDMA) is a channel access method used by various radio communication technologies. It should not be confused with the mobile phone standards called CDMA one, CDMA2000 (the 3G evolution of CDMA one) and WCDMA (the 3G standard used by GSM carriers), which are often referred to as simply CDMA, and use CDMA as an underlying channel access method. One of the concepts in data communication is the idea of allowing several transmitters to send information simultaneously over a single communication channel. This allows several users to share a band of frequencies (see bandwidth). This concept is called multiple accesses. CDMA employs spread-spectrum technology and a special coding scheme (where each transmitter is assigned a code) to allow multiple users to be multiplexed over the same physical channel. By contrast, time division multiple access (TDMA) divides access by time.

# III. Channel Access Method

In telecommunications and computer networks, a channel access method or multiple access method allows several terminals connected to the same multi-point transmission medium to transmit over it and to share its capacity. A channel-access scheme is based on a multiplexing method, that allows several data streams or signals to share the same communication channel or physical medium. Multiplexing is in this context provided by the physical layer. Note that multiplexing also may be used in full-duplex point-to-point communication between nodes in a switched network, which should not be considered as multiple accesses. These are the four fundamental types of channel access schemes:

## A. Frequency Division Multiple Access

The frequency division multiple access (FDMA) channel-access scheme is based on the frequencydivision multiplex (FDM) scheme, which provides different frequency bands to different data-streams. In the FDMA case, the data streams are allocated to different nodes or devices. An example of FDMA systems were the first-generation (1G) cell-phone systems, where each phone call was assigned to a specific uplink frequency channel, and another downlink frequency channel. Each message signal (each phone call) is modulated on a specific carrier frequency. A related technique is wavelength division multiple access (WDMA), based on wavelength division multiplex (WDM), where different data streams get different colors in fiber-optical communications.

## B. Time Division Multiple Access (Tdma)

The time division multiple access (TDMA) channel access scheme is based on the time division multiplex (TDM) scheme, which provides different time-slots to different data-streams (in the TDMA case to different transmitters) in a cyclically repetitive frame structure. For example, node 1 may use time slot 1, node 2 time slot 2, etc. until the last transmitter. Then it starts all over again, in a repetitive pattern, until a connection is ended and that slot becomes free or assigned to another node. An advanced form is Dynamic TDMA (DTDMA), where a scheduling may give different time sometimes but sometimes node 1 may use time slot 1 in first frame and use another time slot in next frame. As an example, 2G cellular systems are based on a combination of TDMA and FDMA.

## C. Packet Mode Multiple-Access

Packet mode multiple-access is typically also based on time-domain multiplexing, but not in a cyclically repetitive frame structure, and therefore it is *not* considered as TDM or TDMA. Due to its random character it can be categorised as statistical multiplexing methods, making it possible to provide dynamic bandwidth allocation. This require a media access control (MAC) protocol, i.e. a principle for the nodes to take turns on the channel and to avoid collisions.

### D. Code Division Multiple Access /Spread Spectrum Multiple Access

The code division multiple access (CDMA) [3] scheme is based on spread spectrum, meaning that a wider radio spectrum in Hertz is used than the data rate of each of the transferred bit streams, and several message signals are transferred simultaneously over the same carrier frequency, utilizing different spreading codes. The wide bandwidth makes it possible to send with a very poor signal-to-noise ratio of much less than 1 (less than 0 dB) according to the Shannon-Heartly formula, meaning that the transmission power can be reduced to a level below the level of the noise and co-channel interference (cross talk) from other message signals sharing the same frequency.



Fig.3. Code division multiple Access (CDMA)

CDMA technology was originally developed by the military during World War II. Researchers were spurred into looking at ways of communicating that would be secure and work in the presence of jamming.

Some of the properties that have made CDMA useful are:

- Anti-jam and interference rejection
- Information security
- Accurate Ranging
- Signal hiding and non-interference with existing systems.
- Low probability of interception

# IV. Spread Spectrum And Its Techniques

Spread spectrum is a means of transmission in which the signal occupies a bandwidth in excess of the minimum necessary to send the information: the band spread is accomplished by means of a code which is independent of the data, and synchronized reception with the code at the receive is used for de-spreading and subsequent data recovery. Two types of spread spectrum techniques are there.

- A. Frequency hopping spread spectrum
- B. Direct sequence spread spectrum

### A. Frequency Hopping Spread Spectrum

The signal is broadcasted over a random series of radio frequencies, hopping from one frequency to another frequency at fixed intervals a receiver, hopping between frequencies in synchronization with the transmitter picks up the message.

## **B.** Direct Sequence Spread Spectrum

Each bit in the original signal is represented by multiple bits in the transmitted signal, using a spreading code. The spreading code spreads the signal across a wider frequency band in direct proportion to the number of bits used.



Fig.4.2. DS System Block Diagram

### V. Ds-Ss Transmitter

In Direct Sequence-Spread Spectrum the baseband waveform is multiplied by the PN sequence. The PN is produced using a PN generator. Frequency of the PN is higher than the Data signal. This generator consists of a shift register, and a logic circuit that determines the PN signal. After spreading, the signal is modulated and transmitted. The most widely modulation scheme is BPSK.



Fig.5.1. DS-SS Transmitter Block Diagram

The PN code used to spread the data can be of two main types. A short PN code (typically 10-128 chips in length) can be used to modulate each data bit. Figure 4 shows the generation of a CDMA signal using a 10-chip length short code. Alternatively a long PN code can be used.



### A. The Pn Generator Design

PN sequences or Pseudo Noise sequence is a periodic binary code which is random in nature generated by the use of shift registers, but generated with taking into considerations some generator polynomials. These properties are known also known as balance property, run property, and correlation property respectively. This code is orthogonal in nature. PN sequence is also known as Maximal Length Sequences.

A PN code is a sequence of chips valued -1 and 1 (polar) or 0 and 1 (non-polar) and has noise-like properties. This results in low cross- correlation values among the codes and the difficulty to jam or detect a data message. A usual way to create a PN code is by means of at least one shift-register. When the length of such a shift-register is n, the following can be said about the period NDS of the above mentioned code-families:





Fig.5.2. PN Generator Block Diagram

### **B. Bpsk Modulator**

The BPSK Modulator is based on the idea of changing the phase of the carrier signal whenever the incoming Bit changes its state, for example, if the incoming message changes its state from 0-1, the carrier changes its phase by  $+180^{\circ}$ , and if it changes its state from 1-0 the carrier changes its phase by  $-180^{\circ}$ .

The BPSK modulator produces the band pass spread spectrum signal which is suitable for transmission from the spreaded signal. The BPSK modulator is implemented using pure digital architecture. The input to the BPSK modulator is the spreaded signal. Spreaded signal is the signal generated by using the PN code and the input data of the CDMA transmitter.



# VI. Ds-Ss Receiver

The CDMA receiver gets its input from the transmitter section and recover the data using matched filter. The matched filter can distinguish the PN sequence and the passes the data to the respective user. We Demodulate the BPSK signal first, Low Pass Filter the signal, and then dispread the filtered signal, to obtain the original message. In the demodulator section, we simply reverse the process. Demodulate the BPSK signal first, Low Pass Filter the signal, to obtain the original message.



Fig.6.1. DS-SS Receiver

## A. Gold Sequence Generator

Length of gold sequence generated is 127 Number of communication links supported is a 63.Correlation property of gold sequences is better than ml sequences and hence they are more preferred. The length of the Gold Sequence is 2<sup>n</sup>-1



Fig.6.2. Gold Sequence Generator

## **B. Bpsk Demodulator**

Digital coherent BPSK demodulator principle is used in this project for receiving the DS-CDMA signals. The BPSK demodulator produce 15 (-7 to 7) digital words, unlike in conventional BPSK demodulator which produces only two symbols ('1' and '0'). This is necessary due to the low power spectral density of DS-CDMA signals and it is only possible to detect the information bits after correlation. This dynamic range of BPSK demodulator can be changed, for a given specification.

# C.Low Pass Filter (Matched Filter)

Matched filter based correlator is used in this project for receiving the DS-CDMA signals. The correlator accepts the 128 demodulator outputs and multiplies with 128 length PN sequence which is a sequence of +1 and -1. The outputs of multipliers are accumulated to produce the correlator output. The magnitude of the correlator output peaks whenever exact match occurs between the PN sequence and BPSK demodulator outputs. The output of the matched filter is given to the threshold detector, for detecting the information bits.

# VII. Design And Implementation

# A. Design Of Cdma Transmitter

### And Receiver

The design and implementation of the CDMA transmitter and receiver considers the following specifications

1. Type of PN Sequence: Gold Code

2. LFSR Size: Two 7 bit LFSRs in case of Gold Sequence 3. PN Sequence Length: 127 in case of gold sequence 4. Maximum no. of communication Links: 63 in case of gold sequence

- 5. Type of Modulation : BPSK

6. Type of demodulation : Coherent BPSK demodulation 7. Type of Correlator : Matched Filter

8. Type of Signal Synthesis: LUT based direct digital fequency

9. Phase Resolution Chosen in DDFS: 5.625

10. Threshold Type adjustable: Constant Threshold value 11. Front end Design Entry : VHDL

12. Backed Synthesis : Xilinx Spartan 3E FPGA

# **C**. Vhdl Implementation Of Cdma

### **Transmitter And Receiver**

A VHDL specification can be executed in order to achieve high level of confidence in its correctness before commencing design and may simulate one to two orders of magnitude faster than a gate level description.

Following tools are used while developing, testing, implementing and programming the CDMA transmitter and receiver blocks. Simulation - Modelsim Xilinx Edition (MXE) Synthesis - Xilinx Synthesis Technology (XST) of Xilinx ISE

# VIII. Results

A.Simulation Results Simulation result for DS CDMA Transmitter



Fig.8.3. Simulation result for DS CDMA Transmitter.

The above simulation result shows the DS CDMA transmitter tested with inputs user\_key, user\_data, pn\_seq and output observed is out\_ss\_signal.

# Simulation result for DS CDMA demodulator

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💠 ss_signal_ck	0	П	ЛГ	ш	П	Л	П	пл
	000000							
demod_out_value	7	17	(7	):7	)7	(.7		7
demod_out_bit	1							
Internation of the second seco	0							
💽 🔷 phase_inc_word	000001							

Fig.8.4. Simulation result for DS CDMA demodulator.

The above simulation result shows the demodulator output which is scaled to 4 bits. In the above figure demodulated output which is scaled to 4 bits can be seen at demod\_out\_value. The values lie in the range of -7 and +7. This is obtained by right shift by nine places and then truncating to 4 bits. This is sent as input to serial to parallel convertor.

# **B.** Synthesis Results

The Floorplan for transmitter on Spartan-3E FPGA is given in the below figure.



Fig.8.5. Floor plan for transmitter block

The Floorplan for receiver on Spartan-3E FPGA is given in the below figure.



Fig.8.6. Floor plan for receiver on Spartan-3E FPGA

## C. Chipscope Results Chipscope Pro Analyzer DS CDMA Top Level Module

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- UNIT:0 MyILA0 (ILA) - Trigger Setup	← out_SS_signal	29	29	31	21	( 0	( -22	30	) 19	) -4	(-24	) - <u>31</u>	·20	3
– Waveform – Listing	— userdata	0	(											
- Bus Plot	- rx_out_bit	0	0											
DEV:1 MyDevice1 (XCFD4S)	— clk	1	1											

Fig.8.7. Chipscope Pro Analyzer DS CDMA Top Level Module.

The above chipscope output shows the transmitted signal which is out\_ss\_signal.It can be observed that data bit and the rx\_out\_bit user are equal.

## IX. Conclusion

In the proposed Project I have implemented various modules of Direct Sequence Code Multiple Access Communication System. It has been observed that the implemented design is fully reconfigurable on any communication links. System developed is implemented with 127 gold code sequence, it can be implemented with any length sequence very easily.

The developed DS CDMA system provides efficient area utilization on FPGA. This is obtained by implementing scaling process in receiver section. Chipscope analysis which provides testing and on chip debug at runtime is also implemented and the results obtained are satisfactory. This work has the following applications.

□ Custom CDMA communication setup with specified

PN sequence length and number of users

□ Standard CDMA systems designs such as used for mobiles and GPS

for mobiles and Of 5

Implementation of a CDMA communication system with

DSSS technique in VHDL has the following advantages

□ The design is fully reconfigurable

 $\hfill\square$  The number of bits and PN sequence can be

changed very easily

□ Useful for both FPGA and ASIC implementations.

Disadvantages

□ Complex hardware is involved in receiver design

which increases the cost of the system

# X. Future Scope

The proposed project can be further extended to implement with multiple transmitters and receiver's .It can be implemented with different modulation techniques and a comparative analysis can also be made. Various techniques can also be implemented to improve the multipath interference effect.

The concept can be extended to design the Global Positioning System which is CDMA system. Frequency hopping spread spectrum technique can also be implemented and compared.

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