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Design of Anti-collision Technique for RFID UHF Tag using Verilog

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***Abstract**: This paper presents a proposed Reliable and Cost Effective Anti-collision technique (RCEAT) for Radio Frequency Identification (RFID) Class 0 UHF tag. The RCEAT architecture consists of two main subsystems; PreRCEAT and PostRCEAT. The PreRCEAT subsystem is to detect any error in the incoming messages. Then the identification bit (ID) of the no error packet will be fed to the next subsystem. The PostRCEAT subsystem is to identify the tag by using the proposed Fast-search Lookup Table. The proposed system is designed using Verilog HDL. The system has been successfully implemented in hardware using Field Programmable Grid Array (FPGA) SPARTAN 3E. Finally the RCEAT architecture is synthesized using xillins 13.3v. From the hardware verification results, it shows that the proposed RCEAT system enables to identify the tags without error at the maximum operating frequency of 180MHz. The system consumes 7.578 mW powers, occupies 6,041 gates and 0.0375 mm^2 area with Data arrival time of 2.31 ns.*
***Key words:** FPGA,Spartan 3e,RCEAT,Verilog HDL,RFID tag,CRC.*

I. Introduction

In the data management system a significant role of the Data link layer is to convert the unreliable physical link between reader and tag into a reliable link. Therefore, the RFID system employs the *Cyclic Redundancy Check* (CRC) as an error detection scheme. The CRC calculation consists of an iterative process involving Exclusive-ORs and shift register which is executed much faster in hardware compare in software [9].

In addition for reader to communicate with the multiple tags, an anti -collision technique is required. A significant advantage of RFID devices over the others identification devices is that the RFID device does not need to be positioned precisely relative tothe scanner. As credit cards and ATM cards must be swiped through a special reader. In contrast, RFID devices will work within a few feet (up to 20 feet for high-frequency devices) of the scanner. But theproblem associated with this technique is thecollision of tags. So inorder to avoid coliision of tags a technique has been proposed which is both reliable and also cost effective. And so call this technique as RECEAT. This proposed technique doesnot require the tag to remember the instructions fromthe reader during the identification process. Thus thetag is treated as an address carrying device only andmemory-less tag can be designed which requires very low power.Some common problems with RFID are reader collision and tag collision. Reader collisionoccurs when the signals from two or more readers overlap. The tag is unable to respond to simultaneous
queries. Systems must be carefully set up to avoid this problem. Tag collision occurs when many tags are present in a small area; but since the read time is very fast, it is easier for vendors to develop systems that ensure that tags respond one at a time.

The tag collision can be eliminated using differenttechniques. They are mainly of two types: a) TreeBased Algorithms and ALOHA based algorithms.Where Tree based algorithms consists of Binary treealgorithms and Query tree. Whereas the ALOHAbased algorithms are classified into ALOHA, SlottedALOHA and Frame Slotted ALOHA. Somehardware's also designed for this purpose. Here inthis paper Tree algorithms have been considered withFast Search Algorithm.

II. Methodology

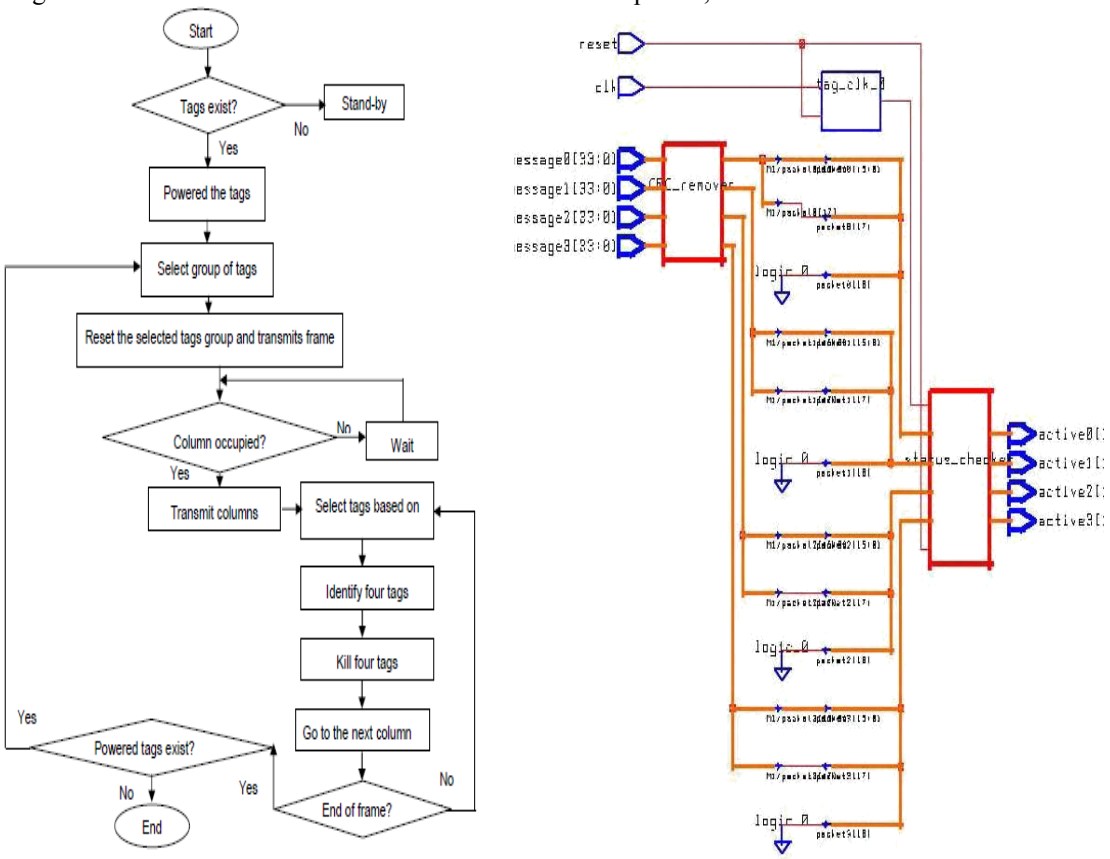
In our proposed RCEAT the frame consists of slots and each slot (column) is divided into four minislots (rows). Therefore in each slot, four tags are allowed for contending the minislots. The RCEAT will identify these four tags using the proposed Lookup table.The uniqueness of this proposed technique is reducing the tag identification time in the Binary Tree.The existing tags are divided into four in each Read cycle to reduce the required iterations and thus faster the tag identification. This proposed technique does not require the tag to remember the instructions from the reader during the identification process. Thus the tag is treated as an address carrying device only and memory-less tag can be designed which requires very low power. The RCEAT identification methodology is shown in Fig. 1. In RCEAT, bidirectional communications are involved, from the reader to the tag (Downlink) and from the tag to the reader (Uplink). When the reader detects there are tags exist in its interrogation zone, it will power these tags. Then the reader sends the Select-group command based on the tag Prefix or Object Class (OC). The selected tags group will move to the Ready state. Next the Reader

transmits Reset signals and its frame. After that the frame is transmitted back to the reader, column by column starting with the first column. This compensates the time required for transmitting the packet to the reader. Therefore for every Read cycle, there are always available packets at the reader waiting for identification.

At the reader, the incoming packets for each link sequentially enter the RCEAT system. To avoid the four incoming packets from colliding with each other, these packets (IDs) are identified using the Binary Tree based technique with maximum four leaves. The reader selects these IDs using the proposed Fast-search Lookup table, and then the selected ID will be identified. Based on this proposed Lookup table, the four IDs will be identified from the smallest value to the largest one in one Readcycle. Then the tag that has successfully identified will be acknowledged by sending the Kill-tag.

III. Architecture

The RCEAT architecture consists of two subsystem; PreRCEAT and PostRCEAT. In the PreRCEAT, the received messages are fed into the CRC-remover module. These received messages will be separated into two; the received packet and the received CRC. These packet and CRC are sent to the CRC-checker module for verification process. The CRC-checker module recalculated the CRC of the received packet. Then, this calculated CRC is compared with the received CRC.If the values are same, means no error, the status-bit is set to its original value i.e. zero. Otherwise or there are errors in the packet, the status-bit is set to two.



After that, this updated status-bit is appended to its respective packet. Finally, the packet with the updated status-bit is fed to the Status-checker module. The Status-checker module will check any errors in the incoming packets. If there are errors, then reset the slot of the respective packet to zero value. Otherwise, fill the slot of the packet with its respective ID. The status-bit is removed from its packet and onlythe tag's ID will be output to the PostRCEAT [8].

In the PostRCEAT, the active tags are divided into a group of four for every Read cycle in order to reduce the number of iterations in the identification process. The PostRCEAT reads all the ID bits at once regardless of its length. This is performed by using the word-by- word multiplexing. During the identification process, the Fast-search module identifies the four tag's IDs simultaneously in one Read cycle which equal to a Tag clock cycle. The module firstly identifies the smallest ID bits until the largest one follows the Binary Tree with a maximum number of four leaves.

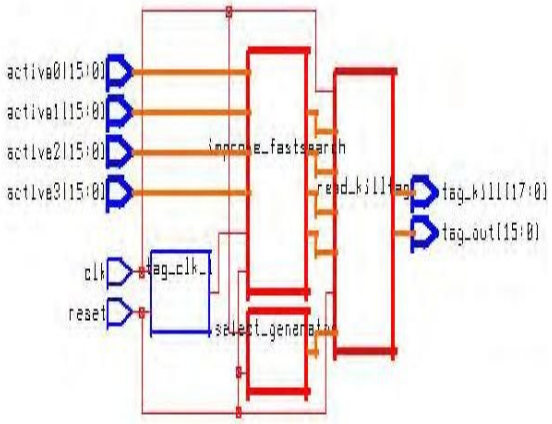


Figure1: Pre RCEAT and Post RCEAT

IV. Simulation results

Verilog HDL codes for the RCEAT architecture have been successfully simulated and verified using the ModelSim XE II/Starter 5.7g tool. The following will discuss the Behavioral simulation waveforms for the selected ports in the RCEAT system as shown in Fig. 2. At the first Read cycle, for the received messages of $000C85844_{16}$, $0000550A5_{16}$, 000101231_{16}, and $0EA6093DF_{16}$, the recalculated CRC of these messages are 5844_{16}, $50A5_{16}$, 1231_{16}, and $93DF_{16}$ respectively. As a result, the calculated CRCs are equal to the received CRCs which are represented by the four bit of the least significant bit (LSB) of the messages. Since there are no errors in the received messages, the Status-bit of the packets are set to zero, which are represented by the MSB of the packets; $000C8_{16}$, 00005_{16}, 00010_{16} and $0EA60_{16}$ respectively. Finally, the ID of these packets will be fed simultaneously to the PostRCEAT subsystem.

In the PostRCEAT subsystem, the Fast-search module will identify the four active tags simultaneously starting from the smallest value to the largest one. For examples, for the four input tag's ID of $00C8_{16}$, 0005_{16}, 0010_{16} and $EA60_{16}$ will be identified as 0005_{16}, 0010_{16}, $00C8_{16}$ and $EA60_{16}$ respectively. Then these identified tags will be fed to the Read-killtag module simultaneously at the negative edge of the Tag clock. Finally, the Read-killtag Module will output the four identified tags serially, one tag at every cycle of the system clock starting from the smallest tag's ID to the largest one. Moreover, at the same clock cycle, the identified tag will be killed.

The RCEAT system has been successfully implemented in hardware using FPGA with desired performances.

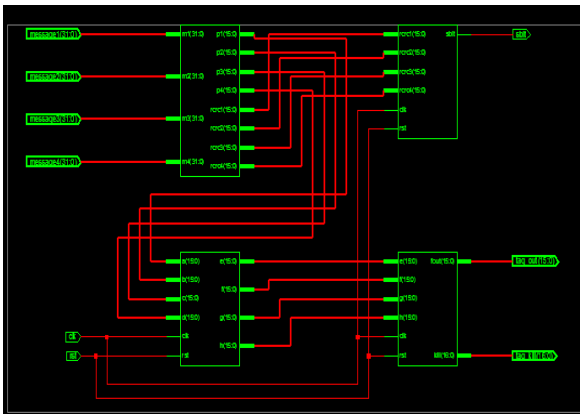


Fig: RTL Schematic

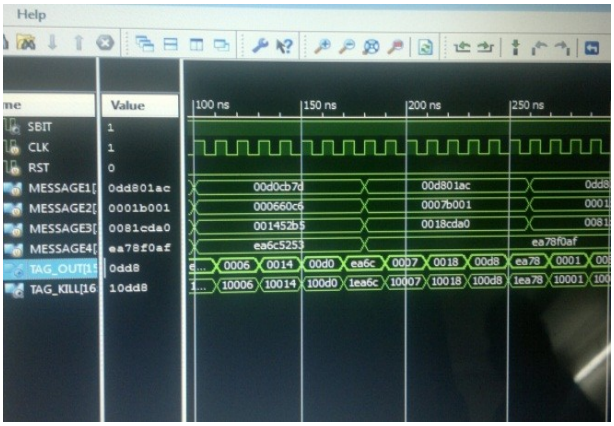


Figure2: Simulated in Xilinx's

Synthesis Report

Number of Slices: 209 out of 4656 4%
Number of Slice Flip Flops: 31 out of 9312 0%
Number of 4 input LUTs: 388 out of 9312 4%
Number of IOs: 164
Number of bonded IOBs: 100 out of 232 43%
Number of GCLKs: 1 out of 24 4%
Minimum period: 5.003ns (Maximum Frequency: 199.880MHz)
Minimum input arrival time before clock: 26.497ns
Maximum output required time after clock: 4.394ns

V. Conclusions

A proposed Reliable and Cost Effective Anti-collision technique (RCEAT) is designed to achieve a reliable and cost effective identification technique of the tag. The RCEAT architecture consists of two main subsystems; PreRCEAT checks error in the incoming packets using the CRC scheme. PostRCEAT identifies the error free packets using Binary Tree based technique. The architecture has been synthesized using Xilinx Technology. The RCEAT architecture also has been successfully implemented in hardware using FPGA. The result shows that the architecture has smaller cell area, power consumption and number of gates. Therefore minimize the implementation and operating costs.

RCEAT is designed toachieve a reliable and cost effective identificationtechnique of the tag. The RCEAT architectureconsists of two main subsystems; PreRCEAT checkserror in the incoming packets using the CRC scheme.PostRCEAT identifies the error free packets usingBinary Tree based technique. The architecture hasbeen synthesized using Xilinx Synthesis Technology(XST)

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