Design a Low Power High Speed Full Adder Using AVL Technique Based on CMOS Nano-Technology

Devendra Kumar Gautam[1], Dr. S R P Sinha[2], Er. Yogesh Kumar Verma[3]

M.Tech Student[1], Associate Professor[2], Research Scholar[3]
Department of Electronics and Communication Engineering
Institute of Engineering & Technology[1,2], Madan Mohan Malaviya Engineering College[3]
Uttar Pradesh, INDIA

Abstract: *Power and delay optimization is a very crucial issue in low voltage applications. In this paper, we present a design of Full Adder circuit using AVL techniques for low power operation. The approach for the design is based on XOR/XNOR & Transmission gate for single bit as hybrid design .By using this approach Full Adder is being designed using 12 transistors. We can reduce the value of total power dissipation by applying the AVLG (adaptive voltage level at ground) technology in which the ground potential is raised and AVLS (adaptive voltage level at supply) in which supply potential is increased. The main aim of the design is to investigate the power, Propagation Delay and Power delay Product for low voltage Full Adder for the proposed design style. The simulation results show that there is a significant reduction in power consumption for this proposed cell with the AVL technique. The circuit is designed using 65 nanometer CMOS technology and simulated using MicroWind and DSCH Ver. 3.1*
Keywords: *Full Adder, AVL Techniques, Low Power, VLSI, High Performance*

I. Introduction

Full adder is the simplest combinational circuit which performs the arithmetic addition of three binary digits. This is the necessory building block for designing a VLSI system. Figure 1.1 shows the logic Symbol of Full adder. In the figure, three inputs are present ,where A represents Augend, B represents Addend and C_{in} represents Carry input. The two outputs are the SUM(S) of A ,B & C_{in} and CARRY out bit denoted by C_{out}. Figure1.2 shows the logic diagram of Full adder. Table 1.1 represents Truth Table of Full adder. It is clear from table that the SUM output is 1 when either of inputs (A or B or C_{in}) is 1 and all of these inputs are 1. Carry output is 1 when any of two inputs (A, B or B, C_{in} or C_{in}, A) are 1 and all of these inputs are 1.
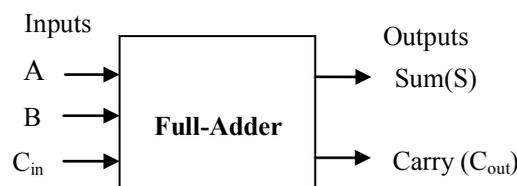
Figure.1.1: Logic Symbol of Full Adder
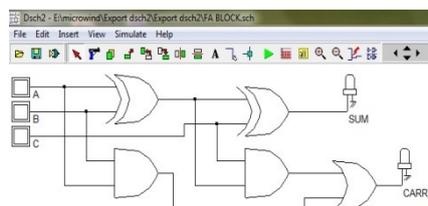
Figure.1.2: Logic Diagram of Full Adder

From table 1.1, the logic expression for Sum output can be written as a Sum of Product expression by summing up the input combinations for which the sum is equal to 1.

$$S = \overline{A}\ \overline{B}\ C_{in} + \overline{A}\ B\ \overline{C}_{in} + A\ \overline{B}\ \overline{C}_{in} + A\ B\ C_{in}$$

Now, this expression can be simplified as :

$$S = A \oplus B \oplus C_{in}$$

Table 1.1: Truth Table of Full Adder

Inputs			Outputs	
Augend bit A	Addend bit B	Carry input C_{in}	Sum S	Carry C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Similarly, the logic expression for carry output can be expressed as a Sum of Product expression by summing up the input combinations for which the carry is equal to 1.
Therefore,

$$C_{out} = A\,B + B\,C_{in} + C_{in}\,A$$

The sum output corresponds to a logic Ex-OR function while the carry output corresponds to an AND function. So that Full adder circuit can be implemented using Ex-OR and AND gates as shown in Figure 1.2. The main aim to realize a circuit required Low power [1, 2] and high performance [3].

II.   Related Work regarding Full Adder Reliazation

There are many papers that have published for the optimisation of Full Adder for Low power. Those are based on different methodologies for Logic design style. These are Centralised XOR/XOR ,Centralised XOR/XNOR[6] ,Complementry Pass Transistor design style, Transmission Gate design style ,Hybrid CMOS design[9] ,Bridge design style [1] and many more. In which various parameters like Power consumption, Propagation Delay, Layout area are being taken into consideration.The main aim of all those design style is to reduce the power consumption as much as possible.

The proposed designing of Full Adder uses XOR/XNOR & Transmission Gate or called a hybrid design[5,10] for the implementation using AVL techniques. By using AVL techniques, there is large reduction in the power consumption & propagation delay as compare to other conventional design.

III.   Proposed Full Adder Design Style

In the proposed design of Full Adder, we are going to design the circuit via XOR/XNOR[6] & Transmission Gate design style as hybrid design[4] and introduce this conventional design with AVL techniques. On the variation in technology scaling [8] ,it introduce the variation in parameters values. As technology is reducing more & more than desired system would be suitable for low power [2, 4] and high performance. In these AVL techniques such as via AVLG (adaptive voltage level at ground) technique in which the ground potential is raised and AVLS (adaptive voltage level at supply) technique in which supply potential is increased.

In this design total 12 transistors are required for the operation of Full Adder[9]. So that as compare to other design style the proposed design style use less No. of transistors, less Layout area, higher performance and less PDP . So that this design style make the Full Adder more efficient .The most affected design is via AVLS technique. The various design styles that we introduce for design the system are as follows.

3.1   C-CMOS implementation of Full-Adder

In this C-CMOS (Complementary CMOS) design style [1], the CARRY is generated through a single static CMOS gate at the source & drain terminals of transistors T11 & T12 respectively. The circuit diagram for this design is shown in Figure 3.1.1.
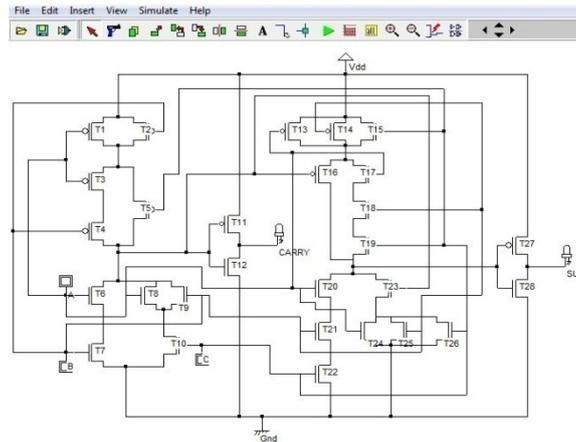
Figure 3.1.1: Circuit diagram of Full Adder using C-CMOS
design style
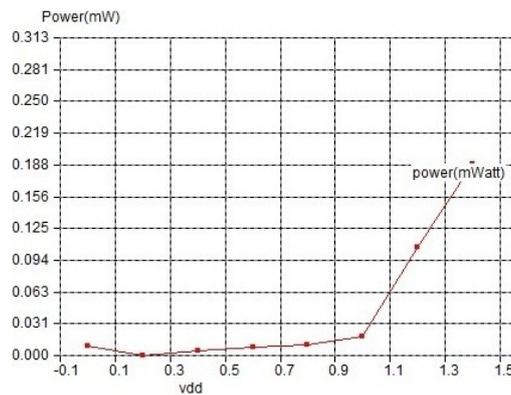
Figure 3.1.2: Variation of power Vs Supply voltage
under C-CMOS design style

This model is designed using 28 No. of transistors. In the design, carry is propagated for the generation of SUM. This design having lots of disadvantages such as power consumption & delay is more. Also routed wires and layout area is more .So that this design widely not used due to complex structure. Variation of Power Vs supply voltage is shown in figure 3.1.2. Simulation result is shown in figure 4.1.

3.2 Conventional Design of Full Adder
In this conventional design style, Full adder circuit is designed via XOR & transmission gate. Here, Sum is generated at the source & drain terminals of transistors T7 & T8 respectively via XOR gate. Carry is generated via transmission gate.
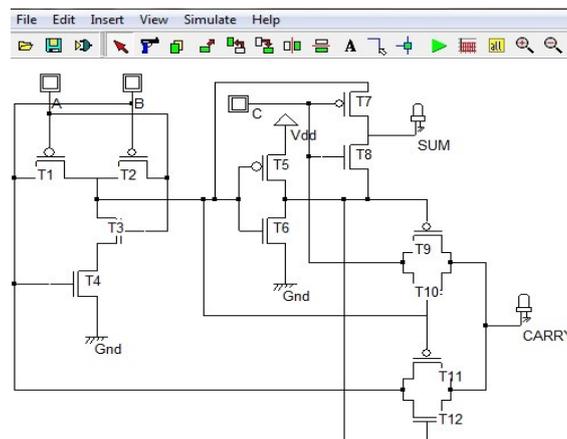
Figure 3.2.1: Circuit diagram of conventional Full Adder
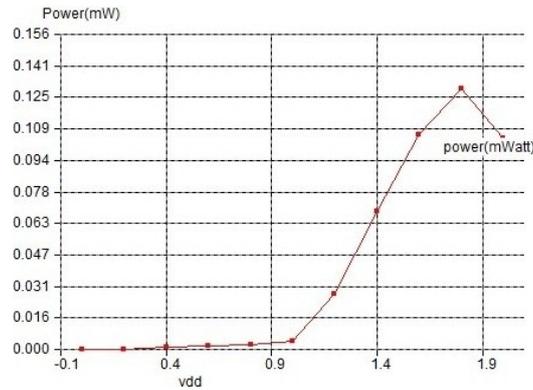
Figure 3.2.2: Variation of power Vs Supply voltage
under conventional design style

This design required only 12 No. of transistors which is less than half of transistors required in C-CMOS design. The circuit diagram of conventional Full Adder is shown in figure 3.2. As technology is scaled down to 65 nm technology [7, 8].Various Changes in parameters can occur, than desired system would be suitable for low power. Variation of Power Vs supply voltage is shown in figure 3.2.2. Several parameters included in the design such layout area, complied cells, power consumption, PDP and propagation delay reduced too much as compare to C-CMOS. Simulation result is shown in figure 4.2.

3.3   Design of Full Adder using AVL Technique
An adaptive voltage level technique[11] can be used to control circuits and it can be used either at the upper end of the cell to bring down the supply voltage value, called AVLS scheme or at the lower end of the cell to lift the potential of the ground node, called AVLG scheme.

3.3.1   AVLG Technique:
In AVLG technique, a combination of N-MOS & P-MOS are connected in parallel. So that an input clock pulse is applied at the N-MOS of circuit of AVLG and rest of all P-MOS are connected to ground. This AVLG circuit is connected at the ground terminal of conventional one by removing ground. Table 3.3.1 shows the working operation of Full adder via AVLG technique. As an increase in ground voltage, there will be a reduction in V_{GS} & V_{GD} of transistor T7 & T8 respectively. The clock pulse is applied at the gate terminal of transistor T13 so that transistor T13 becomes ON and Transistors T14 & T15 becomes OFF.
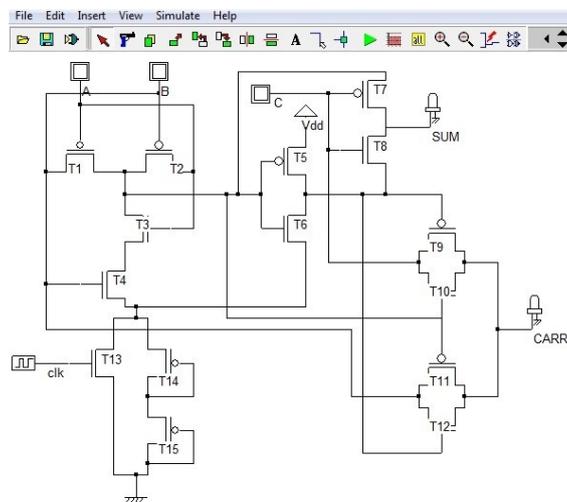
Figure 3.3.1.1: Circuit diagram of Full Adder incorporated with
AVLG technique

The leakage current flowing via transistor T13 is reduced thus the power consumption is reduced through transistor T13. Simulation result is shown in figure 4.3.

Table 3.3.1: Truth Table of Full Adder incorporated with
AVLG technique

Inputs			Outputs	
Augend bit A	Addend bit B	Carry input C_{in}	Sum S	Carry C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	X	X
1	0	0	X	0
1	0	1	0	1
1	1	0	`0	1
1	1	1	X	1
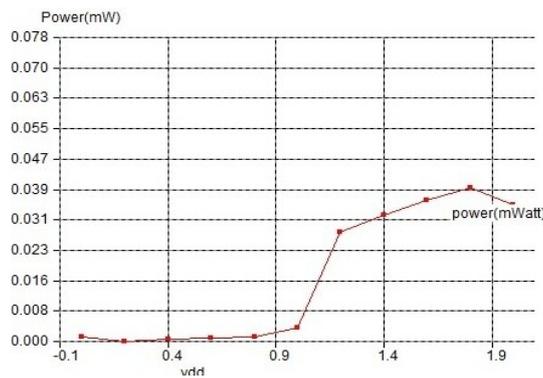
Figure 3.3.1.2: Variation of Power Vs Supply voltage
under AVLG design style

Figure 3.3.1.1 shows circuit diagram of Full Adder incorporated with AVLG Technique. Variation of Power Vs supply voltage is shown in figure 3.3.1.2

3.3.2   AVLS Technique

In AVLS technique, a combination of N-MOS & P-MOS are connected in parallel. So that a input clock pulse is applied at the P-MOS of circuit of AVLS and rest of all N-MOS are connected to drain terminal with supply voltage. Table 3.3.2 shows the working operation of Full adder via AVLS technique**.** The drain terminal of transistor T5 is connected at supply voltage and it becomes ON. A decrease in V_{GS} is observed in transistor T5.
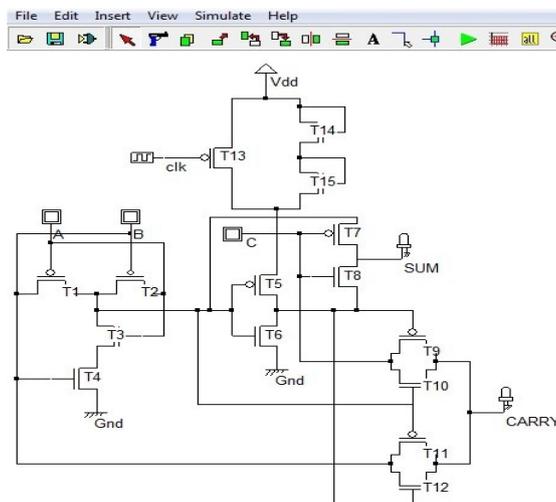
Figure 3.3.2.1: Circuit diagram of Full Adder incorporated with
AVLS technique

As clock pulse is applied at gate terminal of transistor T13, This transistor becomes ON and transistors T14 & T15 becomes OFF. Due to this a loss in power reduction is observed in transistors T5 & T7.

Table 3.3.2: Truth Table of Full Adder incorporated with AVLS technique

Inputs			Outputs	
Augend bit A	Addend bit B	Carry input C_{in}	Sum S	Carry C_{out}
0	0	0	0	0
0	0	1	X	0
0	1	0	1	X
0	1	1	0	1
1	0	0	1	0
1	0	1	X	1
1	1	0	X	X
1	1	1	1	1

The circuit diagram is shown in Figure 3.3.2.2. Transistor T13 is the major source of power reduction [5] in complete circuit.
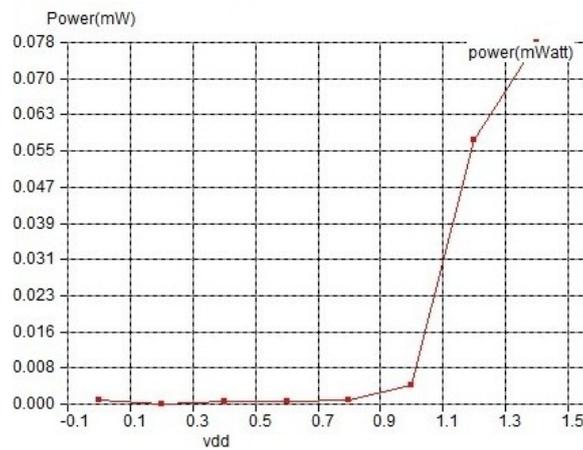
Figure 3.3.2.2: Variation of power Vs Supply voltage
under AVLS design style

Simulation result is shown in figure 4.4 .It is clear that the most power reduction is observed in this AVLS technique. So that the system designed using this modeling style is mostly preferred in any aspect.

IV.   Simulation Results

The simulation is performed using Microwind & DSCH 3.1 tool. The result of proposed hybrid design [5] is being shown in respective figures with average power consumption & Delay below for the different design style of Full Adder at 0.8 V V_{DD}. Figure 4.1 shows Simulation Waveform of C-CMOS Full Adder. Figure 4.2 shows Simulation Waveform of Conventional Full Adder.
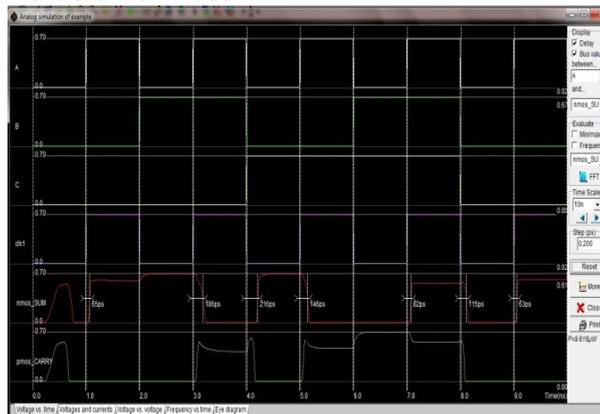
Figure 4.1: Simulation Waveform of C-CMOS Full Adder
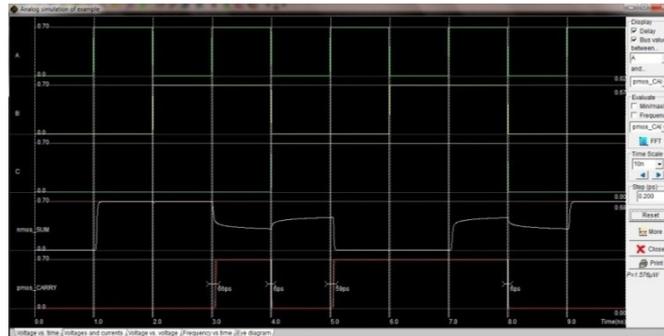
Figure 4.2: Simulation Waveform of Conventional Full Adder
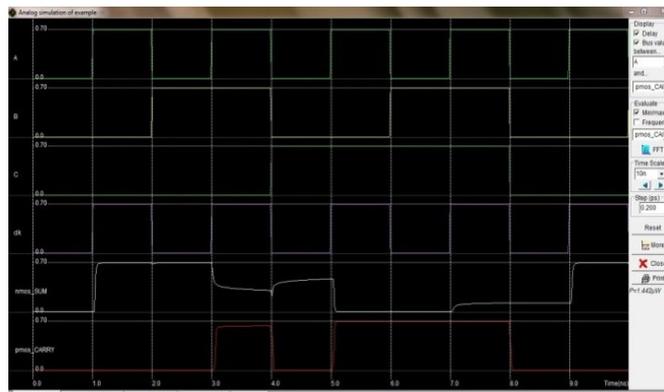
Figure 4.3: Simulation Waveform of Full Adder incorporated
with AVLG Technique
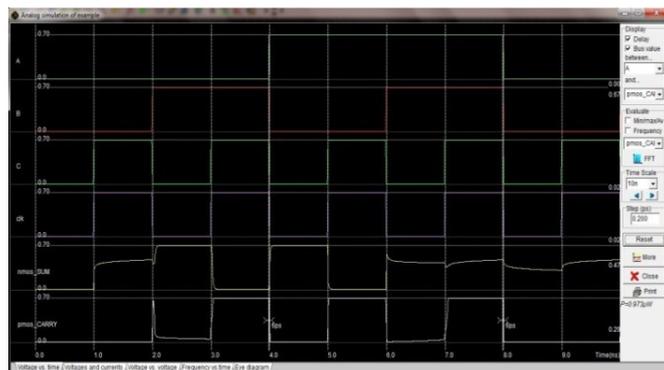
Figure 4.4: Simulation Waveform of Full Adder incorporated
with AVLS Technique

Figure 4.3 shows Simulation Waveform of Full Adder incorporated with AVLG Technique. Figure 4.4 shows Simulation Waveform of Full Adder incorporated with AVLS Technique. The results are compared with others design style. From the result, it is clear that proposed design provide the best performance.

V. Conclusion

The Simulation results clearly explain the reduction in the power consumption by incorporated with AVL Technique that is either AVLG or AVLS Technique. Table 5.1 shows the comparison results among the various design style such as : Conventional , C-CMOS , AVLG & AVLS using 65 nm CMOS Technology. The circuit implemented using AVLS technique gives us the appropriate result among various parameters and helping in obtaining an optimum Full Adder circuit. On designing AVLS technique based Full adder, we obtain a very low power consumption circuit, less propagation delay and also less PDP as compared to other design style. Thus this design is suitable for Low power applications. But the main disadvantage of this design is that it required more routed wire & layout area as compare to AVLG & conventional design. The proposed design gives the best power consumption with all the others.

Table 5.1: Comparison analysis of Full Adder among various designs
Style & various CMOS parameters with 65 nm technology

S. No.	Parameters	C-CMOS	Conventional	AVLG	AVLS
1.	Power Consumption(μw)	9.225	1.576	1.442	0.973
2.	Routed Wires	92	47	57	55
3.	Compiled Cells	28 / 28	12 / 12	15 /15	15 / 15
4.	Layout Area (μm^2)	450	176	224	216
5.	Propagation Delay (ns)	0.089	0.036	0.047	0.031
6.	PDP (fj)	0.821	0.0567	0.0677	0.030
7.	No. of N-MOS and P-MOS transistors	14 , 14	6 , 6	7 , 8	8 , 7

References:

[1]. S. Wariya, Himanshu Pandey, R. K. Nagaria and S. Tiwari ,(2010)"Ultra low voltage high speed 1bit adder," IEEE Transactions Very Large Scale Integeration.

[2]. Shamima Khatoon (2012)"A novel design for highly compact low power area efficient 1-bit Full Adders" ,IJAET

[3]. Keivan Navi and Omid Kavehei(2008)"Low-Power and High-Performance 1-Bit CMOS Full-Adder Cell" JOURNAL OF COMPUTERS, VOL. 3, NO. 2, FEBRUARY 2008

[4]. Praveer saxena, Dinesh Chandra, sampath kumar V(2011) "Design of 1-Bit Full Adder for Low Power Applications" IJAEST,Vol No. 10 Issue No.1,019-025

[5]. Amit gupta, R K Sharma ,Rasika Dhavse, "Low power High speed small area Hybrid CMOS Full Adder"2012/2/1/41/93212

[6]. Subodh Wairya[1], Rajendra Kumar Nagaria[2], and Sudarshan Tiwari[3], "Comparative Performance Analysis of XORXNOR Function Based High-Speed CMOS Full Adder Circuits For Low Voltage",VLSI Design International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.2, April 2012

[7]. V. Vijay1, J. Prathiba2, S. Niranjan Reddy3 and P. Praveen kumar4 (2012) "A REVIEW OF THE 0.09 um STANDARD FULL ADDERS" (VLSICS) Vol.3, No.3, June 2012.

[8]. Farshad Moradi, Dag T. Wisland, Ali Peiravi , Hamid Mahmoodi (2008)"1-Bit Sub Threshold Full Adders in 65nm CMOS Technology" International conference on Microelectronics 1-4244-2370-5/08/$20.00 ©2008 IEEE

[9]. Subodh Wairya[1], Rajendra Kumar Nagaria[2], Sudarshan Tiwari[3] "New design methodologies for Highspeed mixed-mode CMOS Full adder circuits" International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.2, June 2011 DOI : 10.5121/vlsic.2011.2207 78

[10]. Keivan Navi ,Mohammad Reza Saatchi, Omid Daei(2009) "A High-Speed Hybrid Full Adder"EJSR, ISSN 1450-216X Vol.26 No.1 (2009), pp.29-33

[11]. Tanvi Sood1, Rajesh Mehra2 "Design a Low Power Half-Subtractor Using .90µm CMOS Technology "(2013) IOSR-JVSP Volume 2, Issue 3, PP 51-56 e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197

Biography

Dr. S R P Sinha born on 13 May 1958 received his B.Tech. Degree from University of Ranchi in 1981, M.Tech. Degree from University of Roorkee in 1984 and Ph.D from University of Lucknow in 2004. His research interest includes Electronic Devices and Micro-Electronics. He is currently working as Associate Professor in Electronics & Communication Engineering Department in Institute of Engineering & Technology Lucknow from 26 September 2011.

Er. Yogesh Kumar Verma born on 25 June 1988 received his B.Tech. Degree in Electronics and Communication Engineering from Sharda Group of Institutions, Mathura in 2009 and M.Tech. Degree in Electronics and Communication Engineering with specialization in Digital Systems from Madan Mohan Malaviya Engineering College, Gorakhpur in 2012. His research interest includes Device modeling in general and Modeling and Simulation of HBT based devices in particular. His area of interest also includes analysis of Mixed Signal Circuits and Integrated Circuits. He is currently working as Assistant Professor in Electronics and Communication Engineering Department in Noida Institute of Engineering and Technology, Greater Noida.

Devendra Kumar Gautam born on 19 December 1989 received his B.Tech. Degree in Electronics and Communication Engineering from Shardha Group of Institutions Mathura in 2010 and he is currently pursuing M.Tech. in Microelectronics from Institute of Engineering & Technology , Lucknow . His research interest includes Low Power VLSI Design & Analog CMOS Design.