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Comparative Study of High performance Braun's Multiplier using FPGAs

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Abstract: Multiplication is one of the essential operations in Digital Signal Processing (DSP) applications like Fast Fourier Transform (FFT), Digital filters etc. With the advancements in technology, research is still going on to design a multiplier that consumes less power or has high speed or occupies less area or a combination of these in a single multiplier. This makes the multipliers to be used for high speed or low power VLSI applications. The Braun's multiplier is one of the parallel array multiplier which is used for unsigned numbers multiplication. The dynamic power of the multiplier can be reduced by using the bypassing techniques. The delay can be reduced by replacing the ripple carry adder in the last stage by fast adders like Carry look ahead adder and Kogge stone adder. This paper presents a comparative study among different types of bypassing multipliers for 4*4, 8*8 and 16*16 bits and their architectural modifications using different FPGAs like Spartan – 3E, Virtex – 4, Virtex – 5 and Virtex – 6 Lower power using Xilinx 13.2 ISE tool from which we get the delay and the dynamic power and cell area reports are obtained using RTL Compiler from Cadence in 90 nm technology.

Keywords: Field Programmable Gate Array (FPGA), Bypassing Techniques, Digital Signal Processing, Multipliers, Carry Look Ahead adder, Kogge stone adder

I. INTRODUCTION

In order to achieve the high speed and low power demand in DSP applications, parallel array multipliers are widely used. One such widely used parallel array multiplier is the Braun's multiplier. The Braun's multiplier is generally called as the Carry Save Array Multiplier. The architecture of a Braun's multiplier consists of AND gates and full adders. All the architecture implementations demand using ASICs but the cost of development of ASICs is high. So the algorithms must be verified thoroughly before implementing them. FPGA overcomes these disadvantages because of the advantages like high speed of hardware, parallelism and the software flexibility. Also, ASICs are meant only for a particular design but FPGAs can be reprogrammed.

In DSP applications, most of the power is consumed by the multipliers. Hence, low power multipliers must be designed in order to reduce the power dissipation in DSP applications. The power dissipation in CMOS circuits is mainly due to the static power dissipation and the dynamic power dissipation. The power dissipation in CMOS circuits is given by,

$$P = (1/2)*C*V^2*f*N,$$

where, P is the power dissipation, C is the load capacitance, V is the supply voltage, f is the frequency of the clock and N is the total number of switching activities in one clock cycle. Dynamic power is due to the switching activities. So, by reducing the switching activity the dynamic power can be reduced. In this low power multiplier design domain, many papers have been published to reduce the switching activity [7] and also to reduce the power dissipation by bypassing techniques.

In this paper, techniques to further reduce the delay and power are proposed by making modifications to the adders since adders are one of the major building blocks in multiplier designs. Compared with the conventional multipliers, the modified multipliers have an improved performance in terms of delay and power.

II. PREVIOUS WORK AND RELATED RESEARCH

The architecture of a 4*4 Standard Braun multiplier is as shown in Fig.:1. In general, for an n*n Braun multiplier, there will be n(n-1) number of full adders and n^2 AND gates. One of the major disadvantages of the Braun's multiplier is that the number of components required increases quadratically with the number of bits which will make the multiplier to be inefficient. The delay of the Braun's multiplier depends on the delay of the full adders and also on the delay of the final adder in the last stage.

The dynamic power can be reduced by using the bypassing techniques. In Row Bypassing multiplier [2], if the multiplier bit b_j is zero, then the addition operations in the j-th row can be bypassed, thus directly providing (j-1)-th row outputs directly to the (j+1)-th row. Thus, the switching activities will be reduced and hence the power. The Braun Multiplier with Row Bypassing is illustrated in Fig.: 2.

In a column bypassing based Braun multiplier [1], if the multiplicand bit a_i is zero, then the addition operations in (i+1)-th row can be bypassed. The column bypassing based Braun multiplier is illustrated in Fig.:3.

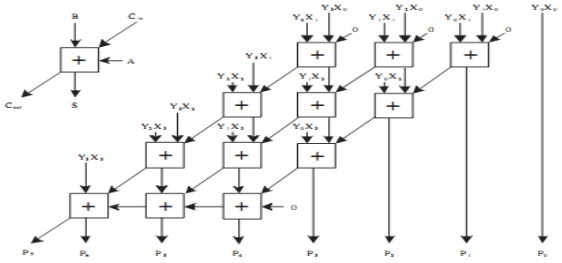

Fig.: 1. 4*4 Braun multiplier

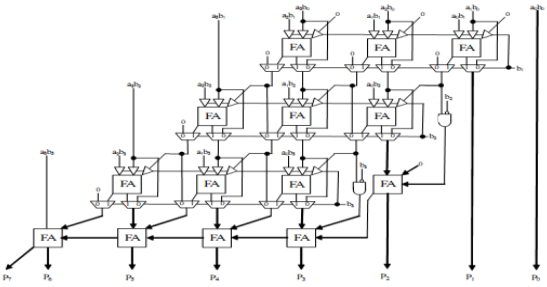

Fig.: 2. 4*4 Row Bypassing Braun multiplier

A multiplier in which either the addition operations in the j-th row or (i+1)-th column can be bypassed is called a 2-dimensional bypassing based multiplier [3]. Here in order to correct the output carry if the bits a_i and b_j are both zero and carry $c_{i,j-1}$ is 1, then either row or column bypassing cannot be performed. So, extra bypassing circuitry is needed. But because of extra circuitry the ability of power reduction is reduced.

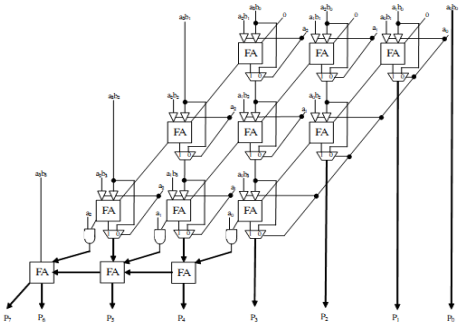

Fig.: 3. 4*4 Column Bypassing Braun multiplier

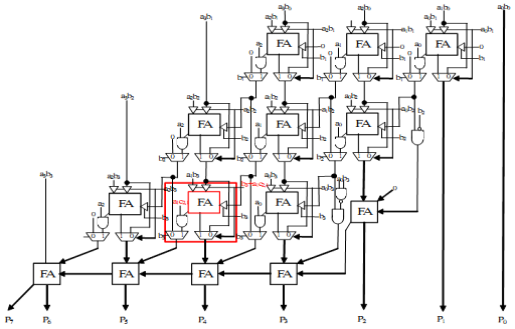

Fig.: 4. Two – Dimensional Bypassing Braun multiplier

A low power multiplier with Row and Column bypassing [4] can be obtained by simplification of full adders. Here the half adders are replaced by the incremental adders or A + 1 adders and the full adders are replaced by A + B + 1 adders. This is as shown in Fig.: 5.

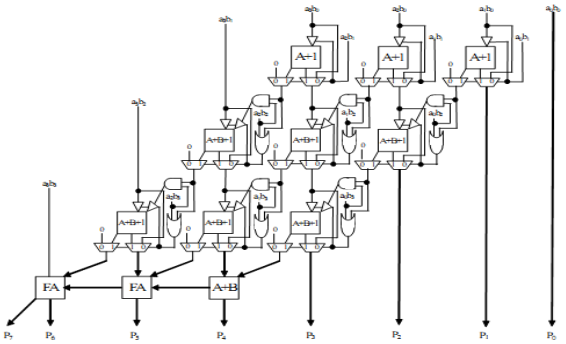

Fig.: 5. Row and Column Bypassing Based Braun Multiplier

III. PROPOSED WORK AND RESULTS

In all the multipliers discussed above, the last stage consists of a ripple carry adder. The delay of the Braun multiplier depends on the full adders and also on the final adder in the last stage. In the last stage, a ripple carry adder has been used. The main drawback of this multiplier is that because of the ripple carry adder in the last stage glitching problem occurs and also the delay of the multiplier will be high.

Ripple Carry adder is a combination of several full adders. The carry input of full adder is dependent on the carry output of the previous full adder, and the present full adder should wait until the previous full adder has completed producing the outputs. Hence, the delay is more for the ripple carry adder. If the number of bits increases, then the delay also increases more for a ripple carry adder.

The delay and power of the multiplier can be reduced by replacing the ripple carry adder with fast adders like Carry look ahead adder and Kogge stone adder. The Modified Row Bypassing multiplier that is obtained by replacing the Ripple carry adder by a Carry look ahead adder and a Kogge stone adder are shown in Fig.: 6(a) and Fig.: 6(b) respectively.

Similarly, the other modified bypassing multipliers are designed. The RTL codes for all the designs as well as their architectural modifications are written in Verilog HDL. All the multiplier designs are simulated and synthesized in Xilinx ISE 13.2 tool and the delay has been calculated. By using different FPGA devices like Spartan-3E, Virtex-4, Virtex-5 and Virtex-6 Lower Power FPGA devices, the delay values have been calculated and a comparison is made among them. The FPGA devices used for comparison are: Spartan-3E (xc3s500e-4-ft256), Virtex-4(xc4vlx15-10-sf363),Virtex-5(xc5vlx30-1-ff324) and Virtex-6 Lower Power (6vlx75tlff484-1l).

The maximum combinational path delay reports for 4*4, 8*8 and 16*16 bits obtained using Xilinx 13.2 ISE simulator for different FPGA devices is shown in Table: 1.

From the above results, it is observed that Virtex-6 Lower Power FPGA is showing the less maximum combinational path delay for the multiplier designs. The proposed work in this paper i.e.; replacing Ripple carry adder in the last stage by a Carry look-ahead adder or by a Kogge stone adder shows the minimum delay.

The glitching problem caused by ripple carry adder can also be eliminated. These changes can be highly noticeable when the number of bits is more.

All the multiplier designs are synthesized in Cadence in 90 nm technology and cell area and the dynamic power reports are obtained by using RTL Compiler tool from Cadence.

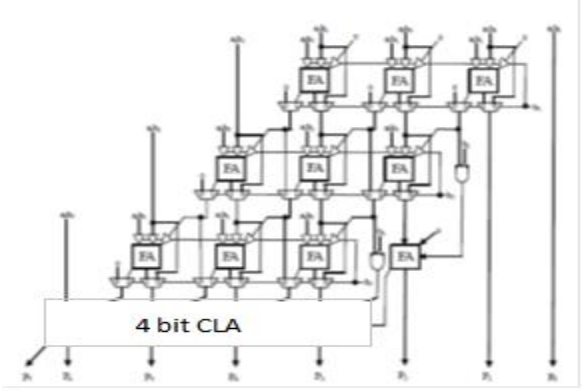

Fig: 6(a). 4*4 Row Bypassing Multiplier with Carry Kogge Look Ahead Adder (CLA) stone adder (KSA)

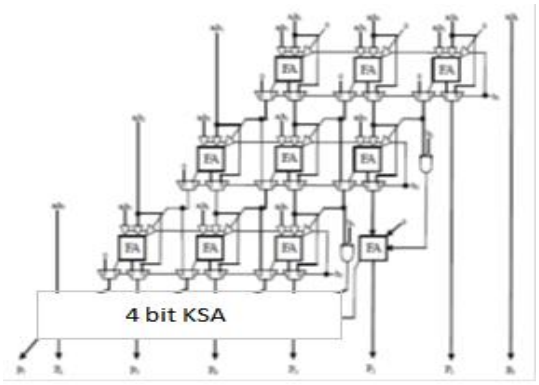

Fig: 6(b). 4*4 Row Bypassing Multiplier with

Design	Spartan - 3E			Virtex - 4			Virtex - 5			Virtex - 6 Lower Power		
	4*4	8*8	16*16	4*4	8*8	16*16	4*4	8*8	16*16	4*4	8*8	16*16
MULTIPLIERS WITH RCA IN THE LAST STAGE												
Braun Multiplier	13.127	23.75	45.194	10.987	18.204	33.366	7.667	13.476	22.807	3.277	8.773	17.594
Row Bypassing Multiplier	14.127	27.599	49.678	11.231	20.157	35.414	7.879	12.981	23.601	3.297	7.366	14.92
Column Bypassing Multiplier	11.955	22.512	42.673	10.032	17.172	30.925	7.545	14.252	25.463	3.319	7.938	16.6
2 - dimensional byapssing based multiplier	15.443	28.548	89.394	12.344	21.195	41.658	7.896	14.821	25.457	3.445	7.796	16.462
Row and Column Bypassing based Multiplier	12.698	26.187	48.093	10.46	19.187	33.345	6.561	13.522	28.226	3.085	6.3	19.585
MULTIPLIERS WITH CLA IN THE LAST STAGE												
Braun Multiplier	13.013	21.87	42.161	10.75	17.096	30.845	6.768	13.722	24.586	2.554	7.83	13.876
Row Bypassing Multiplier	14.832	26.376	56.843	11.068	19.79	40.145	8.354	13.959	24.567	3.383	8.482	16.573
Column Bypassing Multiplier	11.813	21.067	42.502	9.914	16.275	31.247	7.539	14.643	25.551	3.319	8.391	16.647
2 - dimensional byapssing based multiplier	14.593	27.385	58.002	11.72	20.151	40.608	8.798	14.157	26.196	4.971	7.97	15.64
Row and Column Bypassing based Multiplier	12.715	24.666	47.419	10.426	18.556	32.313	6.561	14.52	27.111	3.085	6.846	13.311
MULTIPLIERS WITH KSA IN THE LAST STAGE												
Braun Multiplier	13.24	20.987	34.579	11.02	16.159	25.94	7.936	12.485	19.509	4.208	8.531	14.454
Row Bypassing Multiplier	13.97	29.904	49.076	11.195	21.067	33.8	8.43	13.151	20.789	3.214	7.421	16.037
Column Bypassing Multiplier	11.813	21.957	34.821	9.914	17.035	26.587	7.545	13.739	23.076	3.319	9.312	17.059
2 - dimensional byapssing based multiplier	15.216	27.851	48.255	11.099	20.64	34.699	8.055	14.167	22.117	3.166	6.976	14.699
Row and Column Bypassing based Multiplier	12.715	27.069	40.79	10.426	20.253	30.463	7.465	14.706	24.318	3.085	6.445	13.649

Table: 1. Comparison of Maximum Combinational Path delay between different multipliers for different FPGAs.

The cell area and dynamic power reports obtained using RTL Compiler from Cadence are shown in Tables: 2, 3, 4, 5, 6 and 7, for multipliers with Ripple carry adder (RCA), Carry Look ahead adder (CLA) and Kogge stone adder (KSA) in the last stage.

Table 2: Cell Area of n*n Multipliers with RCA

Multiplier	4*4	8*8	16*16
1	229	1089	4708
2	566	2841	12539
3	423	2117	9365
4	458	2477	11311
5	397	2118	9626

Table 3: Cell Area of n*n Multipliers with CLA

Multiplier	4*4	8*8	16*16
1	316	1125	4779
2	573	2882	12608
3	429	2622	9469
4	487	2521	11557
5	395	1801	9682

Table 4: Cell Area of n*n Multipliers with KSA

Multiplier	4*4	8*8	16*16
1	250	1195	5059
2	1150	3002	12953
3	445	2223	9716
4	517	2638	11726
5	411	1719	9928

1-Braun Multiplier, 2-Row Bypassing Multiplier, 3-Column Bypassing Multiplier, 4-Two Dimensional Bypassing Based Multiplier, 5-Row and Column Bypassing Based Multiplier

Table 5: Dynamic Power (in nW) of n*n Multipliers with RCA

Multiplier	4*4	8*8	16*16
1	15271.302	94537.445	615893.31
2	12017.391	52561.648	198238.64
3	11410.594	49992.233	181291.75
4	23224.551	146622.218	923092.76
5	14842.492	77166.384	363609.15

Table 6: Dynamic Power (in nW) of n*n Multipliers with CLA

Multiplier	4*4	8*8	16*16
1	13250.144	98139.566	609985.21
2	12996.714	52701.055	198053.64
3	11383.028	46738.134	181880.35
4	24004.840	152582.846	972554.95
5	14876.679	118189.948	364761.44

Table 7: Dynamic Power (in nW) of n*n Multipliers with KSA

Multiplier	4*4	8*8	16*16
1	16363.290	106688.362	682672.23
2	17441.173	53119.727	198398.53
3	11598.181	50626.525	182902.63
4	26937.271	165868.142	1009797.1
5	15229.245	58180.035	373221.26

From the cell area reports, it is observed that the cell area is more for Carry Look ahead adder and Kogge stone adder compared to that of a Ripple Carry adder. Kogge stone adder has more area compared to the other two adders.

From the dynamic power results, it is observed that the dynamic power has been reduced for bypassing based multipliers which implies that the total power has also been reduced. The dynamic power is more the Two-dimensional bypassing multiplier because of the extra bypassing circuitry used in its design. The multipliers with Carry Look ahead adder and Kogge stone adder in the last stage have more dynamic power compared to that of the Ripple Carry adder.

IV. CONCLUSION

From the obtained results in Xilinx and Cadence, it can be concluded that if the multiplier is to be used for high – speed applications, then a Kogge stone adder can be used with the multiplier design but the area as well as the dynamic power increases. But by using a Carry look ahead adder in the last stage of the multiplier designs, with a slight increase in cell area and the dynamic power but the delay reduces significantly. Thus, it is observed that the Carry look ahead adder has the optimized values in terms of area, delay and dynamic power. The Virtex – 6 Lower Power FPGA showed the least maximum combinational path delay for different multiplier designs compared to other FPGA devices like Spartan – 3E, Virtex – 4 and Virtex - 5.

V. FUTURE WORK

In this paper, the proposed work has been done for 4*4, 8*8 and 16*16 bit unsigned multipliers. The bypassing techniques with the architectural modifications can also be applied to signed array multiplier architectures.

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