Graphene: A new era of semiconductor devices beyond silicon

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Abstract: *Graphene has an exceptional electronic properties that makes it the successor of silicon. Many groups are fabricating graphene transistors and graphene MOSFETs with a cut-off frequency of 300 GHz. For various RF circuit applications, including low-noise amplifiers, the unique ambipolar nature of graphene field-effect-transistors can be utilized for high-performance frequency multipliers, mixers, and high-speed radiometers. So, the graphene new era has begun.*

Keywords : *Ambipolar, FLG, GFET, graphite, nanotechnology, RF circuit.*

I. INTRODUCTION

Graphene is purely the theoretical form of carbon. In 2004, Andre Geim and Konstantin Novoselov managed to produce graphene flakes with a technique called mechanical exfoliation. Geim and Novoselov were awarded the Nobel Prize in Physics in 2010 for their discovery of graphene. New graphene related discoveries are in nanotechnology news almost every other day. Graphene is a single layer of graphite. It is a lattice of hexagons, each vertex tipped with a carbon atom. Graphene is a single layer of sp2-bonded carbon atoms, that are packed in a honeycomb lattice [1]. The name graphene is sometimes misleadingly used with multiple layers, even though the variation in properties is quite significant when going from one layer to several. It should be noted that multilayer graphene can have up to ten layers, and still be called graphene. Few layer graphene (FLG) has three to nine layers. The limit where graphene becomes graphite is ten layers. It is the thinnest possible material you can imagine, one of the most transparent, the most conductive, the most mechanically strong, and the most elastic and so on. Graphene is a flat monolayer of carbon atoms tightly packed into a two-dimensional (2D) honeycomb lattice, and is a basic building block for graphitic materials of all other dimensionalities. It can be wrapped up into 0D fullerenes, rolled into 1D nanotube or stacked into 3D graphite. [1]. With a high saturation velocity (5.5×10^7 cm/s) [2], graphene is considered a very promising candidate for millimeter-wave applications. Unlike other materials, charge carriers in graphene are massless and behave in many ways like photons, the particles of light. Graphene is a semimetal with a zero bandgap. However, its high carrier mobility makes it the preferred element in scaling transistors. Graphene's zero bandgap results from its valence and conduction band touching at the K points in the Brillouin zone [3]. One method by which bandgap in graphene is engineered is through the application of a vertical electric field perpendicular to the bilayer graphene channel. In graphene, the charge carriers in the two-dimensional channel can change from electrons to holes with the application of an electrostatic gate, with a minimum density (or Dirac) point characterizing the transition. Graphene is also characterized by a linear dispersion relation with the Dirac point separating the valence and conduction bands with no bandgap. This zero bandgap limits achievable on-off current ratios but this does not rule out analog/RF device applications.

II. DEVICE FABRICATION

The device structure of the dual-gate GFET is shown in Figure 1(a). Single-layer graphene was deposited by mechanical exfoliation on high-resistivity Si substrates (> 10 k$\Omega \cdot$ cm) covered with 300-nm-thick thermal oxide. The source and drain electrodes made of Pd/Au metals (20 nm/40 nm thick) were fabricated by e-beam lithography and lift off. The oxide deposition process form a layer of 12-nm-thick Al_2O_3 by atomic layer deposition (ALD) as the top-gate dielectric. Figure.1 (b) shows that the device transfer characteristics were not appreciably degraded after this dielectric process. Finally, the Pd/Au (20-nm/40-nm) metal stack was deposited as the top-gate electrode. Figure.1(c) shows the SEM image of the double-channel graphene transistor with a gate length of Lg = 350 nm. The width of each channel is 27µm, and the spacing between the top-gate electrode and the source/drain contacts is 300 nm.
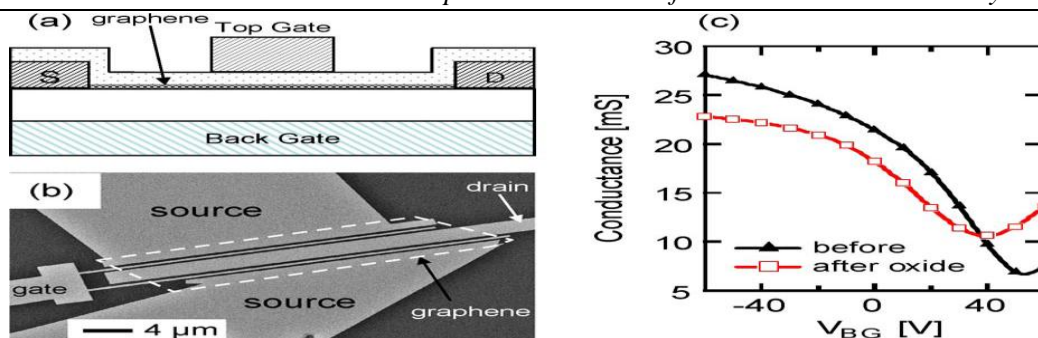
Figure.1(a) Device schematic of the dual gate graphene transistor (b) SEM image of a double-channel graphene transistor.The channel width is 27mm,and the gate length is 350nm for each channel.(c) Measurement channel conductance as a function of the back gate voltage of a graphene devices before and after the deposition of 12nm thick ALD AL 203.Prior to the ALD process,a layer of 2nm AL is deposited and oxidized as the nucleation layer.

III.   TABLES
Table 1. Comparison of graphene for III-V materials.

	InAs	GaAs	InP	Graphene
Electron effective mass(m^*/m_o)	0.023	0.067	0.077	0
Electron mobility($N_D=10^{17}$ cm^{-3})	16000	4600	2800	20000
Electron saturation velocity(x 10^7 cm/sec)	4.0	2.2	2.2	>5
Energy bandgap(eV)	0.36	1.42	1.35	0

IV.   Results And Discussion

A Si substrate is used as the global back gate, while the top gate serves as the main gate terminal for regular FET operations. Fig. 2(a) shows the transfer characteristics of the GFET at different back-gate voltages V_{BG}. At V_{BG} = 0 V, the GFET exhibits ambipolar transfer characteristics with a current minimum at V_{TG} = 0.7 V. This ambipolar transport reflects the gapless nature of the graphene band structure. The current minimum corresponds to the Dirac point, where the total carrier density of electrons and holes in the graphene channel becomes minimal. Dirac voltage V_{DRC}, defined as the top-gate voltage at the Dirac point, is linearly dependent on V_{BG}, as shown in Fig. 2(b), and the slope ($\Delta V_{BG}/\Delta V_{DRC} \approx 35$) can be used to determine the capacitance C_{TG} of the top-gate dielectrics. Using the back-gate capacitance value of C_{BG} = 11.6nF/cm2, C_{TG} is estimated to be 0.40μF/cm2.In Fig. 2(a), the current at the Dirac point decreases with increasing V_{BG}, indicating an increasing series resistance with V_{BG}. This is because the back gate not only shifts the threshold voltage of the graphene transistor but also modulates the graphene that is not covered by the top gate. This additional resistance is analogous to the access resistance in conventional Si MOSFETs. The total resistance of the graphene device (R_T) is modelled as the sum of an ideal graphene channel resistance modulated by the top gate and a series resistance R_S.C_{tot} is the total top-gate capacitance given by

$$C_{tot}^{-1} = C_{TG}^{-1} + C_Q^{-1},$$

where C_Q is the quantum capacitance of graphene. For a relevant carrier density of $\sim 5 \times$ e12 cm−2, $C_Q \approx$ 3μF/cm2, a minimum carrier density $n_0 \sim 5 \times 10^{11}$ cm−2 and a field-effect mobility μ $\sim$ 2700 cm2/V • s, both independent of V_{BG}, was obtained for the graphene channel using the extraction method described in [4] and [5]. In the following, we show that, while the mobility remains constant as V_{BG} varies, the device performance can be improved by optimizing other device parameters. Fig. 2(b) shows the extracted series resistance R_S of the graphene device as a function of V_{BG}, where R_S increases with increasing V_{BG} up to 40 V. This V_{BG} gate dependence of R_S due to ungated graphene is consistent with the trend shown in Fig. 2(c). It is noted that R_S also includes the contact resistance between graphene and metal electrodes. To achieve the optimal RF performance in dual-gate graphene transistors, it is necessary to bias V_{BG} properly so that R_S is at its minimum. Fig. 2(c) shows the transconductance g_m of the graphene device at different back-gate voltages. The impact of series resistance on device performance is evident, as can be seen in the increasing peak values of the p-branch g_m when V_{BG} decreases from 40 to −40 V. At V_{BG} = −40 V and V_{TG} = 1.5 V, the GFET reaches a peak g_m of −0.22mS/μm. It is noted that, while the series resistance is reduced by roughly half from V_{BG} = 40 to −40 V, the peak p-type g_m is enhanced by four times, changing from −0.05 to −0.22mS/μm. The output characteristics at V_{BG} = −40 V are shown in Fig. 2(d). To assess the RF characteristics of the GFET, on-chip microwave measurements were carried out up to 30 GHz. The measured S-parameters were de-embedded using

specific "short" and "open" structures with identical layouts, excluding the graphene channel, to remove the effects of parasitic capacitance and resistance associated with the pads and connections. The use of high-resistivity Si substrates allows for a dc back gate bias while, at the same time, enabling RF operation without significant signal loss. Based on the results in Fig. 2(c), V_{BG} was kept at −40 V in order to achieve the highest RF performance in the dual-gate GFET. Fig. 3(a) shows the current gain |h21| from the measured S-parameters at V_{TG} = 1.6 V and a drain bias V_{DS} = 0.8 V, yielding a cut-off frequency f_T of 50 GHz. The de-embedded current gain |h21| exhibits the −20-dB/dec frequency dependence, as expected for a well behaved FET. This f_T value is the highest frequency reported to date for any graphene transistor, and it also exceeds that of Si MOSFETs (~25 GHz) at the same gate length of 350 nm [24]. Fig. 3(b) shows the peak g_m of p-type GFETs as a function of the series resistance modulated by V_{BG}. The well-known relation $f_T = g_m/(2\pi C)$ established for conventional FETs has recently been demonstrated to be also valid for graphene devices [4]. Based on the measured f_T of 50 GHz for g_m =0.22mS, the right axis of Fig. 3(b) shows the projected f_T as a function of R_S, illustrating a fourfold improvement in f_T as R_S decreases from 110 to 50 Ω.
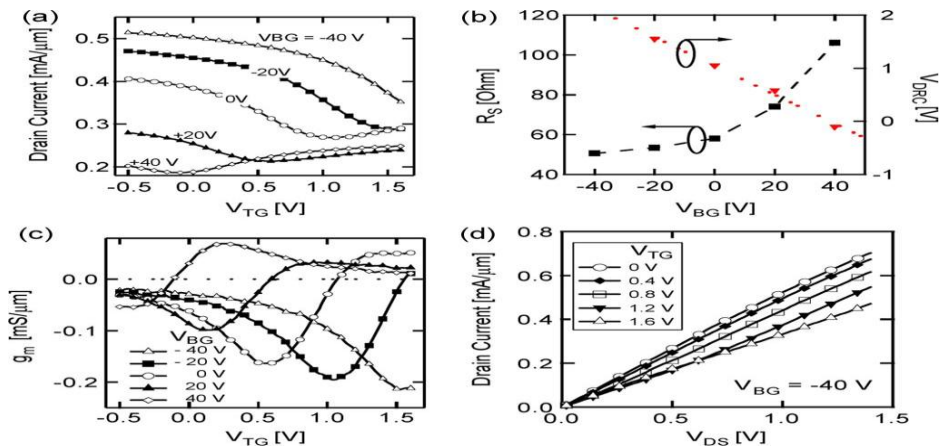

Figure.2 (a) Transfer characteristics of the GFET at various back-gate voltages and V_D = 0.8 V. (b) Series resistance of the GFET and Dirac voltage V_{DRC} as a function of back-gate voltage. (c) Transconductance of the GFET at various back-gate voltages. The drain bias is 0.8 V. (d) Output characteristics at V_{BG} = −40 V.
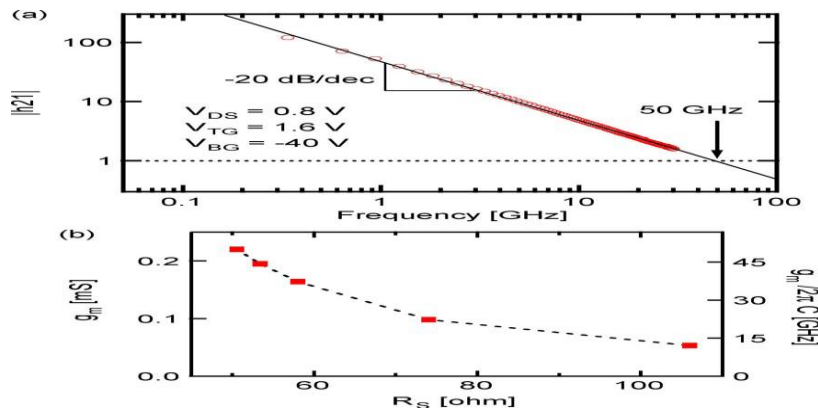

Figure. 3(a) RF performance of a 350-nm-gate GFET, showing a current gain at −20 dB/dec and a cut off frequency f_T of 50 GHz. (b) Peak transconductance as a function of series resistance.

V. CONCLUSION

Graphene is an interesting new material that is relatively easy to produce. It has so many interesting potential applications that it could become the 'new silicon'. The many electrical and mechanical properties of graphene make it a 2D wonderland of physics, not to mention the bountiful chemical properties that have only just began to be researched. It is no surprise then, that graphene is researched in several fields and new findings are reported almost every week.. Future measurements should include stability and durability measurements on GFETs. The top-gate sweeps could be repeated at certain time intervals to find out if the ambient environment changes the electrical properties. GFETs are at the moment very interesting for RF applications, because the cut-off frequency can potentially be raised to the terahertz range. However, the operation of GFETs is limited by the low current on/off ratio and high contact resistance. Also, the question of the existence of full current saturation in graphene remains. The importance of reducing contact resistance is crucial in GFETs with very short channel,

because high contact resistance may otherwise limit the operation and thus lower the cut-off frequency. Furthermore, the cut-off frequency is dependent on the channel length; short channel means high cut-off frequency. Another issue is the very low gain of GFETs. The gain is limited by the contact resistance, current on/off ratio and nonexistent current saturation. Gain is needed in order to cascade GFETs. The low gain is one of the main reasons why there hasn't been an integrated circuit with GFET technology yet, though IBM is said to be working on a graphene IC. All in all, the first GFETs were made just some six-seven years ago, and the pace of improvement is fast. It took decades for silicon technology to replace old vacuum tubes. The main issue in graphene technology actually getting to the consumer markets is the big semiconductor companies themselves. The success and fall of a technology in the end is dictated by the need for better, faster and stronger transistors.

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