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Is a 600-1000V competitive Wurtzite Germanium Carbide power MOSFET having PECVD SiO_2 as the gate dielectric feasible?

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Abstract: *A power MOSFET on 2H-GeC having a wurtzite structure and a bandgap of 2.5 eV is proposed in this seedling article. A set of points are preliminarily listed in this short communication to study the feasibility of fabricating this device. It is the author's contention that a competent device is possible having a high surface field effect mobility of about 700cm^2/V-s and an off-state voltage of 600-1000V can be achieved. The MOS device having plasma-enhanced chemical vapour deposited oxide with Nitrogen at the oxide/semiconductor interface by N_2 or NO annealing will have a low interface trap density and lower near interface trap density than 4H-SiC or 3C-SiC based MOS device that can operate at high temperature of 200°C or more, due to the carbide having a high thermal conductivity as in SiC. Currently, this proposal is an educated speculation by the author.*

Keywords: *Germanium Carbide, power MOSFET, PECVD oxide.*

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I. Introduction

The abundance of Ge is 1.5 atoms in a million atoms of silicon on the earth making it more expensive than silicon, but the electron mobility in a Ge crystal is 3900 cm^2/V-s as compared to 1400 cm^2/V-s in silicon. This mobility can translate to higher surface mobility in a 2H-GeC power MOSFET. Since the native oxide on GeC would be GeO_2 which is water soluble, therefore a deposited oxide is proposed for the MOSFET. The wurtzite 2H-GeC having a bandgap of about 2.5 eV [1] may also prove to be a viable and competent semiconductor material for other power devices such as SCR and BJT.

II. Theory

A set of speculative points are enlisted below as part of the theory and forms the basis for the affirmative feasibility. The points in this seedling article are as follows:

1. SCR operation is suitable at high voltage and high current at low switching speeds. BJT operation is suitable at low voltage and high current at medium switching speeds. MOSFET operation is suitable at medium voltage and high current at high switching speeds. The low frequency 1/f noise fluctuate drain current of MOSFETs operating at low switching speeds. SCR—originated from the Shockley diode at GE during 1955-1957 [2].
2. Linus Carl Pauling (Nobel)-Electronegativity—Carbon (At.no. 6, Carbides), Nitrogen (At no. 7, Nitrides), Oxygen (At no. 8, Oxides), Fluorine (At no. 9, Fluorides), SiC, GeC, GaN, SiO_2, Si_3N_4, Al_2O_3, CF_4, NF_3
3. Baliga's figure of merit related to specific on resistance [3-4].
4. Wide Band Gap (WBG) Review [3-4].
5. –OH (hydrophilic) termination after RCA cleaning, unlike in Silicon which has H-(hydrophobic) termination [5].
6. GeO_2 native oxide is water soluble. SiC has the advantage that native oxide can be grown by oxidation in a furnace, but for GeC MOS device, a deposited oxide is required because the native oxide is water-soluble.
7. N_2 or NO annealing to reduce D_{it}. SiC MOS device after N at interface is similar to GaN MOS device for the 600-700°C processing temperatures with same D_{NIT} levels of 24 x 10^{11}/cm^{2}eV. At higher processing temperatures of 900-1000°C, GaN MOS device has a D_{NIT} level of 40 x 10^{11}/cm^{2}eV. Therefore GeC MOS device with N at interface will give D_{NIT} of about 20 x 10^{11}/cm^{2}eV, as it has a slightly smaller bandgap of 2.5 eV (similar to 3C-SiC at 2.38 eV) as compared to 3.23 for 4H-SiC. GeC is not expected to have high density of acceptor states near CB similar to 3C-SiC because the bandgap is 2.5 eV only and the acceptor states are near 2.8 eV above the VB edge. So, the mobility is expected to be high as in 3C-SiC, although the off-state voltage will be lower than in 4H-SiC having a larger bandgap of 3.23 eV. GaN MOS and GeC

MOS will have lower throughput and will be more expensive than MOS on SiC having a grown oxide that can be mass-produced due to thermal oxidation process involved. However, some niche applications can be assigned to GaN MOS which does not require processing to place N at the interface. Just as Si-C-O-N correlated bonds are formed at the interface in a SiC MOS device after NO annealing, Ge-C-O-N bonds would form at the oxide/semiconductor interface after NO annealing in GeC MOS device [6-9].

8. Deposited oxide, Oxide/Nitride/Oxide (ONO), Al_2O_3, PECVD SiO_2.
9. Density of near-interface traps, D_{NIT} = (2.5/3.3) x 12 x 10^{11}/cm^2 possible= 9 x 10^{11}/cm^2. If the low field leakage current observed on the n-type MOS device on 4H-SiC is same as the calculated displacement current, say for 20 nm oxide at 1.7 x10^{-8}A/cm^2, then the D_{NIT} becomes negligible and interface trap density becomes low. The surface field effect mobility will increase in the n-channel MOSFET on inverted p-type MOS device, but the oxide breakdown field will become lower due to presence of high density of positive fixed charges in the complementary p-type device with the same processing that gives negligible D_{NIT} on the n-type device [6-9].
10. Photovoltaic application is considered with GeC and ZrN as an absorber material (Neeti Gupta, Ph.D. Engg., 2016, New South Wales, Sydney, Australia).
11. Si_3N_4 has even-odd combination of electrons which results in more bulk defects in silicon nitride. SiO_2 has even-even combination of electrons. So, it has less bulk defects. Oxygen in the SiO_2 also provides lower interface trap density with a semiconductor such as silicon. O (Atomic no. 8), N (7), Si (14).
12. Surface mobility in GeC (Eg=2.5 eV) MOSFET could be 700-800 cm^2/V-s as compared to 3C-SiC (Eg=2.38 eV) MOSFET at 260 cm^2/V-s. Electron bulk mobility in Ge is 3900 cm^2/V-s as compared to Si is 1400 cm^2/V-s. The higher mobility in Ge will translate to higher mobility in GeC.
13. The power MOSFET can work at temperatures greater than 200°C as the carbides have higher thermal conductivity.
14. 3C-SiC has a high density of intrinsic defects at 1.8 x 10^{33}/cm^3. The wurtzite 2H-GeC may or may not have that high density of defects. Ge has a density of intrinsic defects at 6.7 x 10^{17}/cm^3 at present [10]. The technology can be improved to reduce defects density.
15. Abundance of Ge on earth is 1.5 atoms in 10^6 atoms of silicon on earth [Wikipedia].

III. Results and Discussion

The speculative points in the theory results in a envision of a power MOSFET having a surface field effect mobility of up to 700 cm^2/V-s that can work at 200°C and have a off-state voltage of 600-1000V.

IV. Conclusion

A competitive power MOSFET on 2H-GeC having a high surface mobility is feasible, and it can work at high temperatures of 200°C or more. Other power devices such as an SCR, BJT, and IGBT can also be considered on wurtzite 2H-GeC semiconductor having a wide band gap of about 2.5 eV

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