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Method for High Speed Signal Analysis

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***Abstract**: In the context of high-speed circuits, the layout analysis of the Printed Circuit Boards (PCB) is always critical and necessary. Due to the high costs of rework when the problems are detected in the clients and due high costs of tools, such as Vector Network Analyzer, for analysis behavior of circuits, using simulation tools is the best way to detect problems in high-speed designs.This work proposes a method to identify phenomena, such as ripple, crosstalk, insertion losses and return losses, that degrade the integrity of signals in transmission lines, evaluating, through simulations, circuits in the frequency domain (S-Parameters). The proposed solutions, changes were made in the printed circuit board design itself, and a simulation of noises from industrial processes was also used to correct problems related in PCB traces, more specific back drilling.*
***Key Words**: High speed signals, Insertion loss,Mixed Mode S-Parameters, Return loss and Signal integrity.*

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I. Introduction

In the 1980s, the war between the Asian and American markets for the capacity of memories, the development of faster processors, increased transmissions rates of internal and external communication, miniaturization and other factors led to a growing evolution that has persisted until today. Today there is the IoT (Internet of Things) and the possibilityto do anything over a Smartphone.An IoT ecosystem consists of web-enabled smart devices that use embedded systems, such as processors, sensors and communication hardware,to collect, send and act on data they acquire from their environments. The IoT devices share the collected data from sensors by connecting to an IoT gateway or other edge devicewhere data is either sent to the cloud to be analyzed Sometimes, these devices communicate with other related devices and act on the information they get from one another. The devices do most of the work without human intervention, although people can interact with the devices for instance, to set them up, give them instructions or access the data, using multitude of protocols, it is possible to receive and send data, audio, video, image files, documents and this demand has only one way, which is to grow. However, there is still a need for physical devices to process these demands. These physical devices are getting smaller and need greater processing capability, so the Electronic Engineers need to control factors that previously could be disregarded.The need for greater data transfer, with higher speeds andwith smaller hardware dimensions and costs, transformed the concept of electronic circuit designs, more specifically for the Printed Circuit Boards (PCB). The objective of this paper is to develop a method that will contemplate, through numerical simulations, a diagnosis of high-speed signal behavior through all devices that an electronic project has. The methodology presented in this paper demonstrate all the steps for the correct simulation evaluation and the correct method execution.

II. Material and Methods

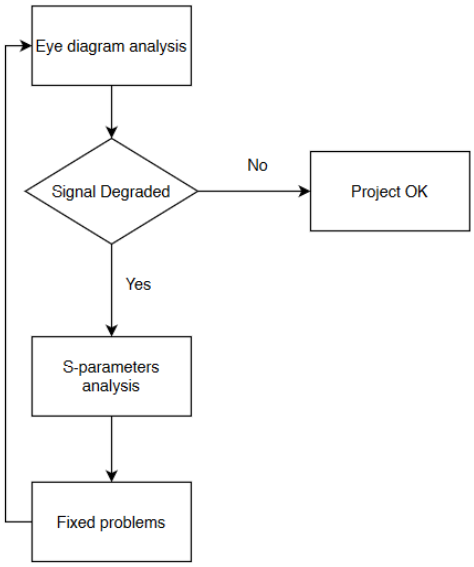
In this chapterwill be presented the methodology adopted for the development of this work.The methodology proposes guarantee the signal and power integrity in critical circuits. The DC Analysis is applied to map voltage drops on the printed circuit board, as well as checking the highest current levels. For the signal integrity analysis, the targets are the differential pairs used in PCIe GEN3 standard. The transmission lines, that is, the communication buses of these signals, pass through the FMC connectors.The FPGA used will be the XCKU040FFVA1156 from XLINX®, as VRM model, the MAX15301 family components from MAXIM INTEGRATED®, the SSD used belongs to the 2100 PCIe NVMe Solid State Drives family, Micron®. Tab. 1 shows the technical characteristics of the components used in the simulation.

Table no 1: Technical characteristics of the components.

Partnumber	Manufacturer	Transmission rate
XCKU040FFVA1156	XLINX®	PCIe Gen3 x 4 lanes (1GB/sec por lane)
Micron 2100 PCIe NVMe Solid State Drives	Micron®	read/write 2,100/2,000 MB/s

In the simulation stage, the SIwave® and Ansys Electronics® simulation tools will be used to acquire the necessary parameters to evaluate the signal degradation.In theSIwave®tool willbe do DC analysis, voltage drops, current levels, crosstalk, S-parameters,and resonant models. In the ANSYS® Electronics tool it is possibleto do the transient analysis. Fig. 1 shows the simulation flowchart that must be performed to obtain the results.

Figure 1: Simulations workflow.



Initially, the project file for ODB++ is converted to be imported into SIwave®.The DC Analysis is applied to map voltage drops on the printed circuit board, as well as checking the highest current levels. It is necessary choose the target traces, in this case, the differential pairs used in PCIe GEN3 standard. In Ansys Electronics®, touchstones files are used for passive interconnections and IBIS models for active components. After the definition of transmission lines, and the design schematics, the eye diagram is the first step to verify the signal integrity, this analyze has two metrics to evaluate, jitter and eye diagram. Ajitter higher than specified and a close eye diagram,it is a clear evidence of degradation ofthe signal, and it can be for two reasons, dielectric loss, and conductor loss.The next step is to calculate the S-parameters, to a complete signal analysis in the frequency domain. In this case study, the analysis is made with Mix Mode S-parameters, particular case for differential pairs.

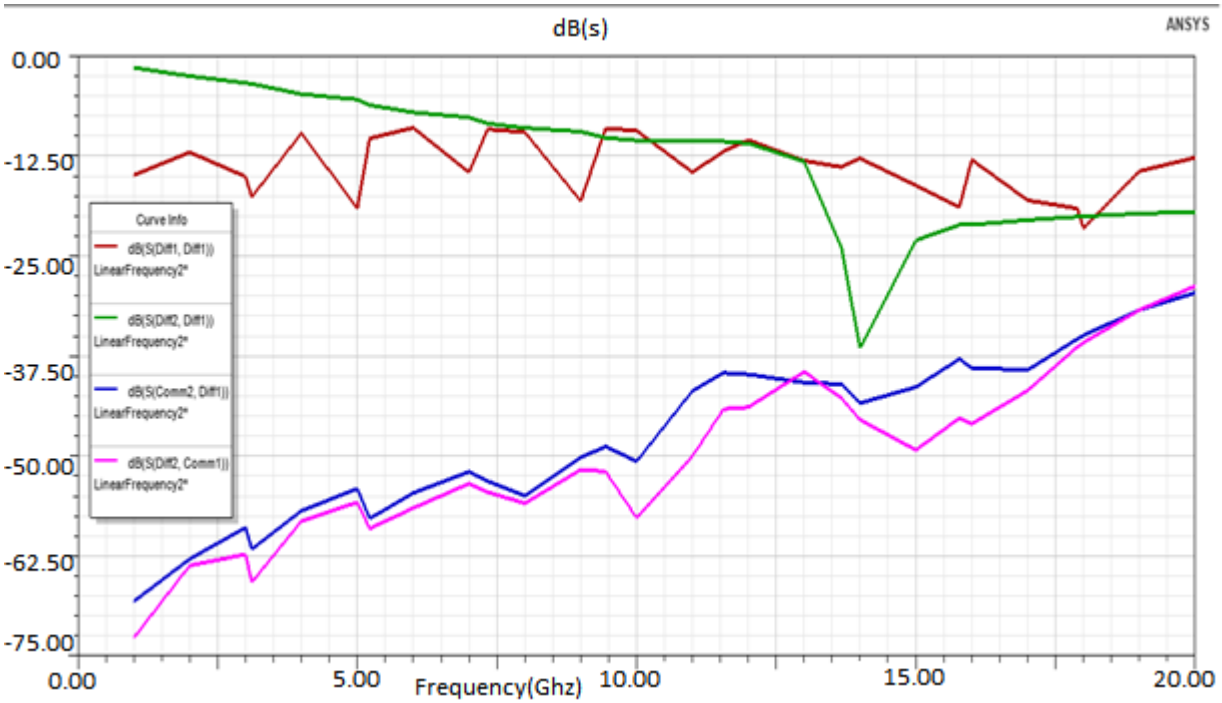
III. Results

A signal is injected into the target traces, where it is possible to evaluate insertion loss and reflection loss, the equation 1 shows the behavior of insertion loss ($SDD_{2\ 1}$) with the frequency.

$$\mathrm{SDD}^{21}\left[\frac{dB}{in}\right] = -4.34x\left(\frac{\mathrm{Rlen}\left[\frac{\Omega}{\mathrm{in}}\right]}{\mathrm{Z0}[\Omega]}(Conductor\ loss) + Gl[Siemens\backslash in]xZ0[\Omega](Dieletric\ loss)\right)(1)$$

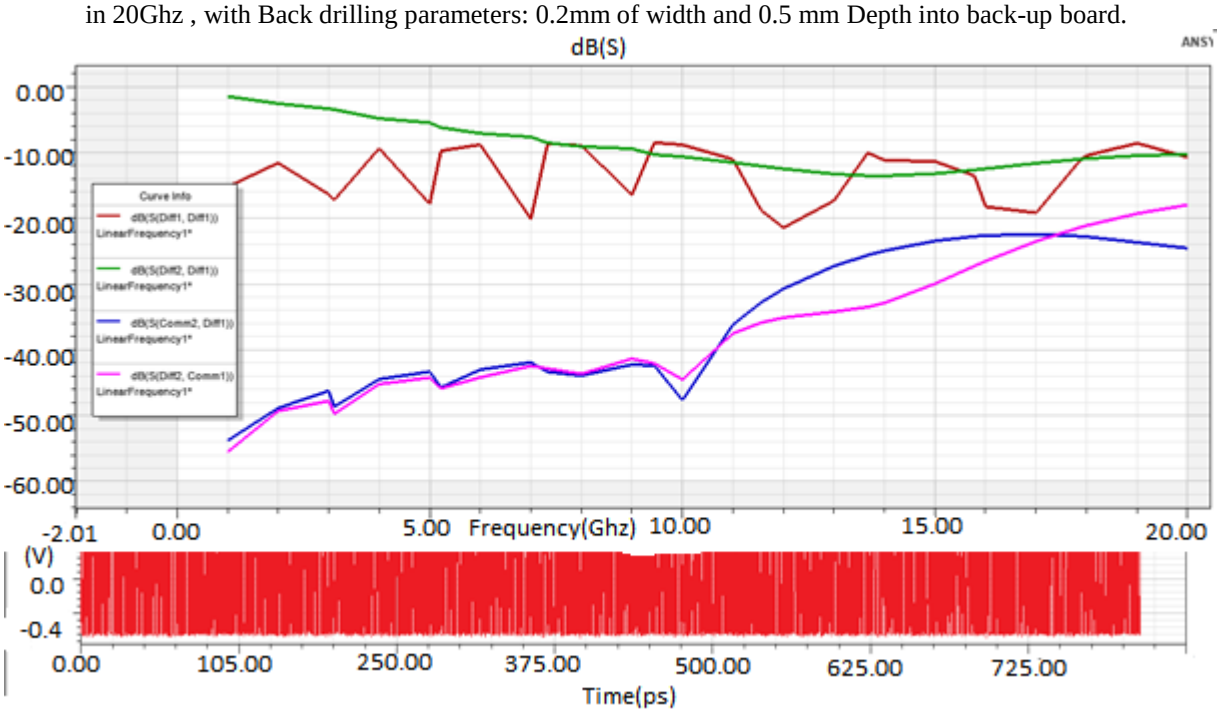
Where the first part of equation 1 is related to the differential pair (conductor loss), the important metrics are length and impedance. The part about dielectric loss in equation1, has the material of printed circuit board and impedance aspects thathave major influence in attenuationsignal [12]. The Fig. 2 shows the $SDD_{1\ 1}$, $SDD_{2\ 1}$, $SDC_{2\ 1}$ and $SCD_{2\ 1}$ parameters, with these four parameters is possible to see the signal behavior related to signal integrity. According to[12], the applied rule in the insertion loss ($SDD_{2\ 1}$, green line), the signal should ideally reach the maximum -10db of attenuation scale, at the specified maximum frequency, but the green line demonstrates the $SDD_{2\ 1}$ parameter, reaches close to -37dB, and this is not the expected behavior according equation 1.

Figure 2: Calculated Mixed mode S-parameters in a differential pair, with1.2 mm width and 120mm of length in 20Ghz.



Important aspect to be considered is the return loss ($SDD_{1\ 1}$, red line), if this parameter is greater than -10dB, the circuit could be a problem related to ripple noise, howeverthe magnitude in dB of this parameter is within the acceptable range, with magnitude valueclose to -10 dB.The pink line is the susceptibility-related conversion mode ($SDC_{2\ 1}$) or whether the circuit is susceptible to electromagnetic problems, to evaluate the behavior in S-parameters, if the magnitude valueis above -30 dB, it's an indicative an asymmetric transmission lines,this aspect is possible to see in Fig. 2. In the blue line it refers to the conversion mode of electromagnetic emission $SCD_{2\ 1}$, if the magnitude (dB) of the parameter $SCD_{2\ 1}$, exceeded $SDD_{2\ 1}$ (dB), in this case, the value of $SCD_{2\ 1}$ is bigger than $SDD_{2\ 1}$, it could be indicativeof these differential pair being aggressive of nearby trails, but the Fig.2 shows that the behavior is acceptable[12].With this analysis, a sharp drop in the frequency close to 14GHz was found in $SDD_{2\ 1}$, as shown in Fig.2. The problem is related to the concept of stub, to fixed it is necessary to use Back drilling, which is a manufacturing technique used in high-speed multi-layer plates, in order to reduce eddy currents, generated by the coated holes [3]. This paper is focused on simulation, in this case,the tool back drilling of SIwave® itself was used, to reduce the stub related vias (vertical interconnect access) of the differential pair. With the analysis done, the Fig. 3 demonstrate the behavior of S-parameters after the Back drilling.

Figure 3: Calculated Mixed mode S-parameters in a differential pair, with 1.2 mm width and 120mm of length in 20Ghz , with Back drilling parameters: 0.2mm of width and 0.5 mm Depth into back-up board.



The signal $SDD_{1\ 1}$ (red line)has a very similar behavior, before the correction, it starts in lower negative value in dB, in low frequency andthe signal goes to -9dB, above -10dB theoretically the signal has a noise ripple, but this is not seen in the parameter$SDD_{2\ 1}$. The $SDD_{2\ 1}$ in the green line, the broad attenuation gone, and the $SDD_{2\ 1}$ has a closer behavior of the equation 1.The$SDC_{2\ 1}$ and $SCD_{2\ 1}$ parameters are the very similar behavior of before the Back-drilling simulation, and in this case, an expected behavior related to a high-speed, but if the $SDC_{2\ 1}$ (pink) and $SCD_{2\ 1}$ (blue) have the magnitudes bigger than, $SDD_{2\ 1}$ the circuit can be a problem related to crosstalk, or noise ripple, these phenomena can be solve with a different layout, or other approach of design using more decoupling capacitors.But in this paper the relevant problem is related to broad attenuation in $SDD_{2\ 1}$, solved by back drilling.

IV. Conclusion

This paper explains an increasingly adopted path, which is the simulation in the design phase. To support the stage of knowledge about the causes and impacts of power integrity, the basic concepts about Power Delivery Network and electronic circuits in connectors were searched in bibliographies, and the phenomena that may affect their design. For the simulation and measurement steps, searches in related works were necessary for the premises for the execution of these activities. The lack of work aiming at the analysis in connectors, serves as a motivation and supports the implementation of the work in question. However, the distance from the academic world to the business environment is real, although some companies have already adopted simulation and previous analysis in their projects, this practice is still unusual, because a most accurate software has a high value, and affect the internal process of the company. Despite the proposed method, the great challenge of this paper is, evaluating the S-parameters. It is true that the simulation software provides the results, but the theory of the S-parameters and the analysis of each signal, changes significantly in each case, the great legacy of this work is the synthesis and the direction of how this analysis can be complex, but it can reveal many conditions that were previously unthinkable, how to solve random failures, and how to shield the circuits to problems related to EMC and EMI. This paper idea is toserve as a guide, also, for RF (Radio Frequency) projects, because the analysis of the S-Parameters is very similarly, changing only a few parameters,for layout analysis of a very dense board in terms of tracesand layers, and as the IoT market, is one of the largest at the moment, the analysis of Antennas Wi-Fi is also a target of paper. This paper is an easy information for the hardware designers, the paper referenced a specific knowledge, to understand the losses and the behavior in a printed circuit board related to a high speed circuits and read S-parameters like a book and with the case study showed how to solve the problems related to Stub in vias.

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