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# Design and simulation of ultra-wideband low noise amplifier for ultra-wideband wireless communication with 0.8 mW power consumption using diode connected transistor

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***Abstract:*** *This paper presents the design and simulation of two stages common source low noise amplifier using diode connected load technique. The amplifier designed and simulated using 130 nm CMOS technology. The amplifier circuitry provides 50.33 GHz bandwidth with power gain of 15 dB. Output noise reduced to 138.2 $uV_{rms}$ as using diode connected load technique and the circuitry gives noise figure of 0.9 dB and input referred third order intercept point of 34.66 mdB. The proposed LNA dissipates very low power reached to 0.8 mW using power supply of 1.2 V.*

***Background****: Low noise amplifier is considered the most important part in radio receiver, it is responsible for amplifying and boosting the received signal at a certain level above noise floor and as a result it can be used in different applications. The design of low noise amplifier is a difficult emission as there is trade of between its parameters to give the suitable performance. There are different parameters determine the quality of LNA such as noise figure, gain, bandwidth, linearity and power dissipation. In this proposed study the diode connected transistor which act as a load improves a lot in these parameters, and finally we will get low noise amplifier with wide bandwidth, high gain, good linearity, low noise figure and low power dissipation.*

***Materials and Methods****: In this proposed study two low noise amplifier circuitry are simulated, one of them is the traditional low noise amplifier circuitry which is the circuit we start from, and the other circuit is the proposed low noise amplifier. The traditional LNA circuit uses stagger tuning technique consists of two common source stages to improve the performance of the low noise amplifier. The drawback of this traditional circuit is using very high (MIM) coupling capacitors in the input and output and this will increase the parasitic capacitance of the circuit and so the bandwidth will be reduced also the noise figure will be increased. In the proposed low noise amplifier circuitry the parameters of LNA is improved by using diode connected load technique without affecting on the bandwidth or the output noise of amplifier as some of coupling capacitors in the traditional circuit will be removed in the proposed one. The two circuitries will be simulated and the advantage of the proposed diode connected load technique will be discussed.*

***Results****: The performance parameters of the proposed LNA circuitry is simulated, the noise figure parameter is simulated, bandwidth and amplifier gain are simulated. The linearity of the circuit has been also simulated and the power consumption of the circuit is calculated. The layout of the proposed LNA is introduced.*

***Conclusion:*** *The performance parameters of the low noise amplifier are improved a lot by using diode connected load technique to get a low noise amplifier suitable for ultra-wide-band wireless communication.*

***Key Word****: Low noise amplifier (LNA); ultra-wide-band (UWB); Noise figure (NF); Diode connected transistor.*

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## I. Introduction

Nowadays, the design of low noise amplifier with low dissipated power, low noise figure and ultra wide band has a great attention, especially as the great applications which required low dissipated power and wide bandwidth low noise amplifiers in its operations such as high speed wireless communications[1]. Ultra wide band systems (UWB) are operating at frequency ranging from 3.1 GHz- 10.6 GHz[2]. As, low noise amplifier is considered the most challenging building block in UWB systems, so the development of its performance is considered an important target. There are many parameters that describe the LNA performance[3], the low noise figure (NF), low dissipated power and wide band width with a good linearity are the most important parameters in developing LNA operation. So, the design of LNA involves tradeoffs between its parameters such as noise

figure (NF), dissipated power, gain and linearity[4]. Great efforts have been done to satisfy these goals to design a LNA with good performance. There are many LNA design technique have been listed to achieve these goals. One of these techniques which use stagger tuning technique consists of two stacked common source stages with different resonance frequencies[5] to achieve a bandwidth ranging from 2.6 GHz to 9.2 GHz and noise figure of 3.5 dB. Another technique[6] that designs low noise amplifier using two common source and shunt feedback stages to provide a bandwidth ranging from 1.85 GHz to 10.2 GHz and noise figure of 4.5 dB. In this paper a very low dissipated power, low noise figure, high linearity and wide bandwidth low noise amplifier is proposed and designed in 130 nmCMOS technology, which consists of two stages common source using diode connected load technique, to satisfy the requirements of the ultra-wide band (UWB) systems in the noise, dissipated power and bandwidth. The design parameters and simulation results of the proposed LNA are presented.

## II. Low noise amplifier overview in UWB systems

The functional block diagram of ultra-wideband receiver is shown in Fig. 1. The main building block in the UWB receiver is LNA, by improving LNA performance so, the UWB system operating well. The ultra-wideband signal can be transmitted over very wide bandwidth. Ultra-wideband system is capable of transmitting and receiving wireless signals at very high rate and consuming a very small amount of power. There are many applications of UWB not only wireless communication but also imaging and radar applications.

As shown in Fig. 1, the block diagram of UWB receiver which receives a very low value of emission power from UWB transmitter in order to prevent interfacing with other wireless devices which operating at lower wireless standards. The design of LNA for UWB applications differs from those of narrowband wireless systems. in this paper the design of low noise amplifier with ultra bandwidth, low noise figure, good linearity and very small power dissipation is provided.

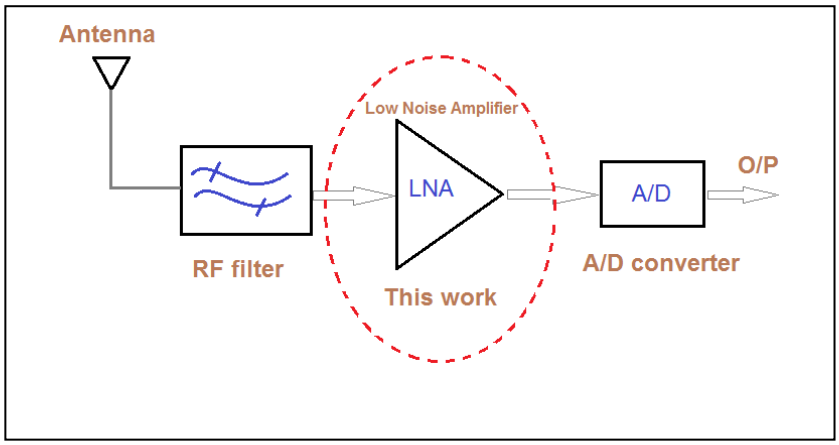


**Fig. 1:** Ultra-Wideband Receiver (UWB)

## III. The proposed low noise amplifier circuitry

In this section the traditional low noise amplifier and proposed low noise amplifier will be discussed in details and a comparison between these configurations will be presented. The advantage of the proposed diode connected load technique in noise reduction and return loss will be discussed with results.

***Traditional LNA circuitry design using stagger tuning two common source stages***

The traditional low noise amplifier circuit diagram that uses a technique of stagger tuning[5] is shown in Fig.2. The amplifier circuitry consists of two common source cascaded stages. The first stage of the two cascaded stages is used to dominate noise performance of the LNA amplifier and the second stage is used to optimize linearity performance of the amplifier. The traditional LNA circuitry as shown consists of source inductor Ls which used to generate real part for input impedance matching. The other circuit components $L_g$, $L_3$, $L_4$, $C_3$, and $C_4$ are used for matching network at the input. $M_3$ is the output transistor works as a buffer for output measurement. The resistor R is used to provide bias voltage for the transistor $M_2$. The power saving of this traditional LNA circuit is demonstrated by by stacking the second stage on top of first stage[7]. Capacitors $C_1$ and $C_2$ are used for coupling purposes, as capacitor $C_1$ for coupling between the two stages and $C_2$ works as AC ground at the source of $M_2$. In this technique the values of $C_1$ and $C_2$ must be very high to provide better coupling. The problem in this design technique using two common source stages that the two coupling capacitor $C_1$ and $C_2$ are Metal-Insulator-Metal (MIM) capacitors and their values are very high, because large MIM capacitors will suffer from parasitic capacitance between bottom plate of the capacitor and ground, this will

reduce circuit gain, affect bandwidth and increases output noise of LNA. Besides the problem of parasitic capacitances of coupling capacitors, this traditional circuit uses six inductors and 4 capacitors for its operation, this will increase the power consumption of the LNA.

In the following section the proposed UWB, low noise figure and low power dissipation LNA is presented. Which solve the problem of coupling capacitors, bandwidth reduction and output noise, by using diode connected transistor $M_D$ in parallel with $M_4$ in the proposed LNA.

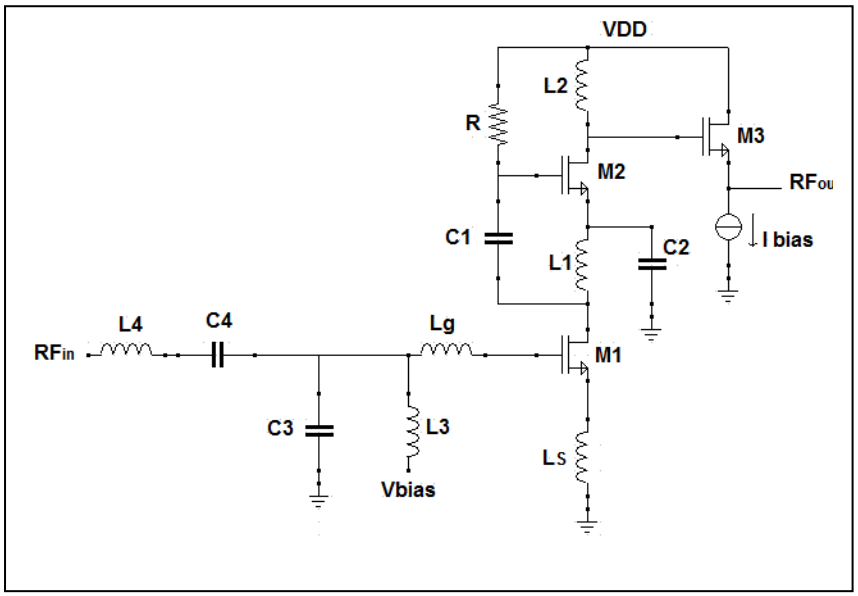


**Fig. 2:** Traditional LNA circuitry design using stagger tuning two common source stages[5]

***Circuitry diagram of the proposed LNA using Diode connected load***

The circuit diagram of the proposed low noise figure, low power dissipation and wide bandwidth LNA uses diode connected load technique and two common source stages is shown in Fig. 3. As shown the circuit consists of two common source stages, $C_4$ and $L_3$ are used for impedance matching at the input. To show the effect of this proposed technique, some results are obtained for LNA about output noise, power dissipated, noise figure (NF), input reffered third order intercept point ($IIP_3$), bandwidth and gain. The simulation results of the proposed LNA circuitry shows the effect of diode connected load transistor ($M_D$) on the amplifier performance.

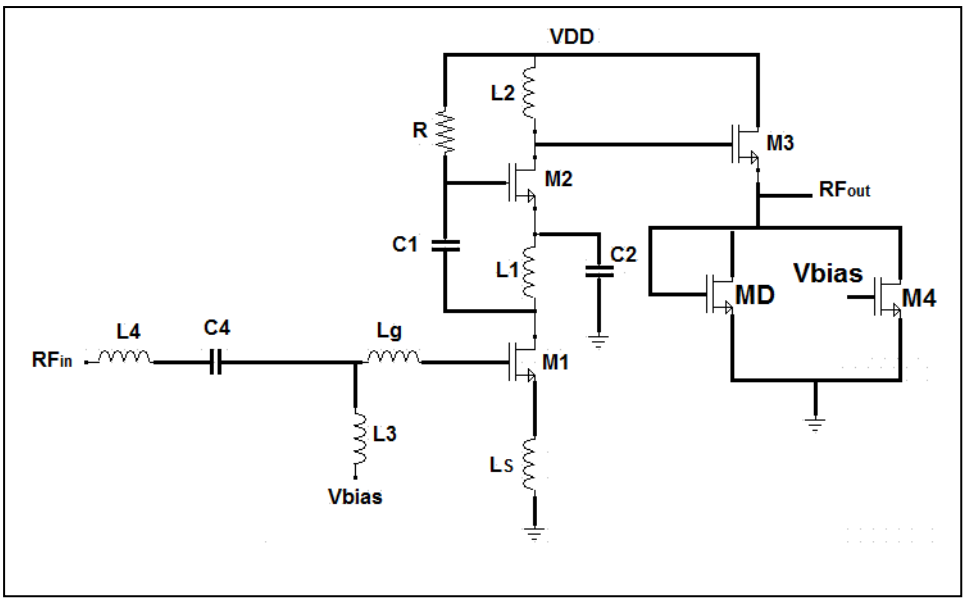


**Fig. 3:** The proposed LNA using diode connected load technique

## IV. Result

A performance comparison has been made between the traditional LNA and the proposed LNA as shown in Table no1. As expected the proposed LNA has performance parameters better than the traditional LNA. The proposed LNA has bandwidth of (50.33 GHz) higher than the traditional LNA using two common source stages, because of the elimination of large coupling capacitor $C_3$. The output noise of the proposed LNA is reduced to 138.2 $uV_{rms}$ because of the diode connected load technique and so noise figure is reduced to 0.9 dB. Also, the dissipated power of the proposed LNA reached to 0.8 mW which compared with traditional LNA which has dissipated power of 15.04 mW. It is clear now from the comparison the effect of using diode connected load technique in output noise. the effect of diode connected load technique will be discussed in the following section.

**Table no 1**. Parameters comparison between the traditional LNA and the proposed LNA using diode connected load.

| **Parameter** | **Traditional LNA** | **Proposed LNA** |
|---|---|---|
| Technology | 130 nm CMOS technology | 130 nm CMOS technology |
| Power supply | 3.2 V | 1.2 V |
| Bandwidth | 6.57 GHz | 50.33 GHz |
| Gain | 5 dB | 15 dB |
| Output noise | 2.26 $mV_{rms}$ | 138.2 $uV_{rms}$ |
| Dissipated power | 15.04 mW | 0.8 mW |
| Noise figure (NF) | 7 dB | 0.9 dB |

**Effect of diode connected transistor on LNA performance**

As known the equivalent small signal model of diode connected transistor is very small resistance ($1/g_{mD}$). The transistor generate maximum output noise when it sees only its own output impedance as a load and noise current of the MOS transistor decreases if the transconductance drops. A small transconductance $g_{m4}$ can be occurred as $M_D$ is connected in parallel with the output transistor $M_4$, and this will decrease $M_4$ noise and the total output noise of the circuit as well. In the proposed UWB LNA the capacitor C3 which in the traditional circuit can be removed in the proposed circuit and the input matching still occcured. Removing C3 will be increase a lot in the proposed LNA bandwidth. So the proposed UWB LNA has a better bandwidth than traditional one. CG suffers from low gain so in our design we have used two common source (CS) stages to improve gain and bandwidth. The proposed UWB LNA has two amplifier stages as shown in Fig. 4.

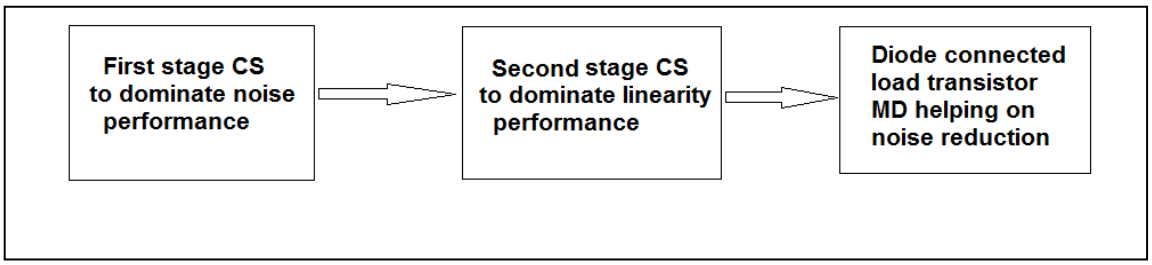


**Fig. 4:** Different stages of proposed design

Figure 5 shows the simulation of the noise figure for the proposed LNA. The circuit gives a very low noise figure value which is 0.9 dB, this happened due to using diode connected load transistor. Diode connected transistor which connected in parallel with output transistor reduces output noise of the circuit and so the output signal to noise ratio will be increased. This increasing in output signal to noise ratio will reduces the noise figure value.

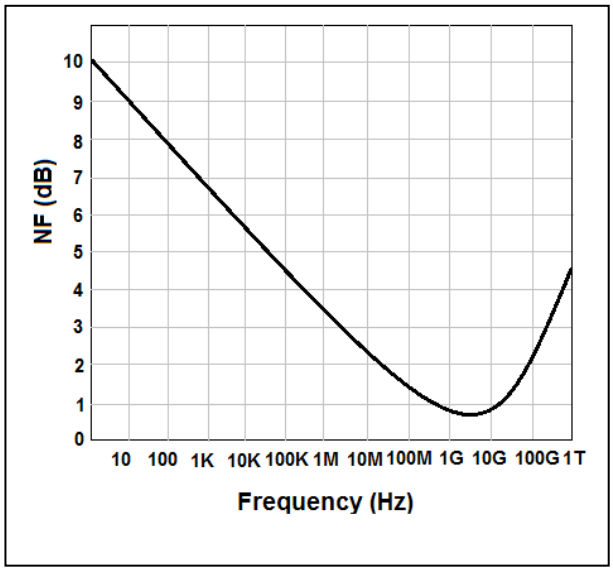


**Fig. 5:** Noise Figure (NF) analysis

Figure 6 shows the plotting of input referred third order intercept point (IIP3) which describes the linearity of the proposed LNA at its operating frequency range. As shown from the plotting that input referred third order intercept point (IIP3) is reached to 34.66 dBm, this means the circuit has a good linearity through the proposed frequency range of 50.33 GHz.

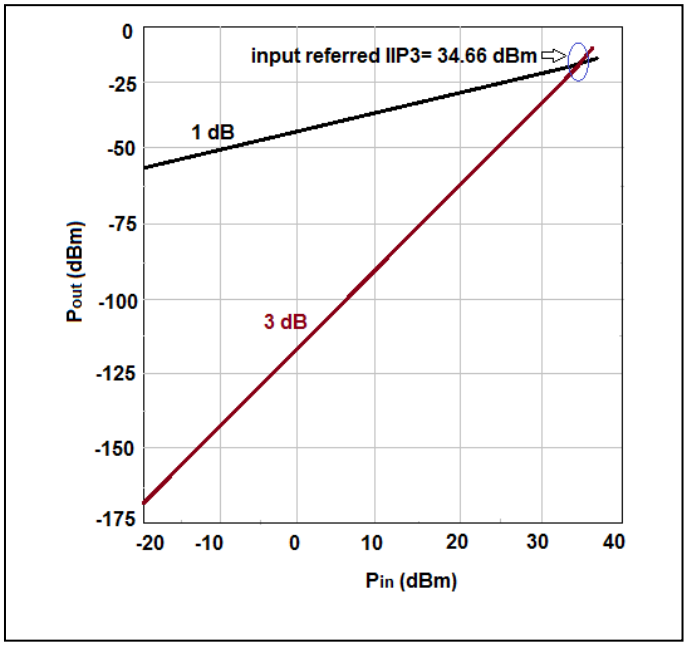


**Fig. 6:** Third order input referred intercept point (IIP3)

Figure 7 shows the simulated return loss $S_{11}$ and $S_{22}$ through the operating frequency range of the circuit. As shown the return loss $S_{11}$ is below -1 dB through the operating frequency range 50.33 GHz.

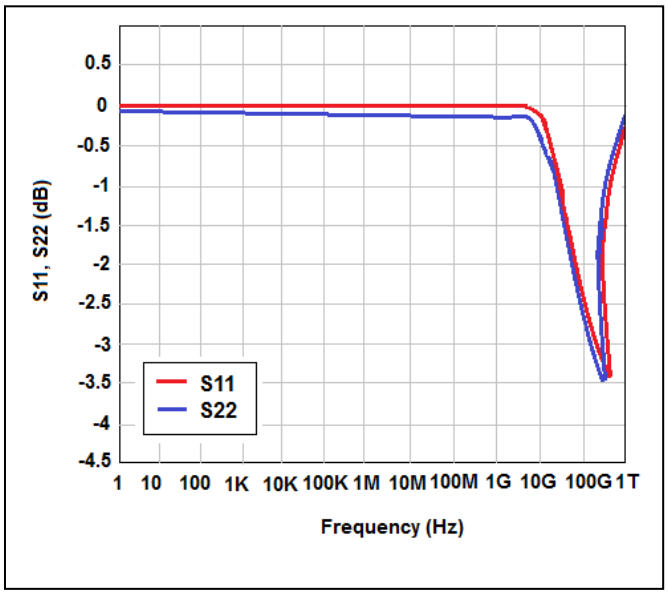


**Fig. 7:** input and output return loss $S_{11}$ and $S_{22}$

Figure 8 shows the layout of the proposed LNA, the circuit is designed in 130 nm CMOS technology. The circuit consists of two transistors, one capacitor, two inductors, and one resistor which implemented using pseudo resistor topology as shown in Fig. 9. Pseudo resistor topology is featured by high impedance. With 130 nm CMOS technology the thick-oxide PMOS transistors (PFET33) can be used to implement this pseudo resistor topology.

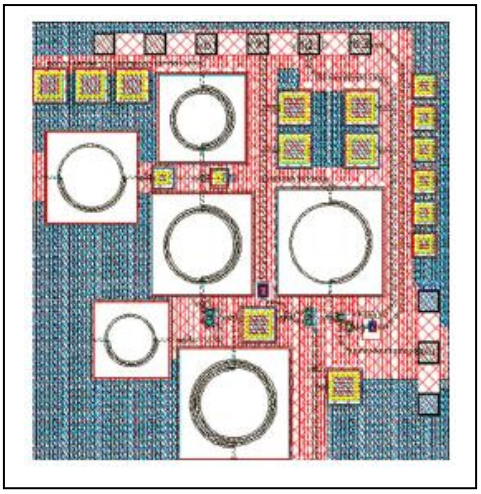

**Fig. 8:** layout of proposed LNA

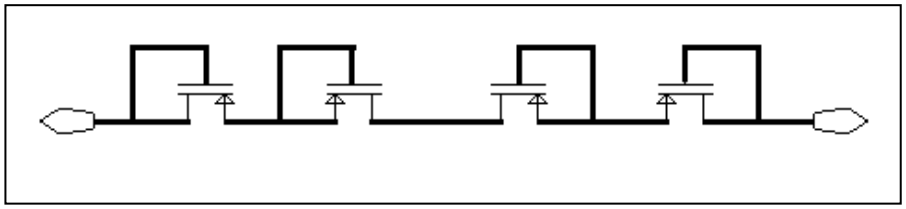

**Fig. 9:** Pseudo resistor (Rp) using (PFET33) transistors that used in the proposed layout of LNA

Table no 2 summarizes the postlayout simulation of the proposed LNA. From these results it is clear that the bandwidth of the amplifier is enhanced to 50.33 GHz due to the removing of coupling capacitor. The circuit dissipate a very low power of 0.8 mW using 1.2 V power supply. The circuit provides a gain of 15 dB

and small noise figure (NF) of 0.9 dB. The input referred third order intercept point (IIP3) is 34.66 dBm and return loss ($S_{11}$) of -1 dB. From these results, the proposed LNA is considered a good candidate for low dissipated power and ultra wideband applications.

**Table no 2.** Summary of the postlayout simulation results of the proposed LNA.

| **Parameter** | **Result** |
|---|---|
| Technology | 130 nm CMOS technology |
| Power supply ($V_{DD}$) | 1.2 V |
| Gain | 15 dB |
| Bandwidth | 50.33 GHz |
| Noise figure (NF) | 0.9 dB |
| S11 | -1 dB |
| IIP3 | 34.66 dBm |
| Dissipated power | 0.8 mW |

Table no 3 provides a comparison between the proposed LNA and the recently published LNA. As shown from the comparison the proposed technique enhanced a lot in the LNA parameters NF, $S_{11}$, IIP3 and dissipated power. The proposed LNA has the smallest power dissipation.

**Table no 3.** Table 4: performance comparison between the proposed LNA and recently published UWB LNA

| Reference | **This work** | [8]/2009 | [9]/2016 | [10]/2016 | [11]/2017 | [12]/2019 | [13]/2021 |
|---|---|---|---|---|---|---|---|
| Technology | **130 nm CMOS technology** | 130 nm CMOS Technology | 0.25 µm SIGe: C BiCMOS technology | 90 nm CMOS technology | 65 nm CMOS technology | 65 nm CMOS technology | 180 nm RF CMOS process |
| Power supply | **1.2 V** | 2.4 V | | 1.2 V | 1 V | 1 V | 1.2 V |
| Gain | **15 dB** | 20.4 dB | 10.5 dB | 20 dB | | 12.8 dB | 10.8 dB |
| Bandwidth | **50.33 GHz** | 55-62 GHz | 29.5 GHz | 24-48 GHz | 35.6 GHz | 55-64 GHz | 3.1-10.6 GHz |
| Noise figure (NF) | **0.9 dB** | 8.7 dB | 2.5-4 dB | 3.1 dB | 5.4-7.4 dB | 3.6 dB | 2.5-4 dB |
| S11 | **-1 dB** | -10 dB | -10 dB | -10 dB | | -12 dB | -10 dB |
| IIP3 | **34.66 dBm** | -12 dBm | 1.8-5.9 dBm | -3 dBm | -15.4 dBm | -6 dBm | 3.84 dBm |
| Dissipated power | **0.8 mW** | 65 mW | 24 mW | 21.1 mW | 19 mW | 8.8 mW | 6 mW |

## V. Discussion

As shown from the obtained simulated results that the proposed LNA circuitry design using diode connected load technique has a great performance compared with the others. From theseresults the noise figure of the proposed LNA is reduced to 0.9 dB compared with the traditional which reached to 7 dB. Linearity of proposed LNA is improved a lot by using diode connected load technique as diode connected load technique gives nonlinearity in a gainst direction of the nonlinearity which exist in the circuit and so the total nonlinearity of the circuit can be removed. In the proposed LNA the input referred third order intercept point (IIP3) reached to 34.66 mdB. The proposed LNA circuit dissipates minimum amount of power reached to 0.8 mW compared with the traditional circuit which consume 15.04 mW. The proposed LNA has wide bandwidth of 50.33 GHz.

## VI. Conclusion

Two common source stages using diode connected load technique LNA is proposed which suitable for low power ultra wideband applications. The circuit is designed and implemented in 130 nm CMOS technology. The reduction of the output noise is discussed due to diode connected load technique. The proposed LNA has a good parameters as low noise figure, high bandwidth, low power dissipation and high linearity. The proposed LNA improves a lot in the operation of UWB systems.

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