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Design and simulation of an asymmetrical 9-level inverter with modulation techniques

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Abstract— *For medium voltage, high power regulation the Multilevel Inverters (MLI) are attracting industry and academic researchers. MLI generates the desired output in the form of stepped waveforms with reduced harmonics. The MLI is expected to be realised using a variety of traditional topologies. Traditional MLIs have the disadvantage of requiring additional components, which increases the complexity of gate pulse production. As a result, MLI's overall costs will rise. This research proposes a hybrid topology to alleviate these drawbacks. With the increase in the number of steps in output voltage, the number of dc sources, power switching devices, converter cost, and space required is significantly reduced compared to typical MLIs. The design and simulation of a hybrid converter using several types of PWM approaches are covered in this work. This hybrid converter combines a T-Type single-phase inverter with an H-Bridge module with sub switches. The proposed construction is designed and simulated by MATLAB Simulink software. The proposed 9 level inverter circuit is designed and simulated by Equal phase angle modulation technique and half height modulation technique , THD is compared.*

Keywords: *multi-level inverter, equal phase angle modulation technique, half height modulation technique, THD*

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I. Introduction

For many years, H-bridge traditional inverters were employed in numerous industrial applications due to their simple switch configuration and ease of control. Their output is of poor quality, with more harmonic components, and their use is unsatisfactory in several applications. PWM inverters with a high switching frequency have a low efficiency and a high dv/dt stress. Traditional H-bridge inverters and Pulse Width Modulated inverters have been replaced by new multilevel inverters.

Multi-level inverter techniques are used in industrial applications to reduce voltage stress on power equipment and create high-quality output voltages. Multi-level inverters increase ac power quality by converting power in short voltage steps, which results in decreased harmonic content. When compared to a two-level output voltage waveform, the harmonic content of this output voltage waveform is substantially reduced.

In response to the conventional limitations of inverters, this paper proposes a new asymmetrical 9-level inverter design, simulated with MATLAB Simulink. Let us discuss the proposed inverter circuit design and switching operations.

II. Multilevel Inverter

Because of the well-known drawbacks of traditional two-level inverters, a multilevel inverter is required. The benefits of a multilevel inverter, as well as the basic notion of a multilevel inverter, are also explained.

Need of Multilevel Inverter

- The output voltage of two-level inverter contains more harmonics.
- PWM-VSIs operating at high switching frequencies are rarely preferred for high power applications due to considerable switching losses.

- PWM-VSIs generate Electromagnetic Interference (EMI).
- As the two-level inverters have to switch between the two extreme levels of the dc-link voltages, they are subjected to High dv/dt.
- The task of reducing harmonic content in the output voltage is addressed by the multilevel inverters.

Advantages of Multilevel Inverters

- They are suitable for high-voltage and high-current applications.
- They have reduced Total Harmonic Distortion (THD) in voltage with increased number of voltage levels.
- They can be operated with the lower switching frequency and hence the switching losses are reduced.
- They have higher efficiency.
- Power Factor is close to unity for MLIs used as rectifier.
- No Electromagnetic Interference (EMI) problem exists.
- It is possible to use power semiconductor devices of lower voltage ratings to realize high voltage levels at inverter output.

III. Design and operating modes

Figure 1 shows a single-phase multi-level inverter. This multi-level inverter is a 9-level CHB with a T-Type single phase inverter and an H-Bridge module with sub switches, as shown. Figure 1 shows the 9-Level Inverter design. Two dc sources, two capacitors, and seven switches make up the architecture of the Hybrid Cascaded H-Bridge Multilevel Inverter. This configuration is made up of a T-Type single-phase inverter and an H-Bridge module with sub switches. This setup removes the need for additional dc sources while also reducing the amount of switches necessary.

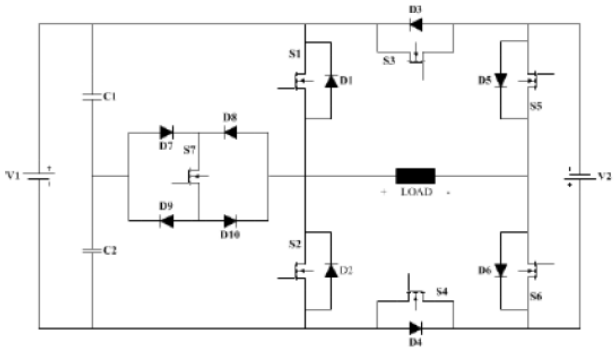

Figure 1 : 9 - level asymmetrical inverter with reduced switches.

Mode	Output Voltage V_o Volts	Switch State						
		S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	0 V	0	0	1	0	0	0	0
		0	0	0	1	0	0	0
1	+24 V	0	0	0	1	0	0	1
2	+48 V	0	0	0	1	1	0	0
3	+72V	0	0	0	1	1	0	1
4	+96 V	1	0	0	1	1	0	0
5	-24 V	0	0	1	0	0	0	1
6	-48 V	0	0	1	0	0	1	0
7	-72 V	0	0	1	0	0	1	1
8	-96V	0	1	1	0	0	1	0

Table 1: Switching table for proposed circuit

Switching Operating Modes

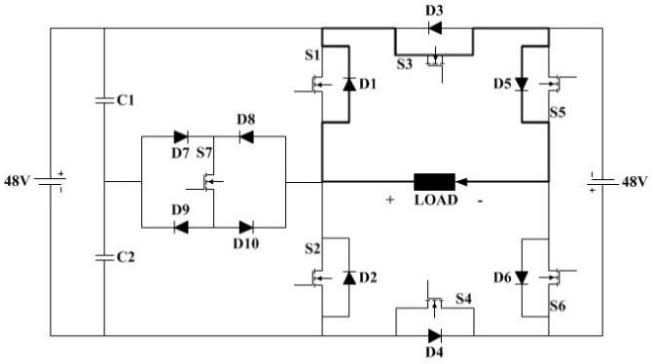

Fig 2: Mode 0 operation of the circuit for 0V level

Fig 2. shows operation for mode 0 In this mode of operation capacitor C1 and capacitor C2 will be in off condition, switche S3 will be turned ON through appropriate gate pulses. Load current Io will flow through the path D1-S3-D5-load-D1 With ouput voltage of vo = 0V.

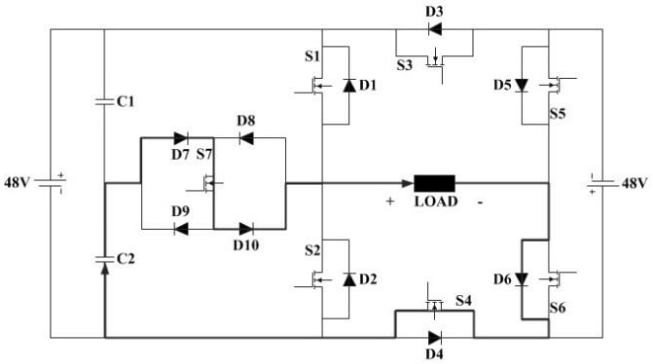

Fig 3 : Mode 1 operation of the circuit for V level

Fig 3. shows operation for mode 1 In this mode of operation capacitor C2 will act as voltage source, switches S4 and S7 will be turned ON through appropriate gate pulses. Load current Io will flow through the path C2-D7-S7- D10- Load-D6-S4- C2,With output voltage of Vo= +24V.

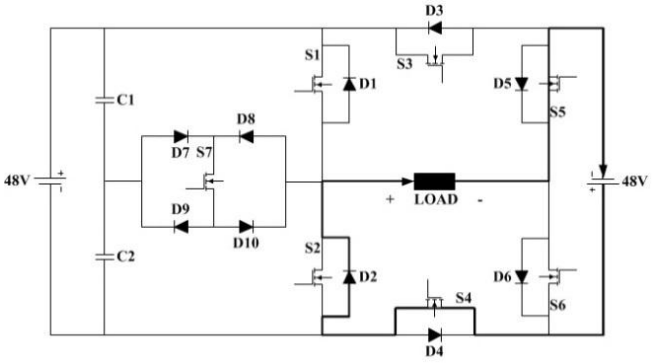

Fig 4: Mode 2 operation of the circuit for 2V level

Fig 4. shows operation for mode 2 In this mode of operation both capacitor C1 and C2 will be in off state, switches S4 and S5 will be turned ON through appropriate gate pulses. Load current Io will flow through the path V-S4-D2- Load-S5,With output voltage of Vo= +48V.

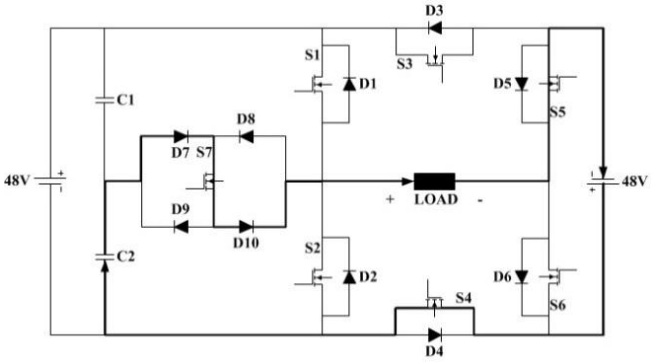

Fig 5: Mode 3 operation of the circuit for 3V level

Fig 5. shows operation for mode 3 In this mode of operation capacitor C2 will be in on condition, switches S5 and S4 will be turned ON through appropriate gate pulses. Load current Io will flow through the path C2-D7-S7-D10- Load-S5-V-S4-C2 With ouput voltage of vo = +72V.

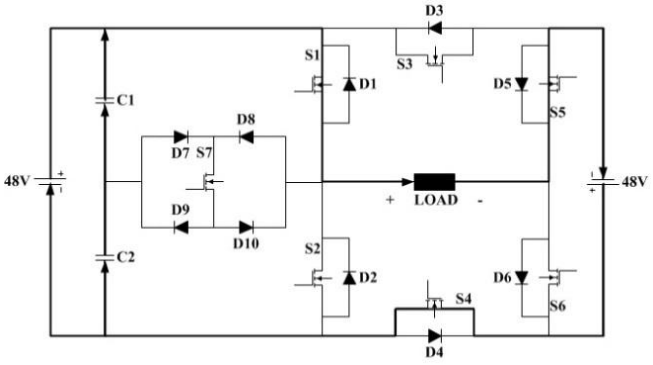

Fig 6: Mode 4 operation of the circuit for 4V level

Fig 6. shows operation for mode 4 In this mode of operation both capacitor C1 and C2 will act as voltage source, switches S5 and S4 will be turned ON through appropriate gate pulses. Load current Io will flow through the path C2-C1-S1- Load-S5-V-S4- C2,With output voltage of Vo= +96V.

Operation modes 5-8 are the exact opposite polarity for modes 1-4. The half positive cycle of modes 1-4 are configured to oppose polarities by resulting in a half negative cycle.

IV. Modulation techniques

Modulation is the process that used to switch the power electronic device from one state to other. The purpose of the modulation techniques is to generate the multilevel output waveform. Each modulation technique generates different switching pulses to achieve the desired output waveform.

Equal Phase (EP) Switching Modu1ation Technique

In this technique the switching ang1es are distributed average1y over the full complete cyc1e ranging from 0 – 360 degrees. The equation to calculate the switching angles by Equal Phase (EP) method is given by

$$Ug = g * (180/ M) \text{ where } g = 1, 2, 3, 4\ldots, 2M$$

M = Number of output voltage levels

Half height switching modulation technique method

The half height method is employed to reduce the harmonic content at the output voltage side. For M is odd, 2(M - 1) switching angles is determined for the period of 0°–90° Since the sine wave is symmetrical waveform, the positive half cycle is mirror symmetrical to its negative half cycle. We define the switching angles in the first quadrant period (i.e., 0°–90°) as main switching angles. Switching angles in second quadrant (90°-180°), third quadrant (180°-270°), fourth quadrant (270°-360°) are to be calculated.

$$\alpha i = \sin^{-1}\left[\left(i - \frac{1}{2}\right) 2/N\text{-}1\right]$$

where i=1 , 2… (N-1)/2

N= level of switching angles

.

V. MATLAB Simulink model

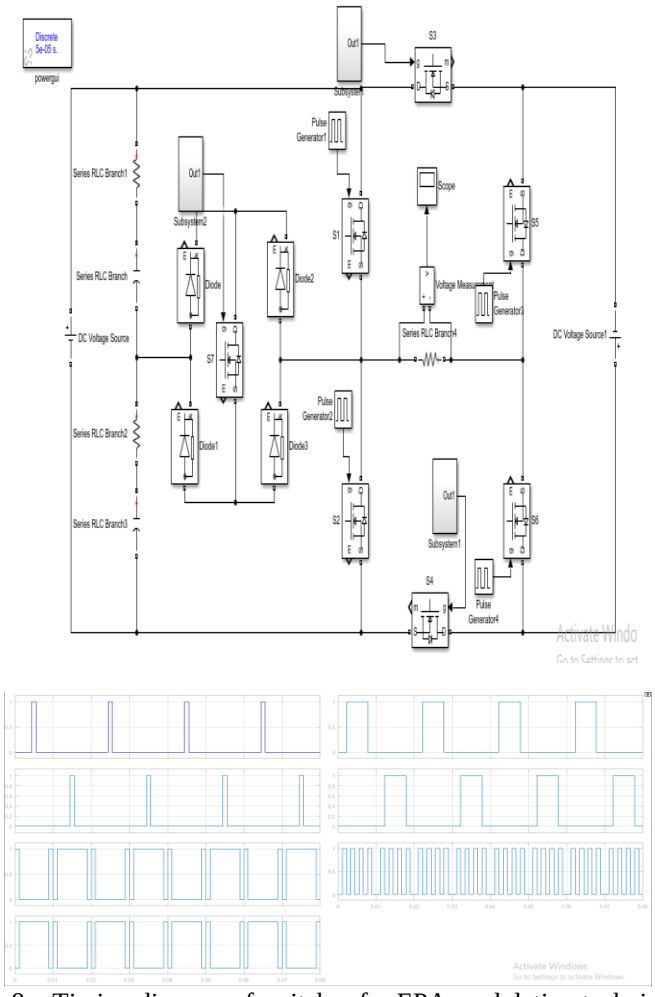

Fig 8 : Timing diagram of switches for EPA modulation technique

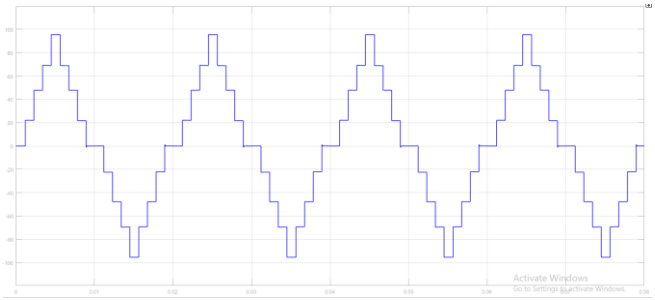

Fig 9: Output voltage waveform of asymmetric 9- level inverter circuit using EPA method

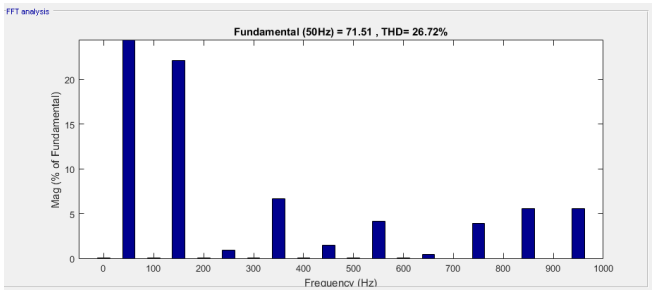

Fig 10 : FFT analysis for THD of 9 -level proposed topology using equal phase angle modulation technique.

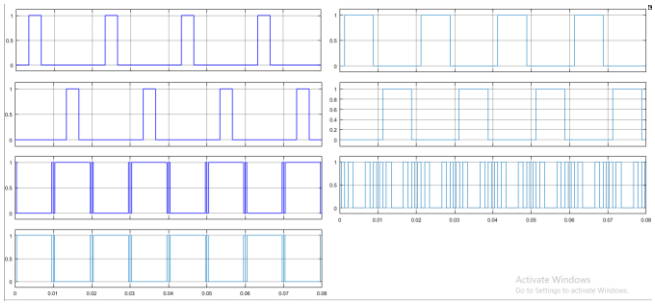

Fig 11 : Timing diagram of switches for half height modulation technique

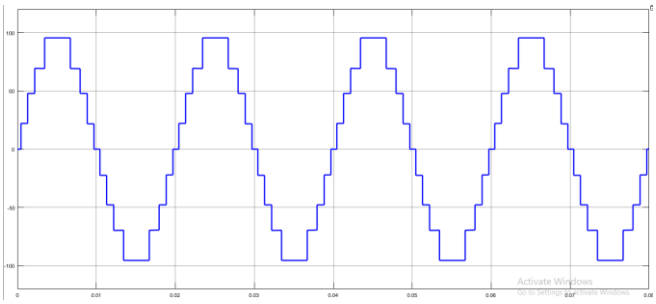

Fig 12: Output voltage waveform of asymmetric 9 level inverter circuit using half height method

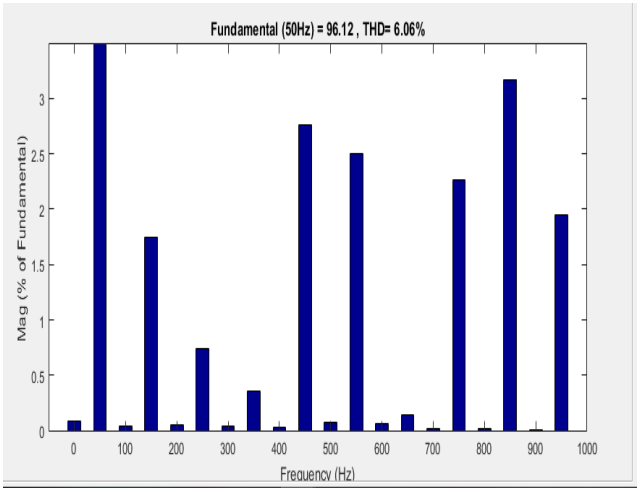

Fig 13 : FFT analysis for THD of 9 -level proposed topology using half height modulation technique

Type of circuit	Number of switches needed	Number of output voltage level
Conventional h-bridge cascaded inverter circuit	16	9
Proposed asymmetrical 11-level inverter circuit	7	9

Table 2 : Comparison table for number of switches and circuit topology.

Modulation technique	Type of load	THD % voltage
Equal phase (EP) modulation technique	*R-L Load* *R=45.3833ohms* L=1.083mH	25.21%
Half height modulation technique	*R-L Load* *R=45.3833ohms* L=1.083mH	6.03%

Table 3: Comparison table of results with Equal phase modulation technique and half height modulation technique.

VI. Conclusion

In MATLAB-Simulink, a new family of multilevel inverters has been introduced and created. When compared to typical similar inverters, it has a lower number of switches. The new topology's operation modes and switching technique are discussed. An equal phase modulation strategy is used with the aid of a pulse generator to research the THD of this model, and then a SHE modulation technique is used with the use of a pulse generator to examine the harmonic elimination of the new topology based on the theory of resultant. Traditional MLIs have the disadvantage of requiring additional components, which increases the complexity of gate pulse production. As a result, MLI's overall costs will rise. To address these flaws, this study proposes a hybrid architecture, which includes the design and simulation of a hybrid converter using several PWM approaches. This hybrid converter is made up of a single phase T-Type inverter and an H-Bridge module with sub switches. Switching functions are easily improved in this hybrid topology. The right figures and tables demonstrate the operational principle. In simulation findings, a high-quality output voltage wave is obtained. It reduces the dv/dt stresses that switches are subjected to, as well as the output voltage harmonic component. The simulation results show that the algorithm can be effectively used to eliminate specific higher order harmonics of the new topology and results in a dramatic decrease in the in the output voltage THD i.e. 6.03%.

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