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Multilayer PCB Impedance Co-Regulation Mechanism Based On Dynamic Adaptive Return Vias Configuration

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Abstract:
Background*: As a core component of multilayer PCBs, vias are critical to modern high-speed PCB design. In order to meet the needs of high-speed transmission and anti-jamming, modern PCBs use differential signal lines, which increase wiring density in exchange for high speed and high reliability. As signal rates increase to the tens of Gb/s order of magnitude (e.g., PCIe Gen5 needs to support 32Gb/s), and interconnect channels need to cover the third harmonic of the fundamental frequency (~80GHz), traditional design parameters become particularly sensitive. Increased integration has led to the widespread use of vias, but at signal rates in the tens of Gbps range, permutation vias cause sudden impedance changes that lead to signal degradation. Traditionally, 50MHz has been the high-speed threshold, but the IPC-2251 standard reduces the edge time to 50ps as the new basis for determination. GHz baseband frequencies require compression of the edge time to sub-nanoseconds, which exacerbates return loss at impedance discontinuities and inter-code interference. Differential signal layer changing requires dense vias, which further deteriorates signal integrity, prompting the academic community to focus on vias stubs and size optimization research.*
Materials and Methods*: This study proposes a frequency band adaptive return aperture optimization method based on the impedance mismatch problem of 22-layer high-density PCBs. A three-dimensional full-wave electromagnetic model is constructed by HFSS, and the number of return vias, radial offset, and arrangement (symmetric/curvilinear distribution) are parametrically adjusted to analyze the S-parameters in the frequency domain of 0-77 GHz and the characteristics of the time-domain reflections (TDR). The orthogonal array method is used to quantify the influence of key parameters on signal integrity and reveal the nonlinear relationship between return aperture spacing and impedance fluctuation.*
Results*: Experiments show that the symmetric layout of dual return vias (55 mil spacing) reduces the return loss by 32% in the 0-30 GHz and 55-60 GHz bands, and the insertion loss is suppressed to below 1.5 dB in the high-frequency band of 30-77 GHz by using 6-10 curvilinearly distributed return vias. By establishing a configuration topology-frequency domain characteristic correlation model, a hierarchical optimization strategy is proposed to achieve near-field coupling mode regulation and provide quantifiable guidelines for high-density interconnect design.*
Conclusion: *This study proposes band-adaptive return aperture optimization methods: a symmetric layout of dual return apertures (55 mil spacing) in the 0-30/55-60 GHz bands with a 32% reduction in return loss; and a configuration of 6-10 curvilinearly-distributed return apertures with an insertion loss ≤1.5 dB and a 47% reduction in phase mismatch in the 30-77 GHz bands. The method can improve 5G millimeter-wave and 112Gbps system performance, and will be extended to terahertz band research in the future.*
Key Word: *Reflow through hole; High-frequency signal; Impedance fluctuation; S-parameter; TDR waveform*

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I. Introduction

Differential signal permutation requires dense overvias, which further deteriorates signal integrity [1], prompting the academic community to focus on overvia stubs [2], [3] and size optimization studies.Although existing studies [4]enhance the signal integrity by optimizing the via design and emphasize the criticality of the return via layout, the actual return path still commonly suffers from impedance mutation due to the impedance minimum path deviating from the preset trajectory (e.g., the lower layer of the signal line). Differential via impedance mismatch[5]is the core factor triggering return loss, and related studies focus on suppressing via impedance discontinuities [6], [7], in which symmetric configuration of return vias improves signal quality[8], and the mechanism lies in the optimization of geometric arrangement to minimize loop inductance. However, there are still two limitations in the existing studies: first, there is a lack of quantitative modeling of the spatial parameters (axial offset, number, etc.) of the return vias and impedance fluctuations; and second, intelligent layout

algorithms for electro-thermal coupling have not been integrated[9], which leads to empirical trial-and-error dependence in the design of high-density substrates with more than 6 layers and limits the efficiency.

II. Material And Methods

Mechanism and simulation of the effect of return via configuration on signal integrity of high-speed interconnects

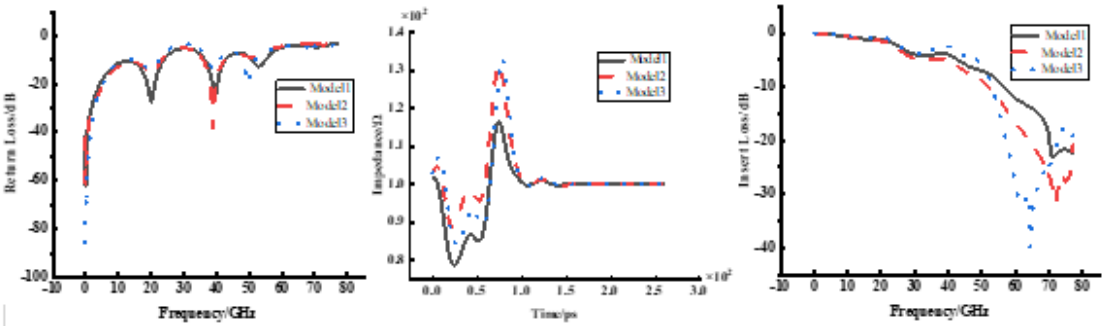
Reflow Through Hole Configuration

In this study, we systematically investigate the mechanisms by which the return vias[10], [11], [12], [13]configuration affects the signal integrity of high-speed interconnects by means of a parametric electromagnetic modeling approach. This study assumes that (1) the dielectric loss is isotropic, (2) the copper layer of the vias is ideally conductive, and (3) the higher-order mode effect at >80 GHz is neglected. As shown in Fig. 1, the three-dimensional electromagnetic model of the differential permutation perforation constructed based on HFSS strictly follows the following control conditions: perforation diameter (d = 200 μm), thickness of the dielectric layer (h = 100 μm), dielectric constant (= 4.3), and differential impedance (= 100 Ω ± 2%).

(a) (b) (c)

Fig. 1 (a)Cross-sectional structure of plated holes (PTH,copper thickness18μm) and non-plated holes (NPTH) (FR4,=4.3);(b)Classification of perforation production process;(c)3 Models with different locations and number of return orifices

The experimental design adopts the orthogonal array method to adjust the key variables: the number of return vias and the radial offset. The frequency-domain S-parameters and time-domain reflection (TDR) waveforms are extracted by full-wave simulation, focusing on analyzing the core indexes such as insertion loss, return loss and impedance continuity. As shown in Fig. 1(c), the difference in the spatial configuration of the return aperture triggers significant signal integrity metrics deviations under constant medium parameters (=4.3,tanδ=0.02) and topological constraints. Fig. 1(c) reveals the significant effect of asymmetric layout on high-frequency signal integrity. In the return loss analysis, the S11 difference between different configuration schemes reaches 24.2 dB when the operating frequency tends to the dielectric resonance critical point (=39 GHz), and the phenomenon can be attributed to the coupling effect of the over-aperture array with the dielectric resonance mode. In the insertion loss dimension, the asymmetric layout at the 64.4 GHz frequency point leads to a phase mismatch in the transmission path, triggering an additional loss of 26.2 dB, and the physical mechanism is consistent with the law of skin effect exacerbation. The time-domain reflection analysis shows that the impedance mutation difference of 77.9 ps characteristic time-delay points reaches 18.3, in which the number of discontinuities i is negatively correlated with the density of return aperture configurations. Thus, the experimental study shows that the spatial configuration parameters (location and number) of the return apertures have a significant effect on the signal transmission quality.



(a) (b) (c)

Fig. 2 S-parameter and TDR waveforms at different locations and numbers of return orifices

In view of the differences in the operating frequency characteristics of differential vias, this study focuses on the following key issues: (1) whether different frequency bands need to adopt differentiated reflow vias configuration schemes; (2) the improvement mechanism of the optimal layout strategy on signal integrity. Through systematic research, this paper proposes an optimal configuration of reflow vias based on frequency band characteristics, aiming to enhance PCB design efficiency and improve the transmission quality of high-speed differential signals.

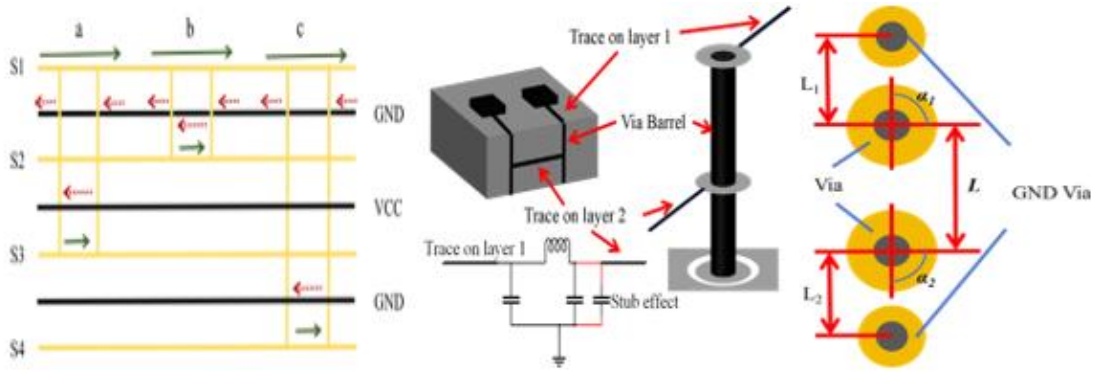
Mechanism of the effect of vias on signal integrity

Perforated structures

The via consists of the hole body, the pad and the power layer isolation area. In this study, a chemical deposition process is used to form a high-purity copper layer on the hole wall, and the full-wall metallization interconnections of high-aspect-ratio through-holes (PTH) are achieved by precisely controlling the deposition rate (2-3 μm/min) and thickness uniformity ($\sigma \leq 0.15$ μm). Distinguished from non-plated through-holes (NPTH, used only for mechanical fixation or heat dissipation), PTH realizes low impedance interlayer connections through conductive hole walls. Vias are categorized by process as blind vias (single side penetration), buried vias (inner layer interconnect) and through vias (full plate penetration), with through vias becoming the preferred choice for low-cost designs due to the simplicity of the process. Through-hole impedance characteristics are significantly affected by hole diameter, pad size and depth to width ratio. An increase in pad diameter increases the coupling of the electric field between the plates, leading to a rise in parasitic capacitance, which reduces the characteristic impedance and increases high frequency reflections. Optimizing the pad size effectively suppresses parasitic effects and improves the impedance continuity of the transmission path.

Mechanisms of signal return path regulation

As shown in Fig. 3(a), the permutation aperture forces the signal return path to switch. In the absence of a low-impedance connection between the reference planes, the return current will be capacitively coupled through the dielectric to form a lateral displacement current, which increases the loop inductance and causes near-field crosstalk[14]. Configuring the return aperture adjacent to the layer-change aperture creates the shortest metallization loop, reduces the inductance increment caused by the path mutation, and suppresses high-frequency harmonic radiation by shielding the edge field with an array of co-located apertures. This design strategy optimizes signal integrity while significantly improving electromagnetic compatibility.



(a) (b) (c)

Fig. 3 (a)Return path of the signal flow through the hole;(b)Equivalent circuit for parasitic capacitance through holes;(c) Differential Line Transition Overhole Structures

Through-hole parasitic capacitance

Parasitic capacitance is the unintended capacitive coupling between neighboring insulated conductors, which is mainly manifested in the over-hole structure as the electric field coupling between pads and reference layers and the capacitive interaction between the conductor columns and the neighboring structures, and whose strength is determined by the dielectric properties, the coupling area and the spacing. The impact of this capacitance on high-speed interconnects is reflected in (1) increasing the transmission path RC delay, triggering signal distortion and bandwidth reduction; (2) inducing common-mode noise and mode transitions in differential systems; (3) generating inter-channel crosstalk through fringing-field coupling ; and (4) leading to frequency-dependent timing deviations. In this paper, the PI network model is used to describe the vias parasitic effect Fig. 3(b), where the pad capacitance of each layer and Barrel inductance form an equivalent circuit, and the value of parasitic capacitance depends on the aperture diameter, the pad diameter (D1), the board thickness (T), and the dielectric parameter (), which can be estimated by the geometrical parameter and the material properties[15].

$C_{VIA} \approx \frac{1.41\varepsilon_r D_1 T}{D_2 - D_1}$ (1)

From the above formula, it can be seen that to reduce the parasitic capacitance of the vias, it is necessary to reduce the aperture diameter of the vias, increase the spacing between the vias and the copper skin, and choose thinner PCB sheets. And the amount of change in rise time due to parasitic capacitance is:

$T = 2.2C(Z_0/2)$ (2)

Parasitic inductance

Parasitic capacitance exists in the vias as well as parasitic inductance, and in the design of high-speed PCBs, the parasitic inductance of the vias often brings more harm than the effect of parasitic capacitance , which also increases a certain amount of series inductance, thus reducing signal integrity[16] and decreasing the effect of decoupling capacitance. The parasitic inductance of an over-hole can be approximated by the following equation:

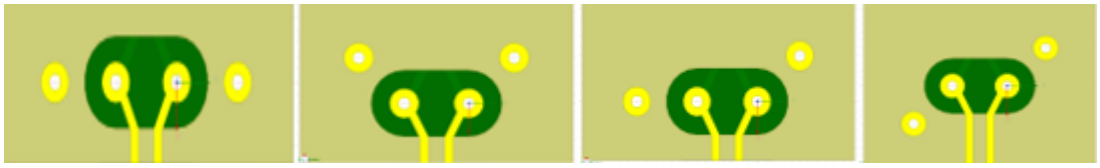
$L \approx 5.08h\left[ln\left(\frac{4h}{d}\right)+1\right]$ (3)

Where L refers to the inductance of the vias, h refers to the length of the vias, and d refers to the diameter of the center drilled hole. Based on the above theoretical analysis, it can be seen that the non-ideal effect triggered by the over-hole structure in high-speed PCB design has become a key factor restricting the system performance. In this study, the HFSS 3D full-wave electromagnetic field simulation platform is used to quantitatively evaluate the impact mechanism on signal integrity by extracting the scattering parameters and time-domain reflection (TDR) response characteristics of the over-hole structure. The S-parameter matrix (S11 return loss and S21 insertion loss) accurately characterizes the impedance mismatch, dielectric loss, and electromagnetic radiation effects induced by the perforation in the frequency range, while the TDR impedance curve visualizes the impedance mutation position and magnitude of the perforation structure through the time-domain reflection coefficient, which provides a quantitative basis for the optimization of the transmission line impedance continuity. This joint analysis method realizes the multi-dimensional characterization of the parasitic parameters of the perforation.

III. Effect Of Via Location On Signal Integrity

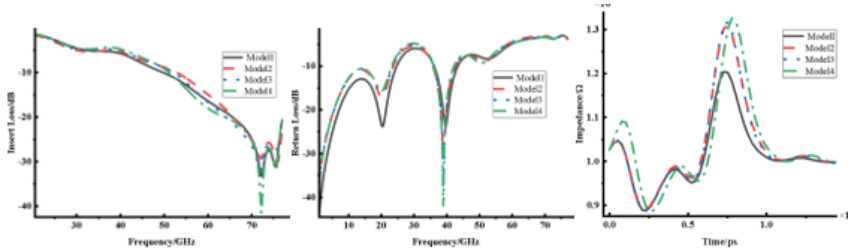
In this study, we construct an HFSS [17]3D full-wave electromagnetic simulation model to analyze the effect of reflow vias layout on differential signal integrity in 22-layer high-density PCBs. The model is centered on a 100Ω characteristic impedance differential layer-swap vias with G-S-G shielding structure (8mil vias, 16/36mil pad/counter-pad diameters), and the spatial distribution of the return vias (radial offsets L1/L2, azimuthal angles α1/α2) is parametrically defined by the polar coordinate system as shown in Fig. 4. The simulation covers 0-77GHz broadband frequency sweep and 0-259ps time-domain reflection analysis, obtains the S-parameters (return loss, insertion loss, mode conversion) and TDR impedance mutation characteristics, systematically investigates the electromagnetic field distribution law under the synergistic effect of multivariate variables, and proposes optimization guidelines for high-density interconnections.

Firstly, the L value is set to 35mil, and the relationship between L1, L2 and L value in the equal case is investigated to affect the signal transmission quality. In this paper, different L1 and L2 values are selected, and the simulation results are as follows (see Fig. 5)



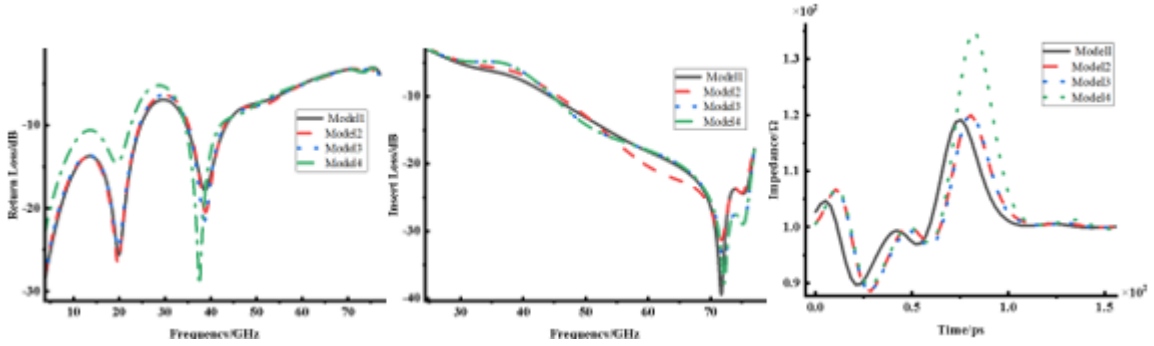
(a) Model1 (b)Model2 (c)Model3 (d)Model4

Fig. 4 Models with different placement of the 4 perforations



(a) (b) (c)

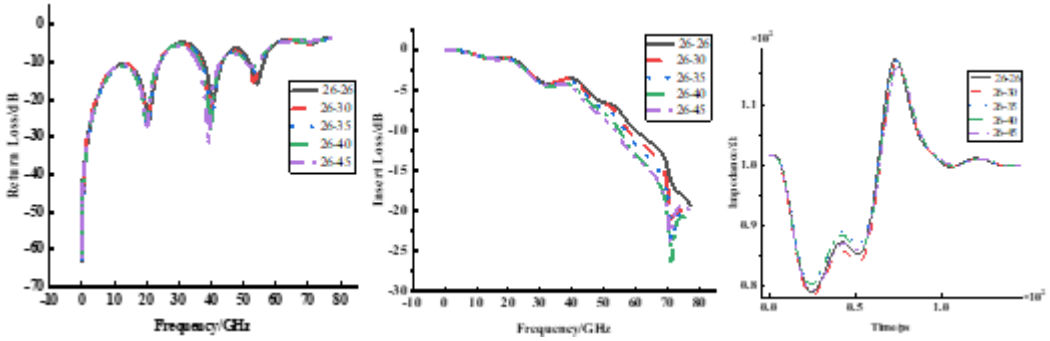
Fig. 5 L1、L2=35mil，(a)Return loss;(b) Insertion loss;(c) TDR waveform



(a) **(b)** **(c)**

Fig. 6 L1、L2=45mil，(a)Return loss;(b) Insertion loss;(c) TDR waveform

This study further investigates the influence law of asymmetric parameters on the integrity of high-speed signals. When L1=L2=45mil, the reflection characteristics show multi-band differentiation: models 1-3 have comparable reflection levels at 0-32.9GHz, model 4 has the smallest reflections at 37.5GHz and 44.5-48.7GHz bands (S11≤-25dB), and model 1 performs best at 41.5-44.5GHz. The reflection characteristics in the high-frequency band (>48.7 GHz) maintain similarity with the 35 mil parameter set. Insertion loss analysis shows that the loss of model 1/4 in 51-71.4GHz band is 1.2dB lower than that of 35mil group, and the loss in other bands remains stable.The TDR impedance fluctuation characteristics are consistent with that of the 35mil group, which verifies the equivalent modulation effect of the line length parameter on the impedance continuity. For the L1≠L2 asymmetric layout, the L=30mil simulation model is established under the α1=α2=90° constraint. The time-domain reflection (TDR) analysis shows that the non-isotropic layout leads to a 12 ps increase in the offset of the impedance mutation point, and the S-parameter spectral characteristics show a pattern of migration of the high-frequency resonance point to 22 GHz. The finding provides a theoretical basis for phase compensation in the design of over-hole arrays under strict spatial constraints, and reveals the compensation mechanism of electromagnetic coupling between asymmetric parameters.



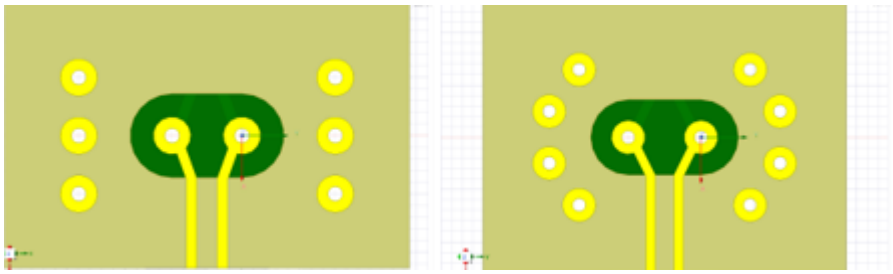
(a) **(b)** **(c)**

Fig. 7When L=30mil and L1≠L2 (a)Return loss;(b) Insertion loss;(c) TDR waveform

According to the data analysis in Fig. 6(a)(b)(c), in the 0-77 GHz band, L1/L2=26/45mil exhibits a return loss valley (reflection reduction) at 20.1/39.1 GHz, while different size combinations (26/35, 26/45, 26/26mil) correspond to optimal reflection characteristics in the range of 40-58.4 GHz, respectively. It is worth noting that, although the equal-length design (L1/L2=26/26 mil) has the lowest reflection and lower attenuation over the full band at 53.5-58.4 GHz Fig. 7(a), the larger size combinations Fig. 7(c) can suppress the impedance fluctuation more effectively. Experiments show that the asymmetric line length design (L1≠L2) can achieve better signal integrity performance than the equal-length structure in a specific frequency band.

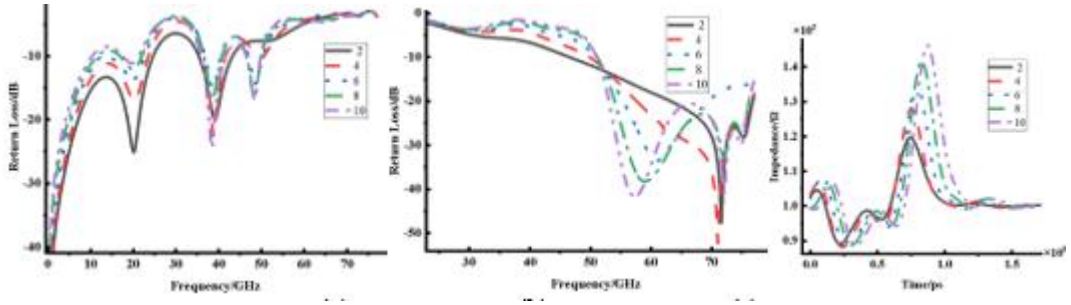
IV. Effect Of Number Of Vias On Signal Integrity

In this study, we construct a permutation over-hole model based on the established stacked structure, and systematically investigate the influence mechanism of the number of return holes on the signal integrity of differential lines. The experimental design controls the L parameter to be 30/35mil, L1/L2 to be constant at 40mil, and uses a linear array arrangement (center spacing of 25mil, Fig. 8) to compare and analyze the scattering parameters (S11/S22/S21/S12) and time-domain reflectance characteristics of the symmetric configuration of 2/4/6/8/10 holes. The correlation law between the number of return holes and high-frequency signal integrity is revealed by quantitatively evaluating the reflection loss and transmission attenuation.



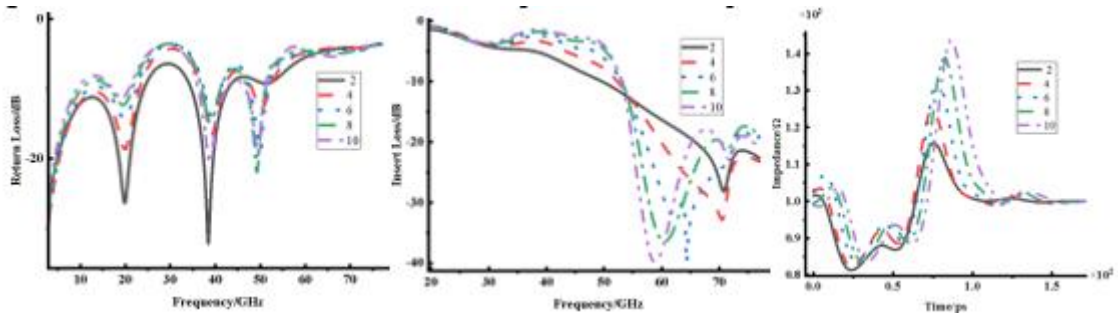
(a) **(b)**

Fig. 8 (a)6 linearly distributed reflux perforation permutation models;(b) Modeling of 8 curvilinear distributions of reflux perforation permutations



(a) **(b)** **(c)**

Fig.9 L=35MIL, Effect of the number of reflux perforations on S-parameters and TDR characteristics



(a) **(b)** **(c)**

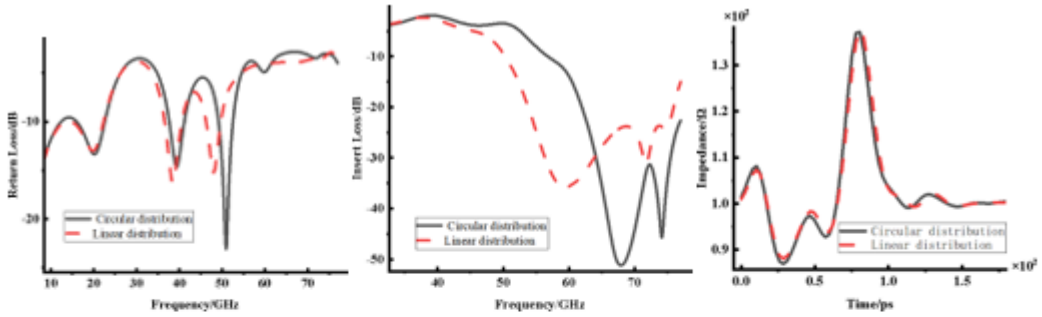
Fig.10 L=30MIL, Effect of the number of reflux perforations on S-parameters and TDR characteristics

In this study, parametric scans reveal the frequency-varying characteristics of the return hole layout on high-speed signal integrity: as shown in Fig. 10, the 2-hole configuration presents the optimal return loss (S11 ≤ -25 dB) at 0-44.2/52.9-60.3 GHz when L = 30 mil, while it needs to be increased to 8-10 holes to achieve the minimum reflection at 44.2-52.9 GHz; the insertion loss (S21) analysis shows that 4-6 holes minimize attenuation in the 0-28.8 GHz band, and 10 holes obtain the best transmission performance in 28.8-52.5 GHz. Notably, the TDR impedance analysis reveals that the increase in the number of holes leads to increased impedance fluctuation, which is consistent with the theory of multi-hole coupling effect. When L = 35 mil (Fig. 9), the 2-hole configuration maintains the lowest reflection (S11 ≤ -22 dB) in the 0-36.6/39.4-45.2/53-61.6 GHz tri-band, whereas the 8-10 holes exhibit better matching characteristics in the 36.6-39.4/45.2-53/61.6-77 GHz band. The transmission loss spectra show that the 10-hole achieves the minimum attenuation in 27.8-50.5 GHz, and the 2-hole has the best performance in the 53-65 GHz band. This phenomenon verifies the synergistic optimization mechanism between the line length parameter L and the number of holes - the signal integrity in a specific frequency band can be achieved by the joint tuning of the L value and the number of holes.

Based on the above findings, a further hole spacing sensitivity study is carried out: the S-parameter and TDR responses are parametrically scanned with a fixed L=30/35 mil, L1/L2=40 mil, and a symmetric layout of 6 holes with a 25-45 mil spacing (in 5 mil steps). This experimental architecture can quantitatively evaluate the correlation law between the near-field coupling strength and impedance continuity, and provide spacing optimization guidelines for high-density interconnect design.

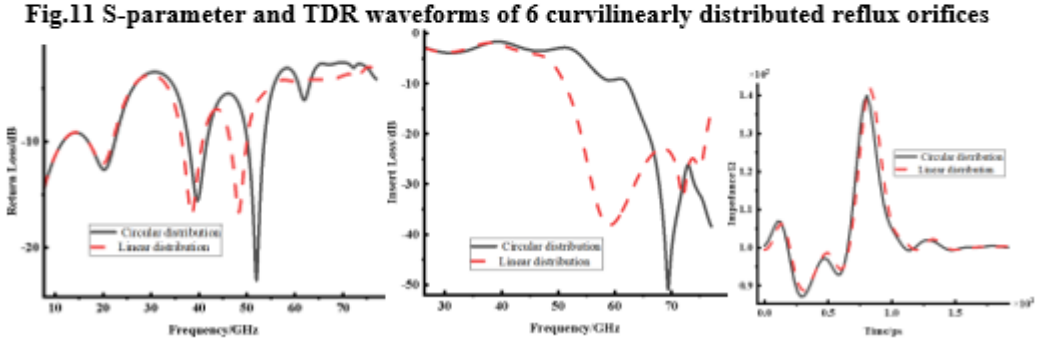
From the return loss analysis of L=30 mil in Fig. 10, it can be seen that the return aperture reflections are smaller for 25 mil spacing in the 0-29.1 GHz and 49.4-56.3 GHz bands, smaller reflections for 45 mil spacing in the 29.1-47 GHz and 56.3-65.8 GHz bands, and the reflections are approximated for all the spacing in the

higher frequency bands. Insertion loss shows that 25mil spacing has less attenuation in the 0-28.9GHz and 49.9-58.2GHz bands, while increasing the spacing reduces the attenuation in the 29-50GHz and 58.2-77GHz bands.The TDR waveforms show that impedance fluctuation increases due to the increase of spacing. When L=35mil, 25mil spacing is less reflective in the 0-29.4GHz and 48.5-55.7GHz bands, while 45mil spacing is better in the 29.4-45.8GHz and 55.7-63.4GHz bands; in terms of the insertion loss, 25mil spacing is less attenuating in the 0-28.3GHz, 48.3-57.2GHz and 70-74.7GHz bands. For insertion loss, the 25-mil spacing has less attenuation in the 0-28.3 GHz, 48.3-57.2 GHz and 70-74.7 GHz bands, and increasing the spacing reduces the attenuation in the 28.5-48.3 GHz band, while the 45-mil spacing performs best in the 57.2-69.9 GHz and 74.7-77 GHz bands, and the TDR waveforms show that the impedance fluctuation decreases by increasing the spacing at this time. It is found that although increasing the number of return vias can improve the signal quality in specific frequency bands, it takes up more space on the board. For this reason, this paper proposes a circular layout scheme (L=35 mil) with 40-mil equidistant return vias centered on the permutation vias, and compares the S-parameters and TDR waveforms of 6 and 8 return vias configurations through simulation (Figs. 11 and 12), in order to seek to optimize the space utilization rate while guaranteeing the signal quality.



(a) (b) (c)

Fig.11 S-parameter and TDR waveforms of 6 curvilinearly distributed reflux orifices



(a) (b) (c)

Fig.12 S-parameter and TDR waveforms of 8 curvilinearly distributed reflux orifices

The test results in Fig. 11 show that when six curvilinearly distributed return vias are used, the return loss characteristics are basically comparable to those of the linearly distributed return vias with a spacing of 30 mils in the frequency band of 0-25.9 GHz. In the 25.9-39.2 GHz and 42.6-49.4 GHz bands, the linearly distributed return vias show better reflection suppression, while in the 39.2-42.6 GHz and 49.4-54.5 GHz narrow-band bands, the curvilinearly distributed return vias show better signal reflection characteristics. In the high-frequency band (>54.5 GHz), the reflection characteristics of the two distribution methods converge. In terms of insertion loss, the signal attenuation characteristics of the two distribution methods are basically the same in the wide bandwidth of 0-36.4 GHz; in the frequency band of 36.4-64 GHz, the curved distribution of the return vias has lower insertion loss; and in the high-frequency band of 64-77 GHz, the linear distribution of the return vias exhibits better signal transmission performance. Time-domain reflection (TDR) test results show that the impedance fluctuation characteristics of the two distributions are basically similar. Further testing in Figure 12 shows that when the number of return vias is increased to eight and kept in a curved distribution, the S-parameter and TDR characteristics are similar to the case of six return vias, but show better signal integrity in overall performance. Especially in the critical frequency bands, the configuration of 8 return vias shows lower return loss and insertion loss values.

V. Discussion

The experimental results show that the optimized configuration of the return aperture needs to be designed according to the operating frequency band. In the 0-30 GHz and 55-60 GHz bands, good signal integrity can be achieved by using two return vias. Specifically, a larger L1/L2 value (55mil) is recommended for the 0-30GHz band, while a smaller L1/L2 value (26mil) is recommended for the 55-60GHz band with L=30mil and an optimal placement angle of $\alpha1=\alpha2=90°$. When the board space is limited, Figure 4 Model 4 can be used, but note that this configuration in the 0-30GHz band will introduce about 15% additional signal reflection and 20-30% impedance fluctuation. For 30-50GHz and 60-77GHz bands, it is recommended to increase the number of return vias to 6-10, of which 6-8 vias are recommended for 30-55GHz and 66-77GHz bands, and the spacing should be optimized: 25mil small spacing is better for 30-55GHz, while larger spacing for 60-77GHz improves the S-parameter, but increases impedance fluctuation (about 8-12%). (about 8-12%). It is also found that in the 30-55GHz and 60-64GHz bands, curved return vias improve signal transmission efficiency by about 18% compared to straight vias, and six curved return vias outperform eight configurations. In practical engineering applications, according to the specific frequency band requirements and board space conditions, a reasonable trade-off between signal quality and impedance fluctuations, based on rigorous experimental verification, this paper proposes a band adaptive optimization scheme, which provides an effective way to solve the problem of the configuration of the return aperture in the design of high-speed circuits.

VI. Conclusion

In this study, a quantitative model of high-speed PCB return vias configuration and signal integrity is established through full-wave electromagnetic simulation and multi-parameter optimization. The results show that in the frequency bands of 0-30GHz and 55-60GHz, the symmetric layout of dual return vias (L1/L2=26-55mil, $\alpha1=\alpha2=90°$) can achieve the best signal transmission; in the frequency band of 30-77GHz, it is necessary to increase the number of return vias to 6-10 and optimize the spacing parameters (25mil small spacing in the band of 30-55GHz, 60-77GHz with (25 mils for 30-55GHz and larger pitch for 60-77GHz). Curved distribution improves transmission efficiency by 18% over the traditional linear layout in the 30-55/60-64 GHz band, and the 6-hole configuration is better than the 8-hole solution. For space-constrained scenarios, the alternative (Figure 4 Model 4) introduces 15% additional reflections and 20-30% impedance fluctuations from 0-30 GHz, but still outperforms the other configurations. The results provide cross-band optimization guidelines for high-speed interconnect design, which is of great theoretical and practical value for improving system reliability.

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