IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676, p-ISSN: 2320-3331, Volume 20, Issue 3 Ser. II (May. – June. 2025), PP 22-47
www.iosrjournals.org

Influence of Parasitic Parameters on Switching Characteristics in Single and Paralleled Silicon Carbide Power MOSFETs

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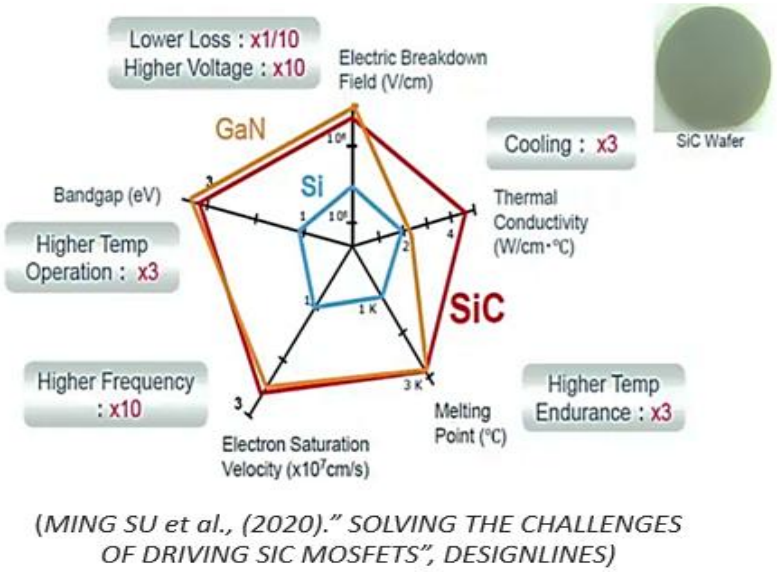
Abstract: *This research evaluates the switching performance of silicon carbide (SiC) transistors compared to silicon (Si) transistors through a double pulse test. The performance was analyzed by measuring switching losses, di/dt, overshooting and switching times. The results demonstrated that switching losses, as well as rise and fall times, are reduced by half in SiC transistors. However, some overshoot in voltage and current waveforms was observed due to the high switching speed of SiC transistors. Subsequently, the impact of parasitic capacitive and inductive elements on the switching performance and switching losses in SiC transistors was studied across various values. The findings revealed that these parasitic components significantly affect the current balancing among SiC transistors in parallel driving circuits, with a recorded current difference of up to 6 A between transistors due to variations in internal capacitor values and the inductive effects resulting from current changes over time in the transistor's terminal paths. Simulation was conducted using LTspice software. In conclusion, the research results were summarized, and conclusions regarding the impact of internal elements on transistor performance were presented.*

Keywords: *switching losses, static current, dynamic current, Double pulse Testing, Parasitic inductance, Parasitic capacitance, current balancing, Parallel SiC MOSFET.*

Date of Submission: 28-06-2025 Date of Acceptance: 10-07-2025

I. Introduction

A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) based on silicon have been one of the key components used in power electronics applications for decades. However, with the advancement of semiconductor manufacturing technology in recent years, silicon carbide (SiC) transistors have emerged, offering remarkable improvements in electrical characteristics. This has positioned SiC transistors at the forefront of a variety of industrial applications such as electric vehicles, renewable energy projects, network infrastructure, energy storage systems, and other medium- to high-power electronics applications.



(MING SU et al., (2020)." SOLVING THE CHALLENGES OF DRIVING SIC MOSFETS", DESIGNLINES)

Figure (1) Advantages of GAN and SiC Mosfets compared to Si Mosfets.

SiC field-effect transistors attract attention due to their distinct set of characteristics compared to their silicon-only counterparts. They feature higher breakdown voltages, greater switching speeds, and lower thermal losses, switching losses, on-resistances, and gate drive requirements (total gate charge) compared to silicon-based transistors. This makes SiC transistors suitable for switching applications at high frequencies and elevated temperatures.

In power electronics applications, multiple transistors are often connected in parallel to ensure a larger current flow through the loads. The parallel connection of SiC transistors results in a lower equivalent resistance for the circuit, contributing to reduced conduction losses and improved switching efficiency. Additionally, driving these transistors in parallel allows for the distribution of total current across multiple devices, helping to manage and reduce thermal dissipation while providing a larger load current, thus enabling operation at higher power levels and frequencies. Despite these advantages, driving SiC transistors in parallel poses significant challenges due to the unequal and unbalanced sharing of load current among these transistors. This imbalance arises from manufacturing variations such as discrepancies in parasitic capacitance values between the transistor terminals (source, drain, and gate) and differences in on-resistance for each transistor. These factors significantly impact the effectiveness of the switching process due to the variations in currents among the transistors, creating challenges that cannot be controlled during the manufacturing phase.

To enhance the performance of controlling turn-on and turn-off processes and balancing losses among these transistors, appropriate design considerations must be taken into account during the implementation and design of the circuits responsible for driving the gates of these parallel transistors. These considerations should address the manufacturing variations in transistor structure while ensuring balanced current sharing among the parallel transistors.

Switching losses vary according to the turn-on and turn-off times of the transistor, which correspond to its switching speed and the amount of current flowing during those times. Some gate driver circuits rely on slowing down the switching speed by using a relatively large gate resistor to balance turn-on and turn-off speeds. While increasing the switching speed can reduce switching losses, it may also lead to undesirable overshoot in voltage and current waveforms. Conversely, reducing the switching speed will inevitably increase switching losses; therefore, a specific strategy is required to balance switching speed and losses while ensuring balanced currents among all transistors being driven in parallel. This balance positively impacts load driving performance.

In this study, we present a comparison of electrical characteristics between two types of field-effect transistors: one based on silicon and the other based on silicon carbide technology. We will illustrate the impact of variations in parasitic elements on current sharing among parallel-connected transistors.

The study classifies the types of current sharing imbalance between transistors into two categories: static and dynamic. The static imbalance is due to the asymmetry in the on-resistance associated with the threshold voltage, which is affected by the junction temperature in the transistor. The dynamic imbalance arises from

transient switching processes, differences in gate turn-on delay times, and the rate of change of current during the Miller current flow. These factors lead to switching losses, sudden changes, and overshoots in voltages and currents during the turn-off and turn-on phases.

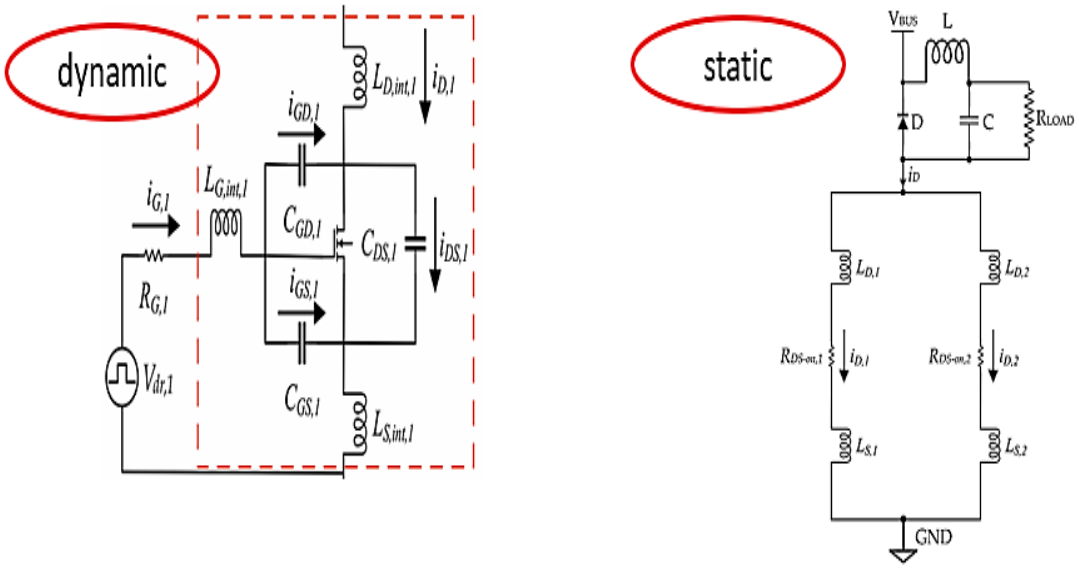


Figure (2) Factors affecting the process of controlling the performance of the switching process and balancing currents between transistors _ Static and Dynamic States.

2- Comparison of Switching Behavior between Silicon Carbide (SiC MOSFET) and Silicon (Si MOSFET):

Double Pulse Test (DPT) is a test method to measure switching performance and evaluate dynamic behavior and power losses during turn off and turn on Sic Mosfet. the goal of this test is to measure the dynamic characteristics of the transistor, such as response time, losses, and the ability to handle high currents.

The first pulse is used to turn on the transistor (convert it to the "ON" state) and determine response time. It provides an initial behavior analysis of how the transistor responds to voltage and current changes at startup. While the second pulse works on Performance evaluation in operating state, The second pulse is used after the transistor is turned on to evaluate its performance in continuous operation, measure the time it takes for the transistor to go from the "ON" state to the "OFF" state when the gate voltage is removed.

So, the two pulses help provide a comprehensive picture of transistor performance under different operating conditions, facilitating design optimization and better efficiency in energy applications.

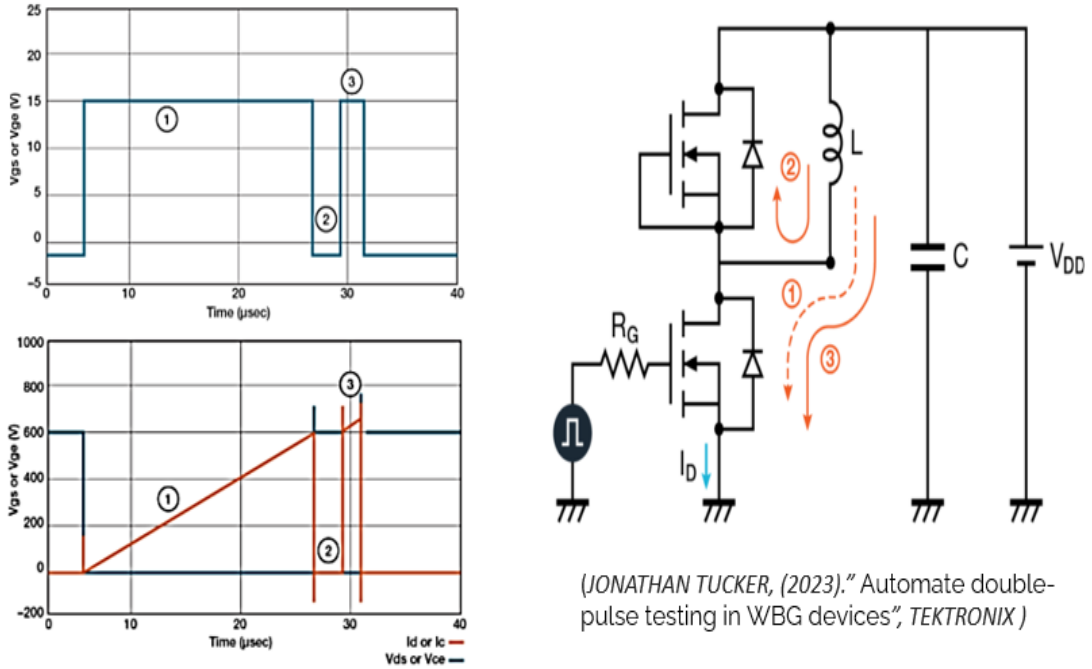


Figure (3) Double pulse test mechanism.

We rely on a set of important metrics for performance evaluation that indicate the quality of the switching process, the most important of which are:

i. (dv/dt and di/dt): are measured between 10% and 90% of nominal values of voltage and current respectively.

ii. Turn-on delay time $\boldsymbol{td(on)}$: This is the period from when the gate-to-source voltage reaches 10 % of its final value, to when the drain current reaches 10 % of its final value during turn on.

iii. Turn-off delay time $\boldsymbol{td(off)}$: This is the period from when the gate-to-source voltage drops to 90 % of its on-state voltage, to when the drain current drops to 90 % of its on-state value during turn off.

iv. Current rise time $\boldsymbol{tr}$**:** The current rise time is the period when the drain current rises from 10 % to 90 % of its final on-state value during turn on.

v. Current fall time $\boldsymbol{tf}$: The current fall time is the period when the drain current drops from 90 % to 10 % of its on-state value during turn off.

$$ton = td(on) + tr \quad and \quad toff = td(off) + \boldsymbol{tf} \tag{1}$$

vi. Switching Losses (E_sw, Off **&** E_sw, ON): These losses are power losses that occur during the transition between the on and off states and are caused by the time it takes for the transistor to perform the switching process, and other factors such as switching frequency, type of load (resistive or inductive), and transistor characteristics.

$$E_{,sw,ON} = \int_0^{tr+tfv} vds(t).id(t)\,dt \tag{2}$$

$$E_{,sw,Off} = \int_0^{tf+trv} vds(t).id(t)\,dt \tag{3}$$

$$P_{t,sw} = (E_{sw,OFF} + E_{,sw,ON}) \tag{4}$$

vii. The voltage overshoot: caused by di/dt increases as the drain current rises, primarily due to a reduction in the fall time of the current. This ringing phenomenon occurs as a result of resonance between the parasitic capacitance of SiC power devices and the stray inductance (Ls) present in the test circuit.

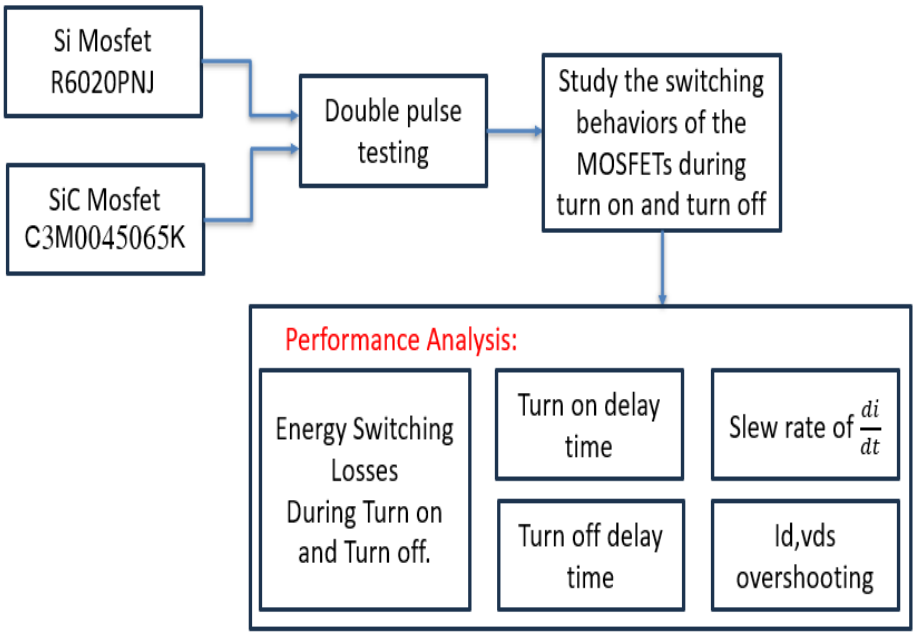


Figure (4) block diagram of double pulse Testing.

Table (1) Double pulse Testing simulation parameters.

Dc Bus Voltage	400 volts
Decoupling Capacitor	220µF
Load	1mH-inductive
Transistor Type	R6020PNJ, (Si)
	C3M0045065K, (SiC)
Positive driving voltage	+15 volt
Negative driving voltage	-5 volt
Drain-Source On-State Resistance	190mΩ
	45mΩ
Total Time of two pulses	70 µsec
Gate Resistor	10Ω

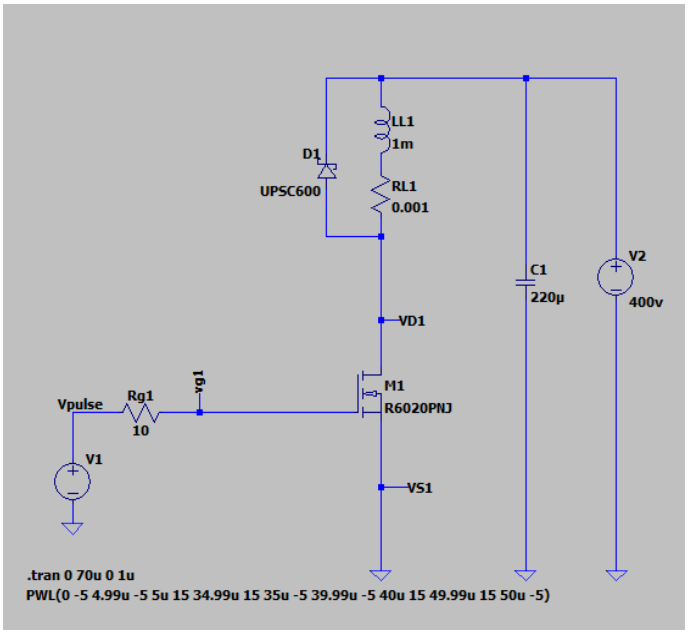


Figure (5) Electrical diagram of the double pulse test circuit on the R6020PNJ silicon transistor.

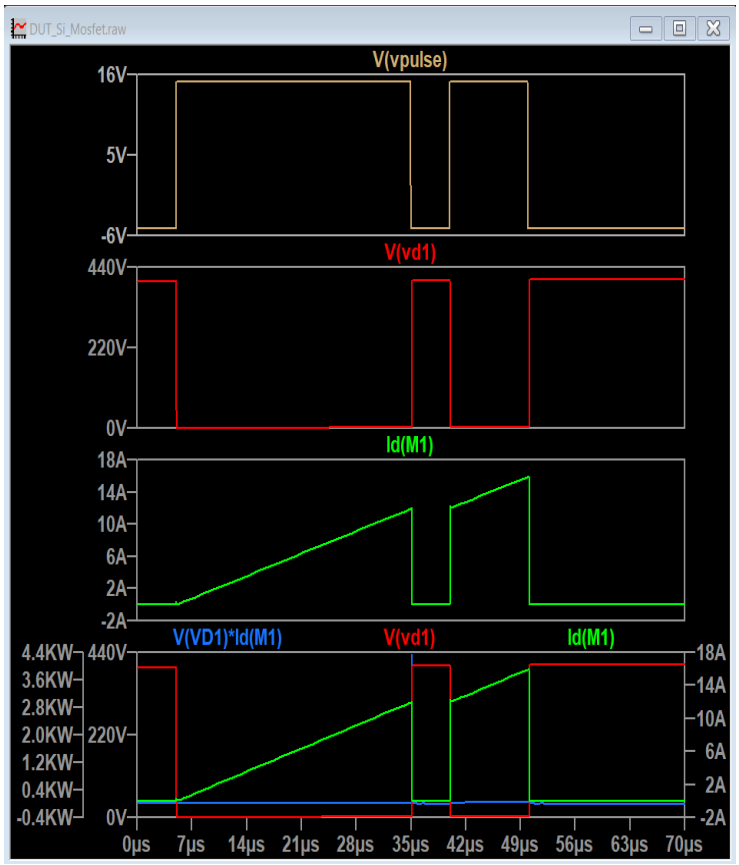


Figure (6) Driving pulses and voltage, current and power curves for the R6020PNJ silicon transistor.

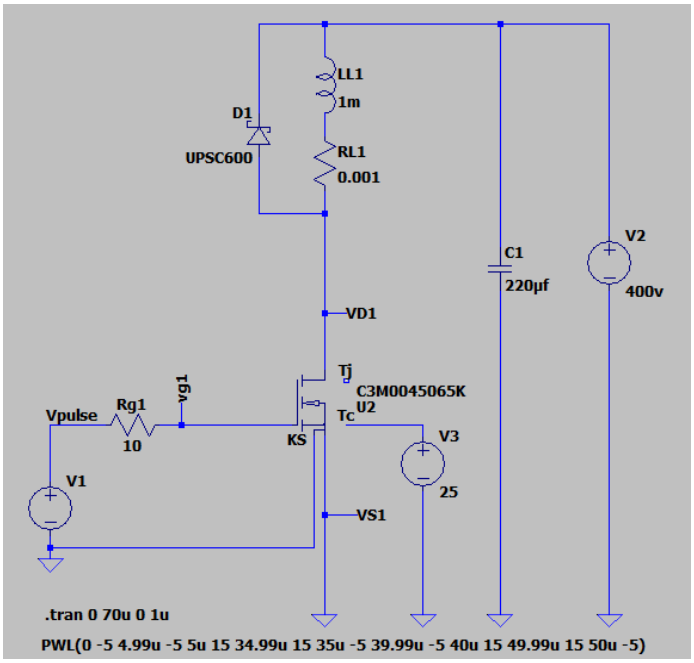


Figure (7) Electrical diagram of the dual pulse test circuit on a silicon carbide transistor C3M0045065K.

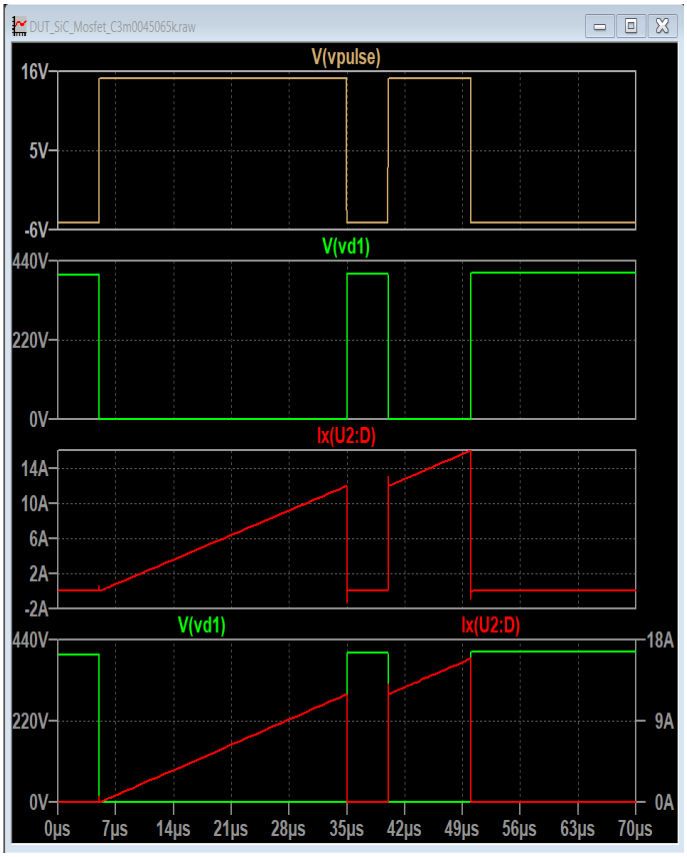


Figure (8) Driving pulses and voltage, current, and power curves for the C3M0045065K silicon carbide transistor.

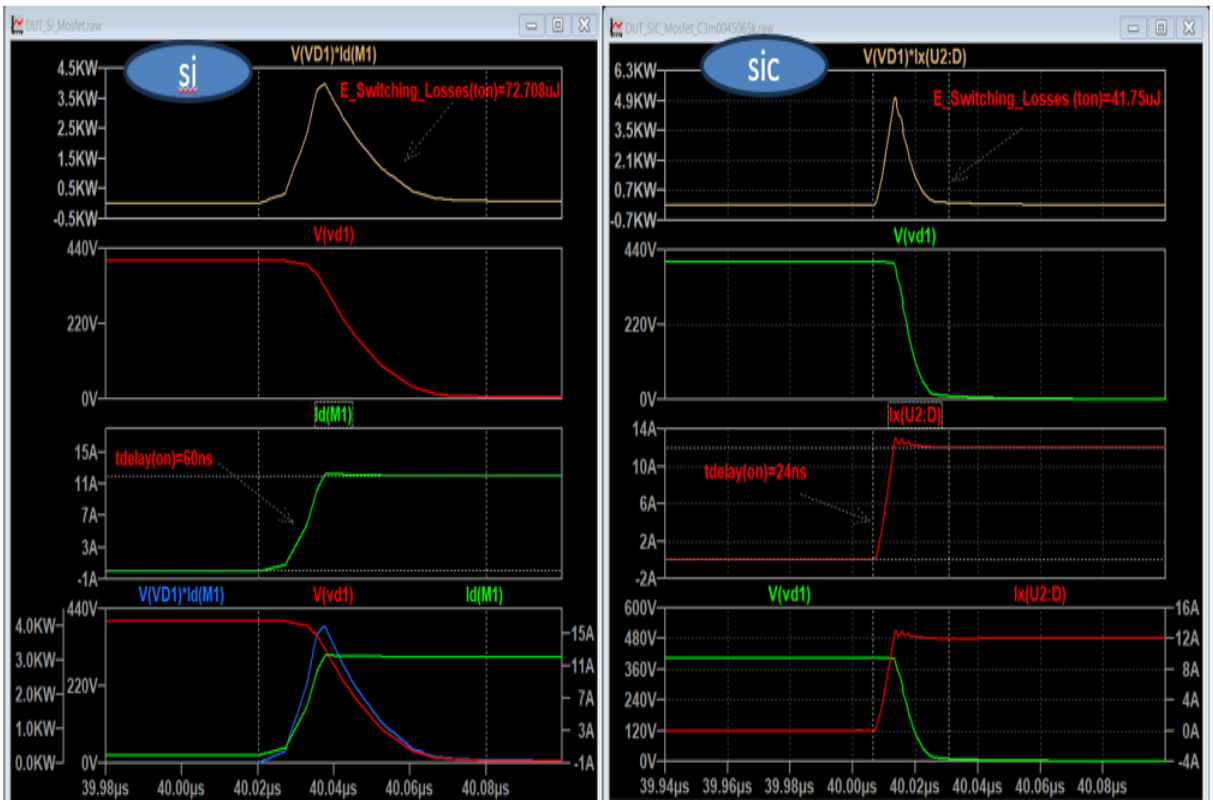


Figure (9) Voltage, current and power loss curves of the two transistors during Turn on operation.

Table (2) Energy Loses and Time delay Analysis for Si and SiC Mosfets during Turn on process.

parameter	E_{on}**(µJ)**	t_{don}**(ns)**
Si Mosfet	70.71	60
SiC Mosfet	41.75	24

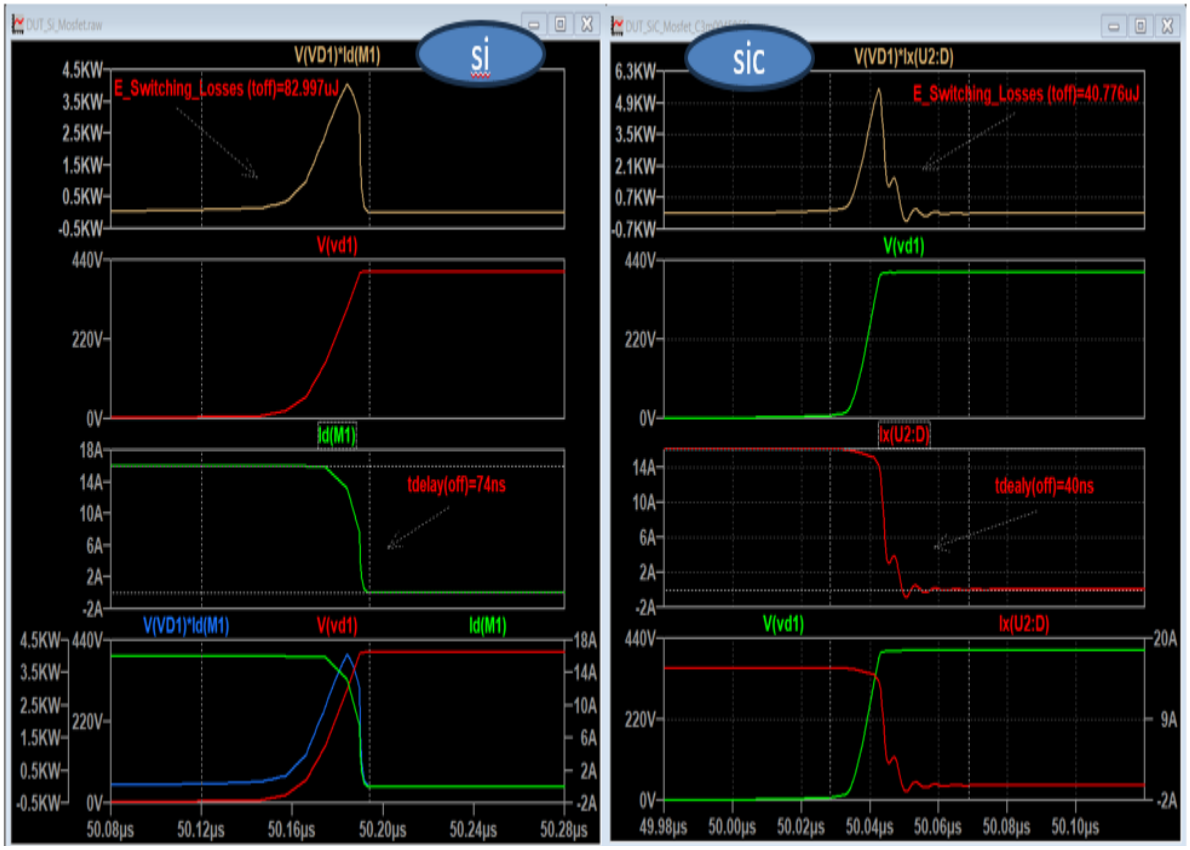


Figure (10) Voltage, current and power loss curves of the two transistors during Turn off operation.

Table (3) Energy Loses and Time delay Analysis for Si and SiC Mosfets during Turn off process.

parameter	E_{off}(µJ)	$t_{d\text{off}}$(ns)
Si Mosfet	82.99	74
SiC Mosfet	40.77	40

The switching times in silicon carbide transistors decrease to 24 ns and 40 ns for the turn-on and turn-off processes, respectively, compared to silicon transistors. The power loss in silicon carbide transistors reduces to 41.75 µJ and 40.77 µJ for the turn-on and turn-off processes, compared to silicon transistors. The rapid change in current flow rate in silicon carbide transistors causes greater overshoots in voltage and current signals compared to silicon transistors.

3-Influence of Parasitic Parameters on The Switching Characteristics of SiC Mosfets:

In this part of the research, we will evaluate the switching behavior of the Silicon Carbide (SiC) MOSFET model C3M0045065K using a double pulse test. We will intentionally vary the values of the internal parasitic parameters and drive parameters, and observe their impact on performance indicators such as switching losses, turn-on and turn-off delay times, and the rate of change of current over time, as illustrated in the box diagram in Figure (11).

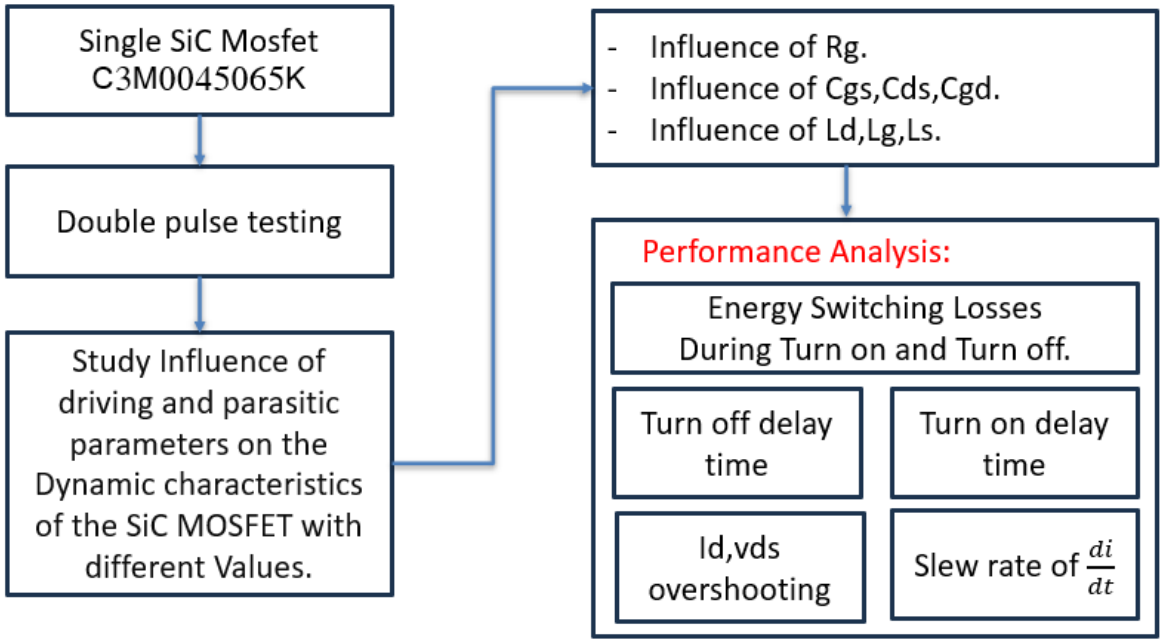


Figure (11) Block diagram of performance analysis of the effect of parasitic elements on the Dynamic characteristics of the silicon carbide transistors.

Table (4) illustrates the study parameters, including the gate drive voltages and the internal parameters of the transistor.

Table (4) Simulation parameters of Double pulse Testing for SiC Mosfet under different parasitic values.

Dc Bus voltage	400 volts
Decoupling Capacitor	1000µF
Load	1mH
Transistor Type	C3M0045065K, (SiC)
Positive driving voltage	+15 volt
Negative driving voltage	-5 volt
Drain-Source On-State Resistance	45mΩ
Ciss (input Capacitance)	1621pf
Crss (Reverse Capacitance)	8 pf
Coss (output Capacitance)	101pf
Rg	[1,5,10,15,20] Ω
Inductive effect of di/dt through the drain.	[1,10,30,50,70] nH
Inductive effect of di/dt through the source.	[1,3,6,9,12] nH

Inductive effect of di/dt through the gate.	[1,5,10,15,20] nH
Drain to Source Capacitance.	[75.90 ,110, 125] pf
Gate to Drain Capacitance.	[6, 8, 10, 15, 20] pf
Gate to Source Capacitance.	[1.5, 2.5, 3.5, 4.5, 5.5] nF

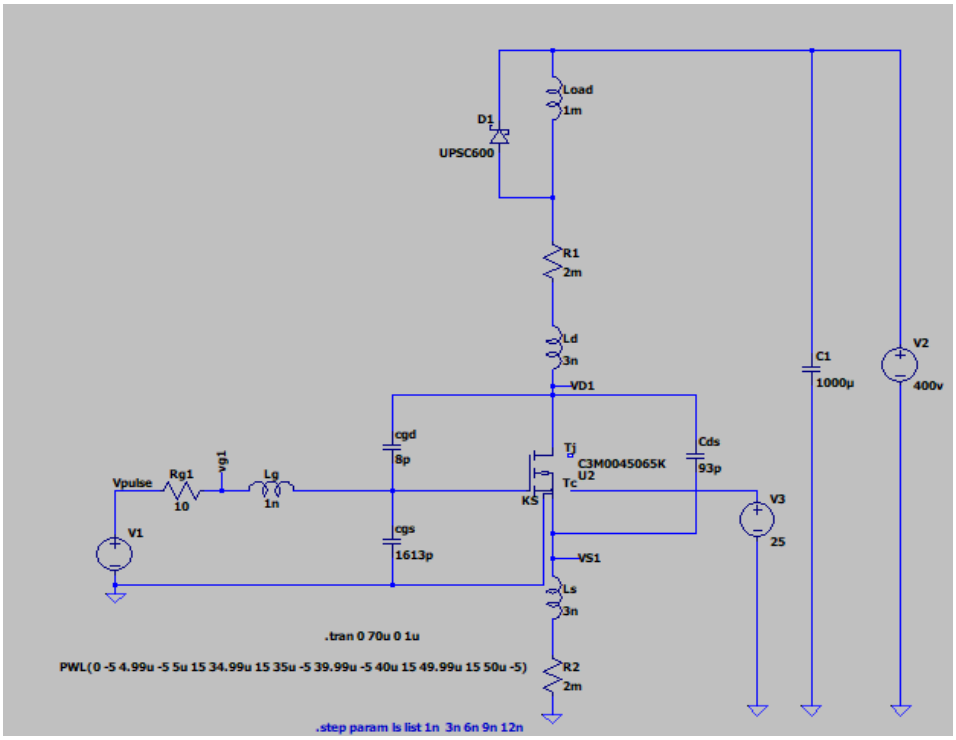


Figure (12) Double pulse Testing for Sic Mosfet under different Values of parasitic Components.

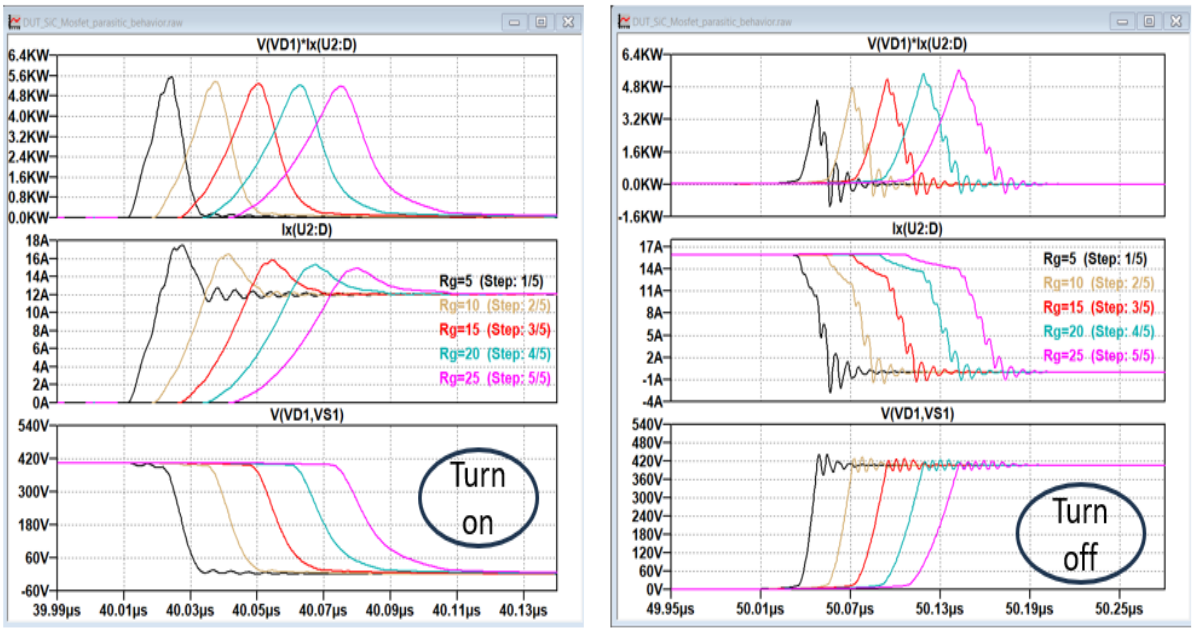


Figure (13) Voltage, current and power loss curves of the transistor during switching (on/off) operation for different Rg values.

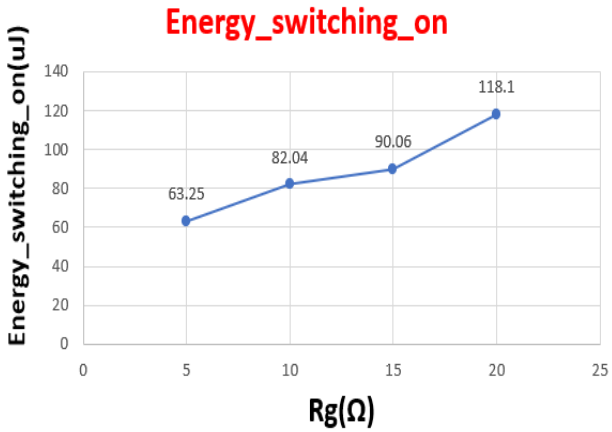


Figure (14) Energy Switching Losses during Turn on for Different Rg Values.

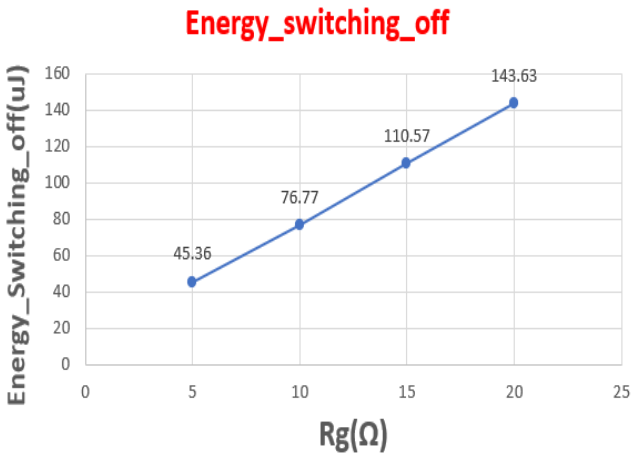


Figure (15) Energy Switching Losses during Turn off for Different Rg Values.

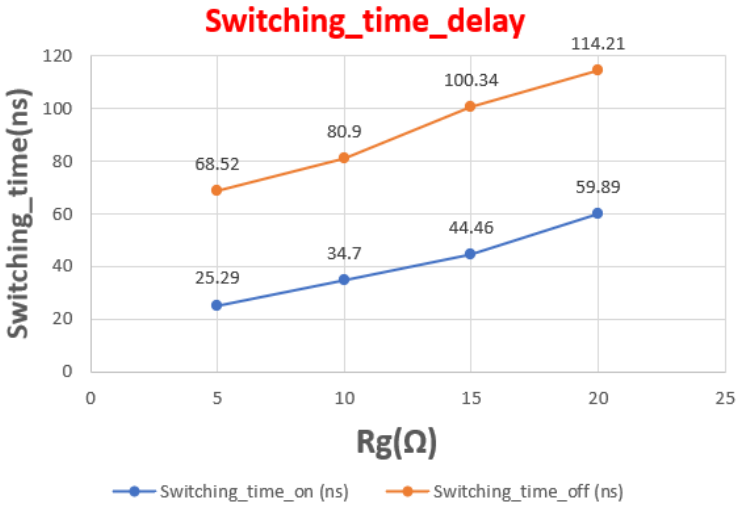


Figure (16) Switching Time Delay during Turn on/off for Different Rg Values.

Table (5) Performance indicators of SiC transistor at different gate resistance values.

Rg(Ω)	E_{off}(µJ)	E_{on}(µJ)	t_{off}(ns)	t_{on}(ns)
5	45.36	63.25	86.52	25.29
10	76.77	82.04	80.9	34.7

15	110.57	90.06	100.34	44.46
20	143.63	118.1	114.21	59.89

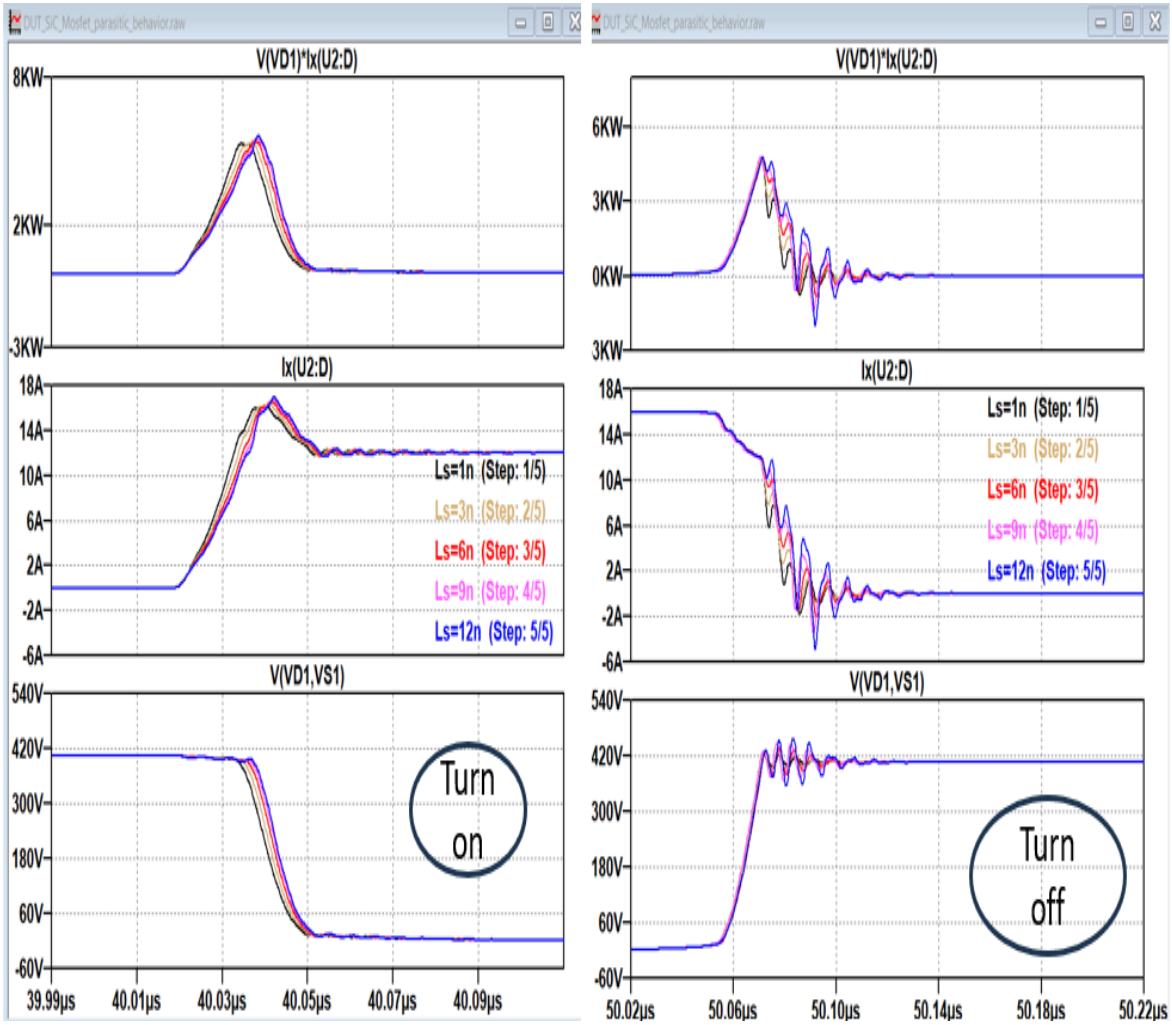


Figure (17) Voltage, current and power loss curves of the transistor during switching (on/off) operation for different Ls values.

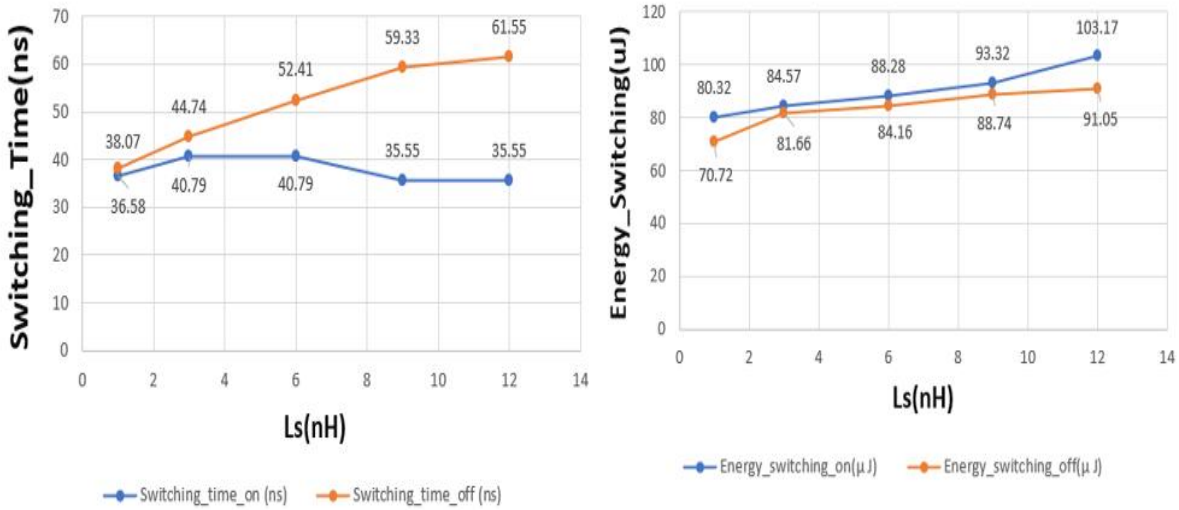


Figure (18) Switching Time Delay and Energy Loses during Turn on/off for Different Ls Values.

Table (6) Performance indicators of SiC transistor at different Ls values.

Ls(nH)	E_{off}(µJ)	E_{on}(µJ)	t_{off}(ns)	t_{on}(ns)
1	70.72	80.32	38.07	36.58
3	81.66	84.57	44.74	40.79
6	84.16	88.28	52.41	40.79
9	88.74	93.32	59.33	35.55
12	91.05	103.17	61.55	35.55

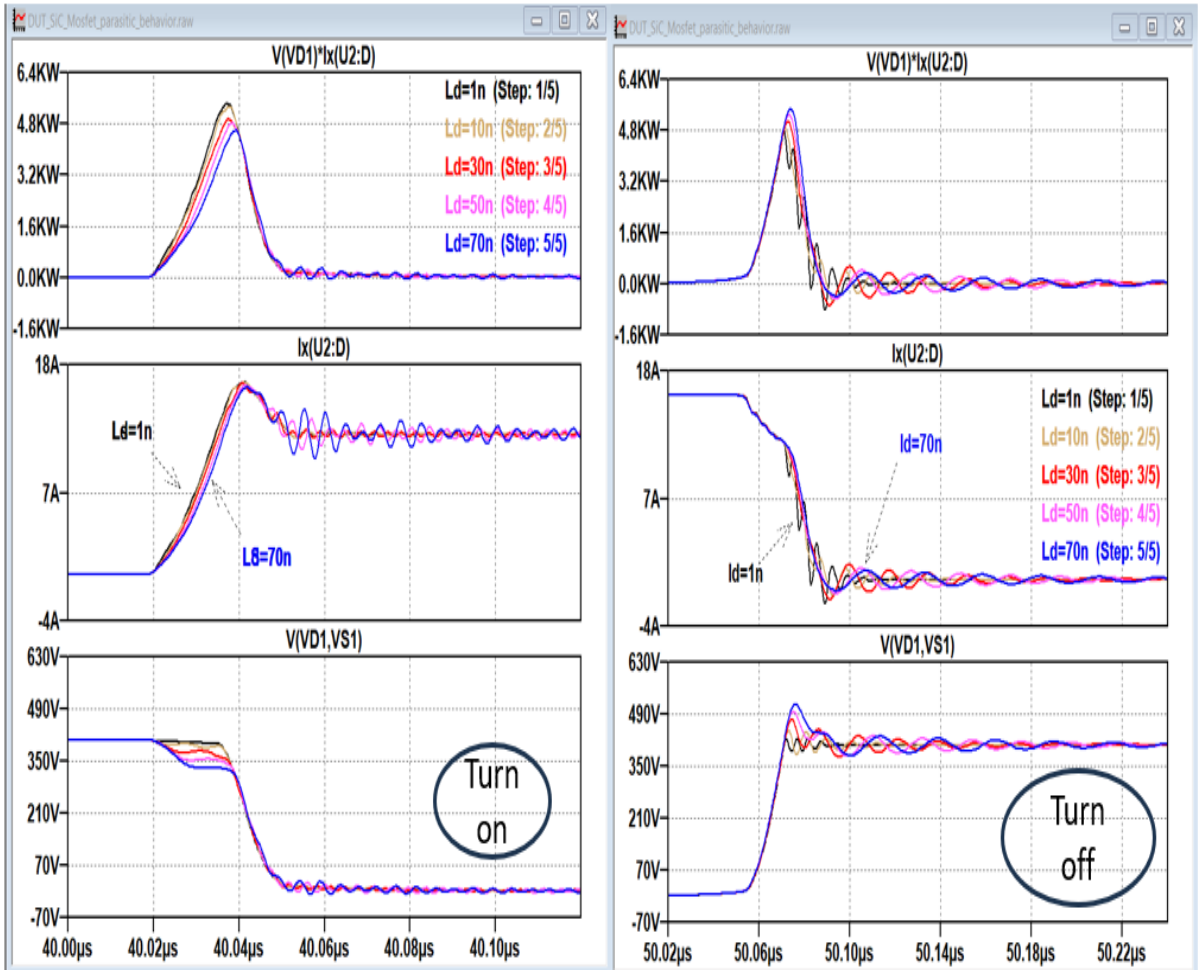


Figure (20) Voltage, current and power loss curves of the transistor during switching (on/off) operation for different Ld values.

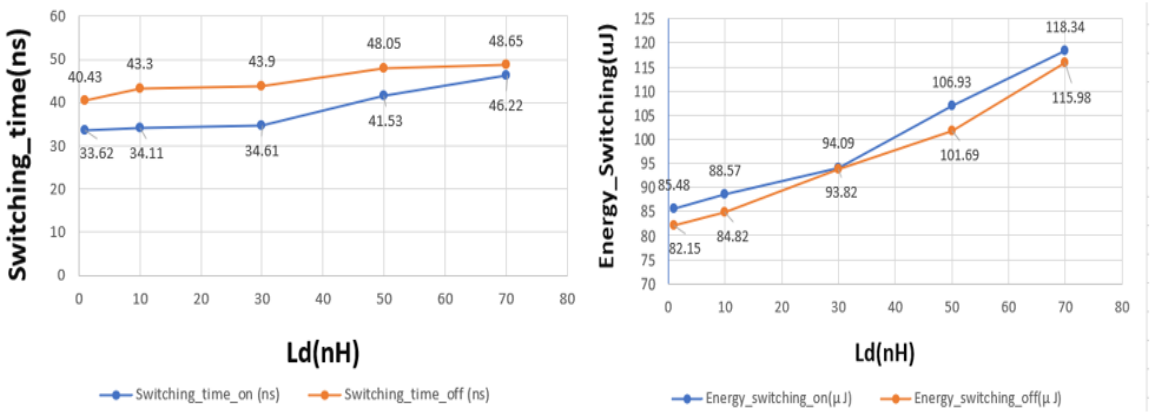


Figure (21) Switching Time Delay and Energy Loses during Turn on/off for Different Ld Values.

Table (7) Performance indicators of SiC transistor at different Ld values.

Ld(nH)	E_{off}(μJ)	E_{on}(μJ)	t_{off}(ns)	t_{on}(ns)
1	82.15	85.48	40.43	33.62
10	84.82	88.57	43.3	34.11
30	93.82	94.09	43.9	34.61
50	101.69	106.93	48.05	41.53
70	115.98	118.34	48.65	46.22

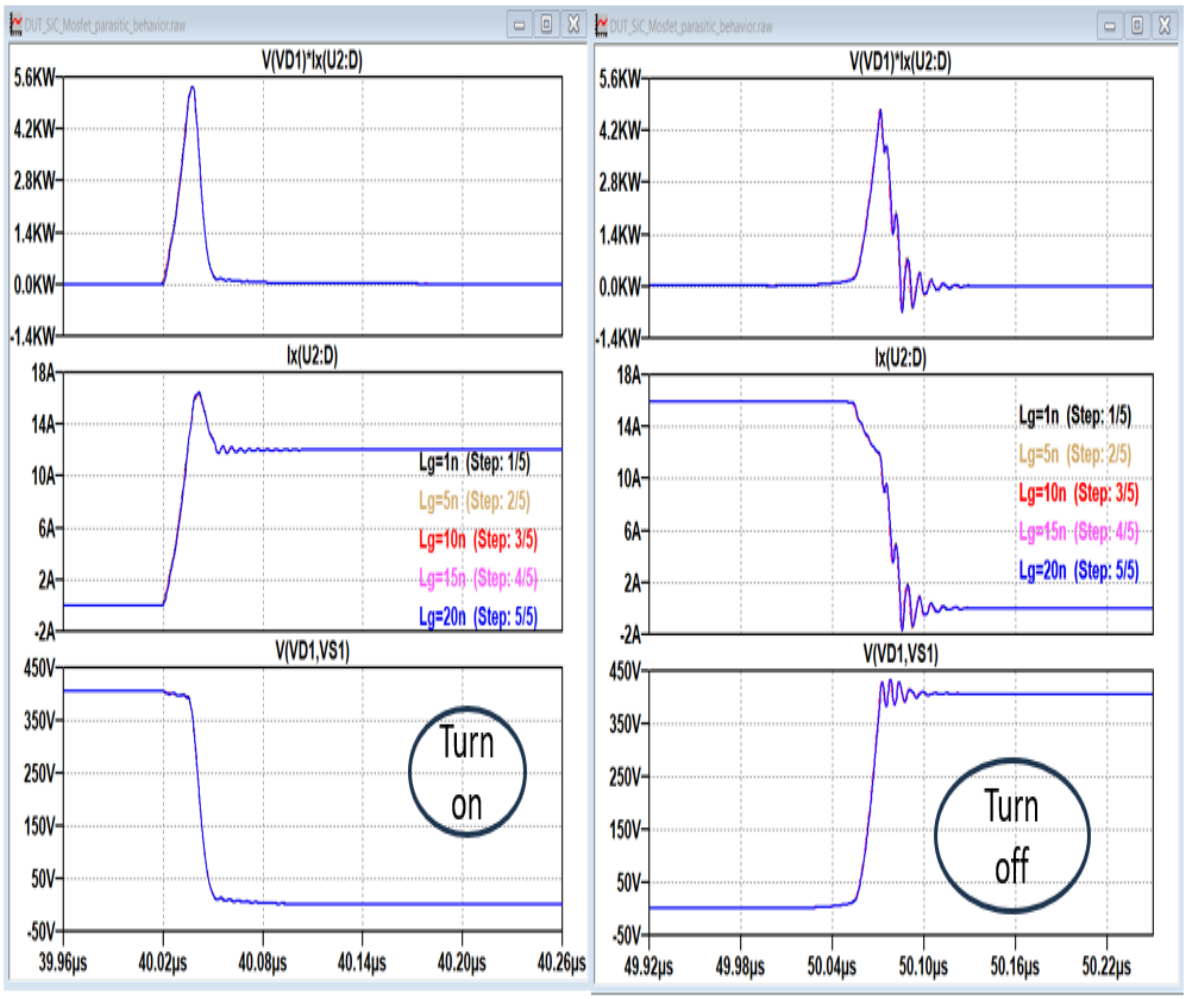


Figure (22) Voltage, current and power loss curves of the transistor during switching (on/off) operation for different Lg values.

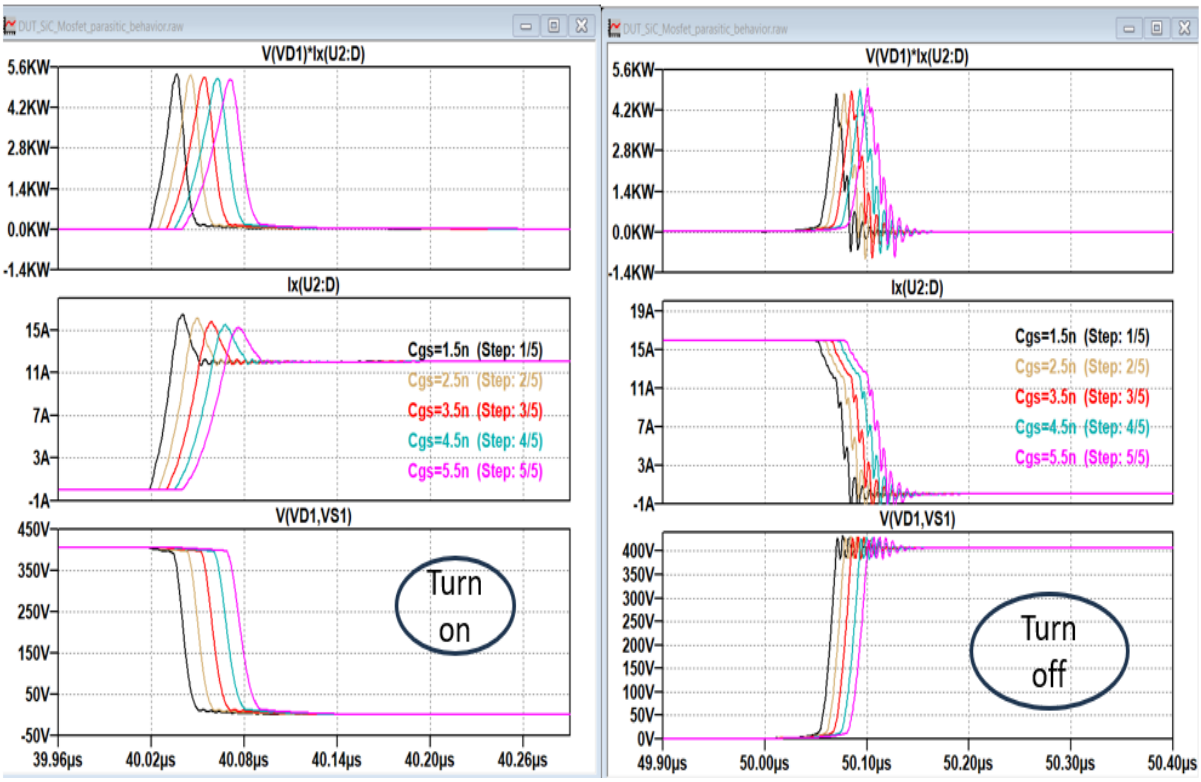


Figure (23) Voltage, current and power loss curves of the transistor during switching (on/off) operation for different Cgs values.

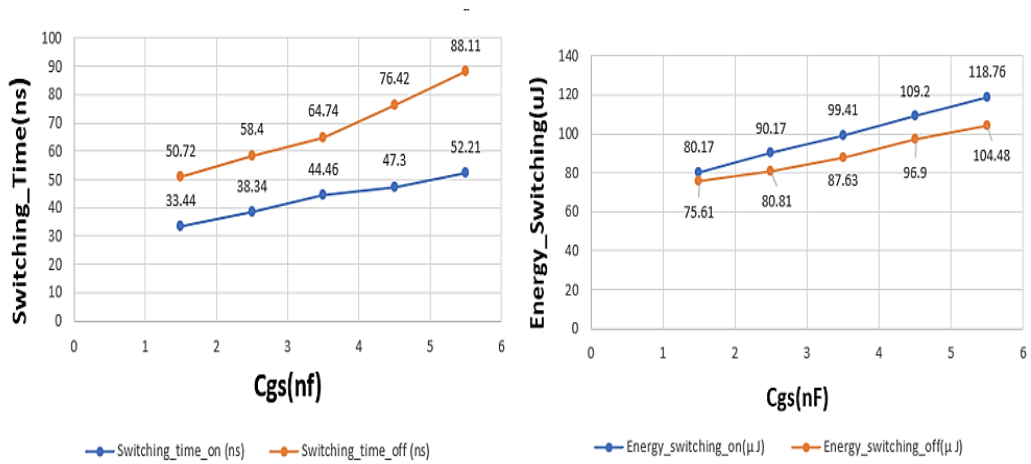


Figure (24) Switching Time Delay and Energy Loses during Turn on/off for Different Cgs.

Table (8) Performance indicators of SiC transistor at different Cgs values.

Cgs (nf)	E_{off}(µJ)	E_{on}(µJ)	t_{off}(ns)	t_{on}(ns)
1.5	75.61	80.17	50.72	33.44
2.5	80.81	90.17	58.4	38.34
3.5	87.63	99.41	64.74	44.46
4.5	96.9	109.2	76.42	47.3
5.5	104.48	118.76	88.11	52.21

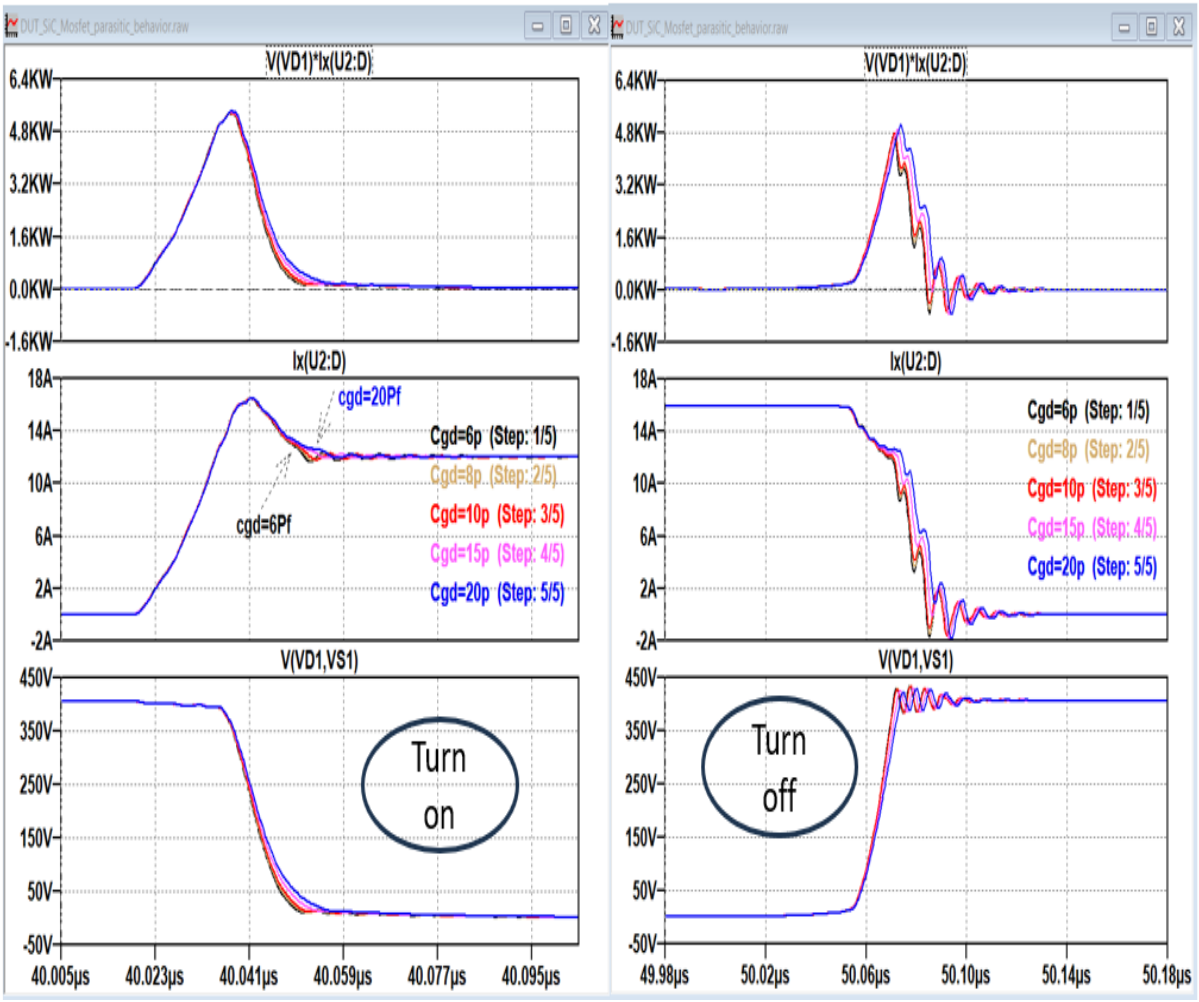


Figure (25) Voltage, current and power loss curves of the transistor during switching (on/off) operation for different Cgd values.

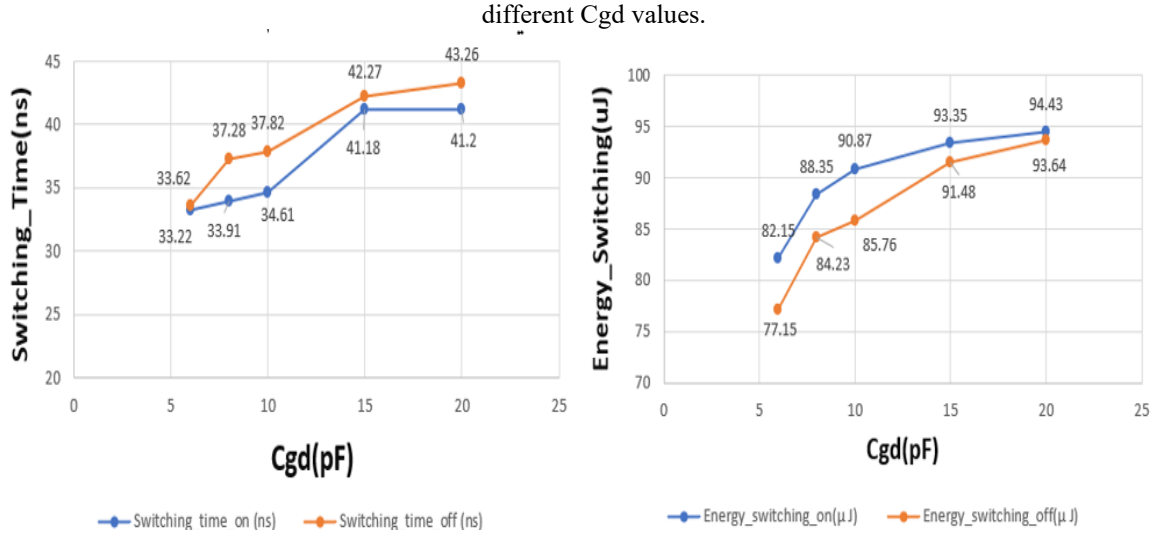


Figure (26) Switching Time Delay and Energy Loses during Turn on/off for Different Cgd.

Table (9) Performance indicators of SiC transistor at different Cgd values.

Cgd (pf)	E_{off}(µJ)	E_{on}(µJ)	t_{off}(ns)	t_{on}(ns)
6	77.15	82.15	33.62	33.22
8	84.23	88.35	37.28	33.91
10	85.76	90.87	37.82	34.61
15	91.48	93.35	42.27	41.18
20	93.64	94.43	43.26	41.2

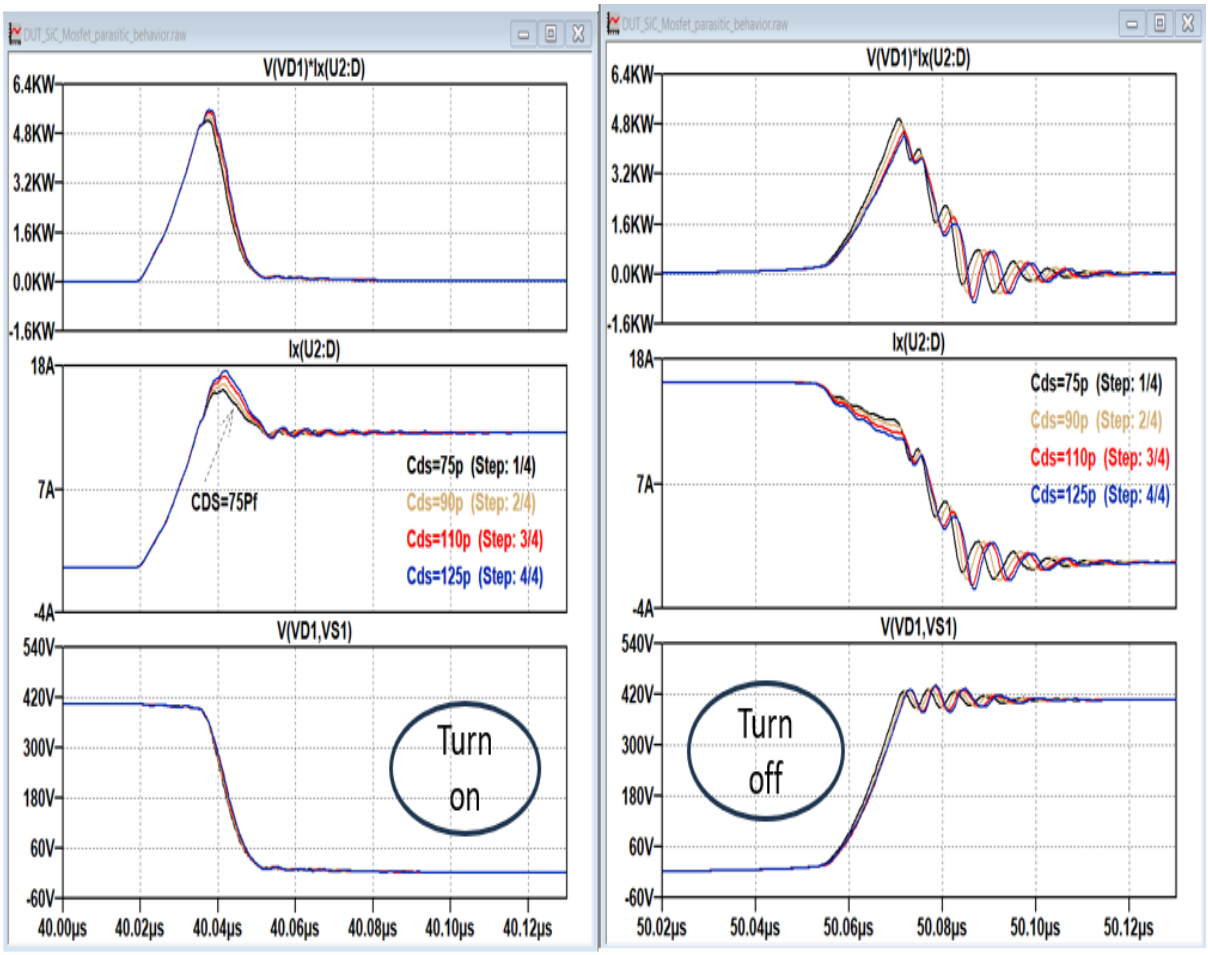


Figure (27) Switching Time Delay and Energy Loses during Turn on/off for Different Cds.

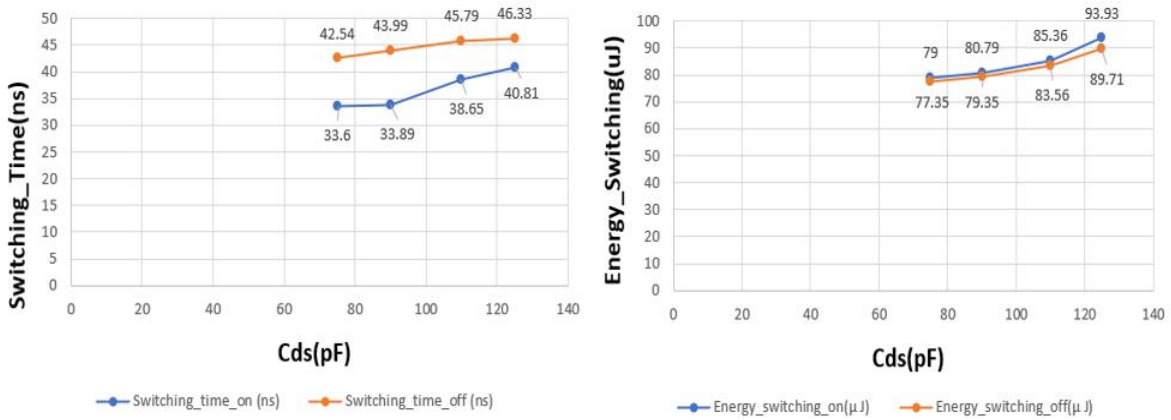


Figure (28) Switching Time Delay and Energy Loses during Turn on/off for Different Cds.

Table (10) Performance indicators of SiC transistor at different Cds values.

Cds (pf)	E_{off}(µJ)	E_{on}(µJ)	t_{off}(ns)	t_{on}(ns)
75	77.35	79	42.54	33.6
90	79.35	80.79	43.99	33.89
110	83.56	85.36	45.79	38.65
125	89.71	93.93	46.33	40.81

The simulation results can be summarized in the following points that should be taken into account in the design considerations of drive circuits:

i. Increasing the gate resistance value slows down the switching process because it increases the charging time of the input capacitance.
ii. Increasing the gate resistance value increases the power loss during both the turn-on and turn-off processes, especially during the turn-off stage.
iii. Increasing the gate resistance value leads to a reduction in undesirable overshoots in the voltage and current signals during the switching processes.
iv. Choosing a gate resistance value within the range of Ω [5-10] allows for a reduction in undesirable overshoots during the switching processes while maintaining good switching times.
v. An increase in both (Ls, Ld) causes an increase in the switching times of the transistor as well as switching losses.
vi. The value of Ls has the greatest effect on delaying the turn-off time of the transistor and on undesirable overshoots during the turn-off process.
vii. The value of (Lg) does not affect the turn-on and turn-off times of the transistor, but it increases the undesirable overshoots in the voltage signal between the drain and source.
viii. An increase in the values of Cgd and Cds leads to unwanted overshoots during the turn-off process of the transistor.
ix. The value of Cgs has the most significant impact on increasing the turn-on and turn-off times of the transistor, while having a lesser effect on overshoots compared to the capacitances Cgd and Cds.

4- Parasitic Inductance Effects on The Switching Performance of Parallel Sic Mosfets:

Connecting transistors in parallel plays a significant role in enhancing the performance of electronic circuits. Parallel connection reduces the overall resistance in the circuit, leading to decreased power losses due to heat. This configuration also enhances the switching efficiency, allowing transistors to operate more quickly and effectively. the total current is distributed among them rather than being concentrated in a single transistor. This

distribution minimizes thermal dissipation, as each transistor experiences a reduced thermal load. Consequently, this helps maintain the operating temperature within safe limits. Moreover, the performance of the switching process is significantly improved as the total gate capacitance decreases when transistors are connected in parallel. A lower gate capacitance translates to a shorter switching time, thereby enhancing the overall switching performance of the circuit.

Lastly, by distributing current across multiple transistors, circuits can support higher currents and, consequently, greater power levels. This capability enables the system to handle larger loads without risking failure or breakdown.

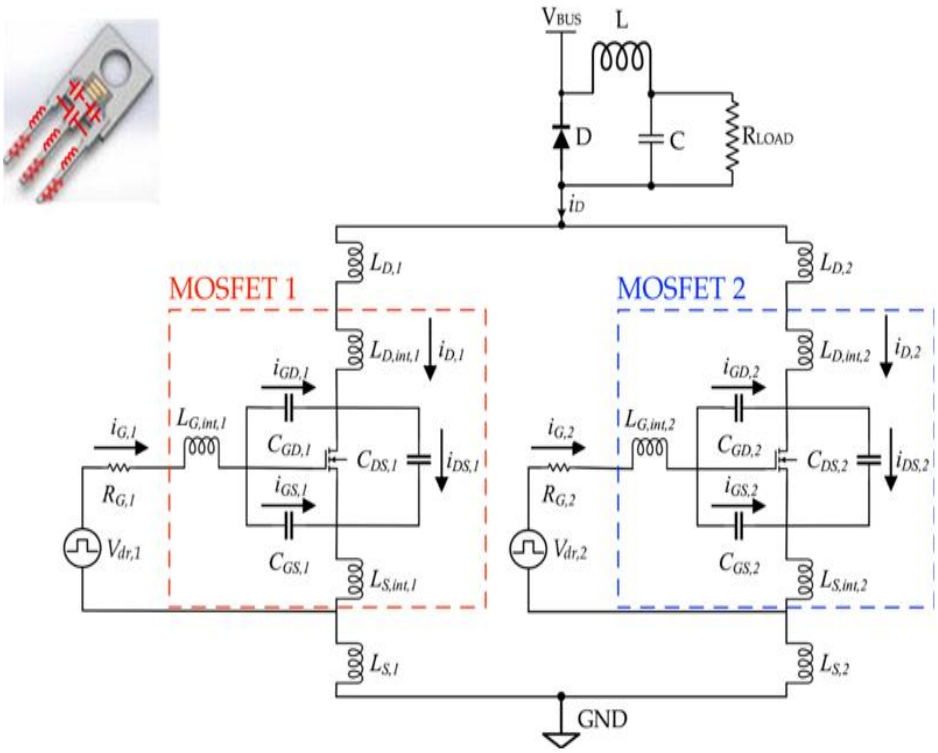


Figure (29) Parallel driving of silicon carbide Mosfets.

In this section of the research, we will study the effect of variations in the values of parasitic elements in parallel driving circuits, specifically when driving two silicon carbide (SiC) MOSFETs using pulse signals at a frequency of 200 kHz and a duty cycle of 50%. The charging and discharging paths are secured using a totem pole configuration, with a charging resistance Rg(on) equal to 10 ohms and a discharging resistance Rg(off) equal to 5 ohms. We will investigate performance indicators such as switching losses, switching times, the rate of change in current, and the difference between the currents of the two transistors. This analysis will take into account the parasitic inductive effects in the paths as well as the parasitic capacitive effects between the transistor terminals. The capacitive effects will be calculated based on the input capacitance C_{iss} and output capacitance C_{oss} values according to the datasheet for these transistors. A deliberate difference in these capacitance values will be introduced between the two transistors to simulate manufacturing variations that cannot be controlled during production.

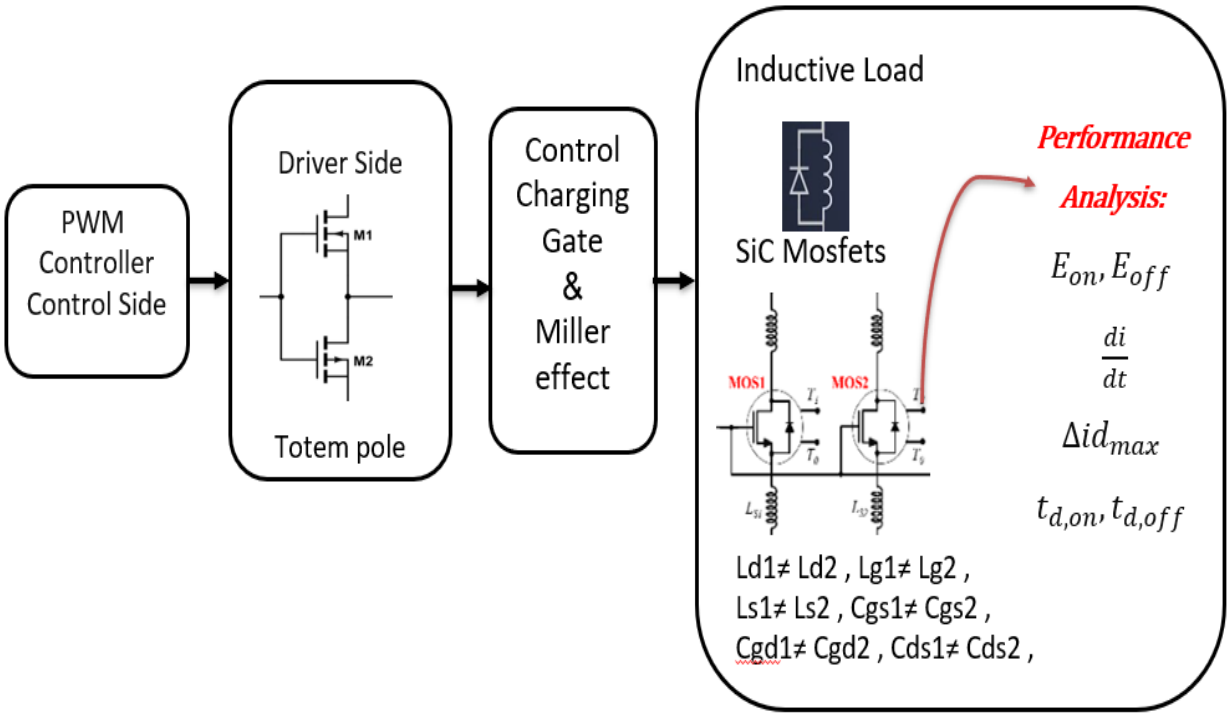


Figure (30) The block diagram of the parallel driving circuit.

We calculated the values of the internal parasitic capacitances between the transistor terminals using equations 5, 6, and 7 provided below, based on the datasheet of this transistor.

Ciss=Cgs+Cgd (5)
Coss=Cds+Cgd (6)
Crss=Cgd (7)

Table (11) Simulation parameters of Driving Parallel SiC Mosfets under different parasitic values.

Dc Bus voltage	400 volts
Decoupling Capacitor	1000µF
Load	100uH
Transistor Type	C3M0045065K, (SiC)
Positive driving voltage	+15 volt
Negative driving voltage	-5 volt
Drain-Source On-State Resistance	45mΩ
Ciss (input Capacitance)	1621pf
Crss (Reverse Capacitance)	8 pf
Coss (output Capacitance)	101pf
Rg (on)	10 Ω
Rg(off)	5 Ω
Inductive effect of di/dt through the drain.	Ld1=10nH, Ld2=1nH

Inductive effect of di/dt through the source.	Ls1=7.5 nH, Ls2=1.5 nH
Inductive effect of di/dt through the gate.	Lg1=1nH, Lg2=1.7 nH
Drain to Source Capacitance.	Cds1=120 pf, Cds2=95pf
Gate to Drain Capacitance.	Cgd1=8pf, Cgd2=25pf
Gate to Source Capacitance.	Cgs1=2100 pf, Cgs2=1613 pf
Operation Frequency	200 kHZ
Duty Cycle	50%

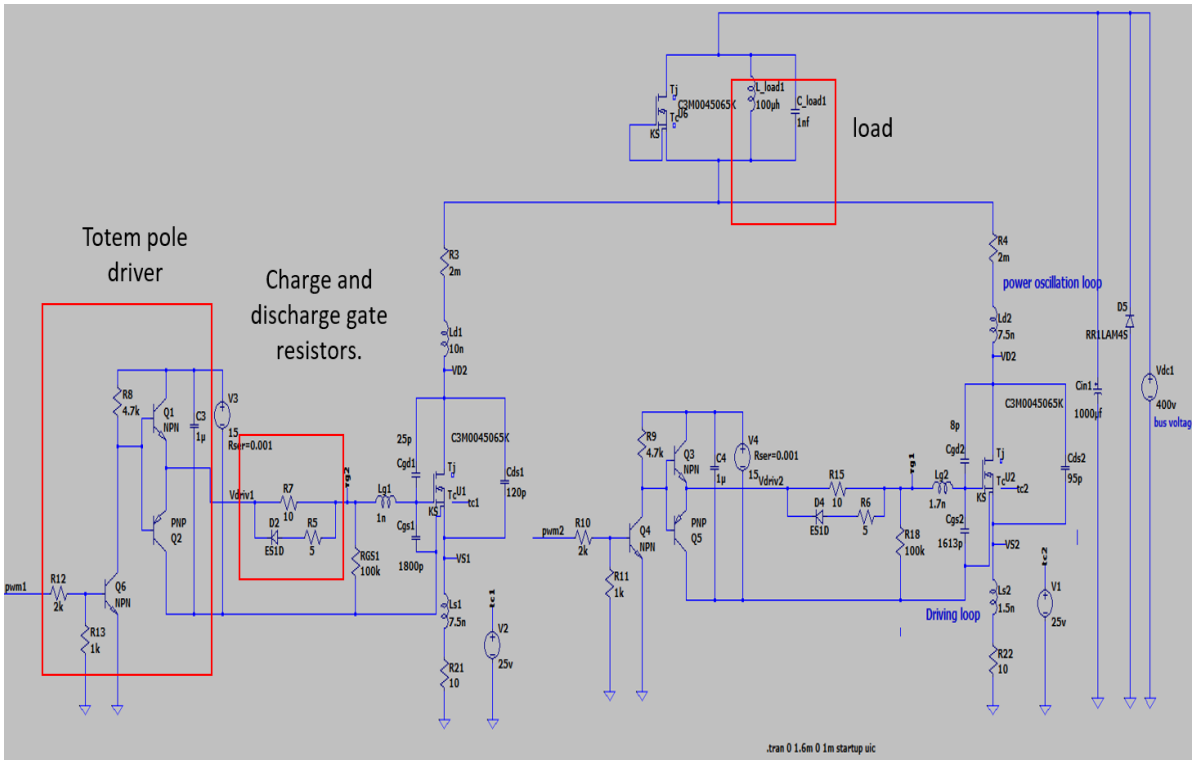


Figure (31) Circuit diagram for driving two C3M0045065K silicon carbide transistors in parallel.

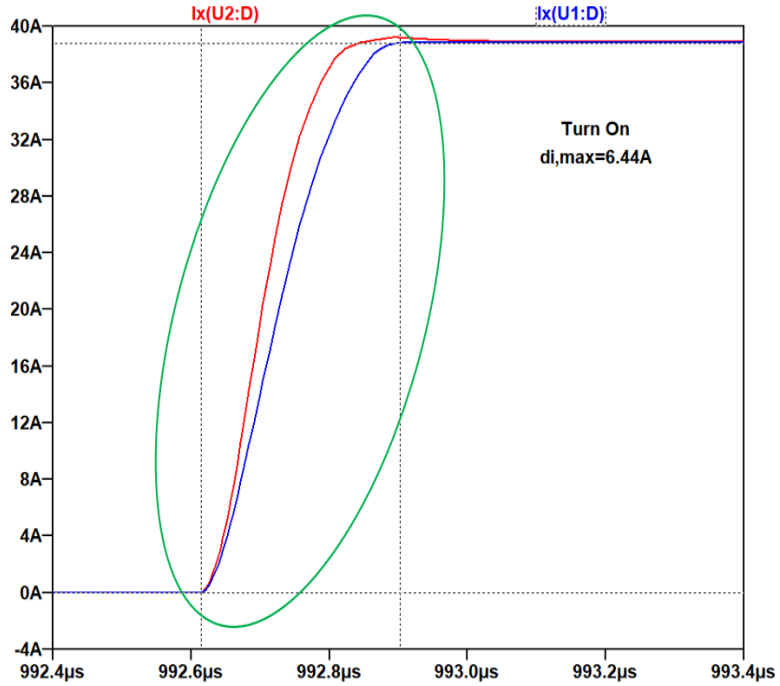


Figure (32) Simulation diagram of dynamic current imbalance at turn-on moment.

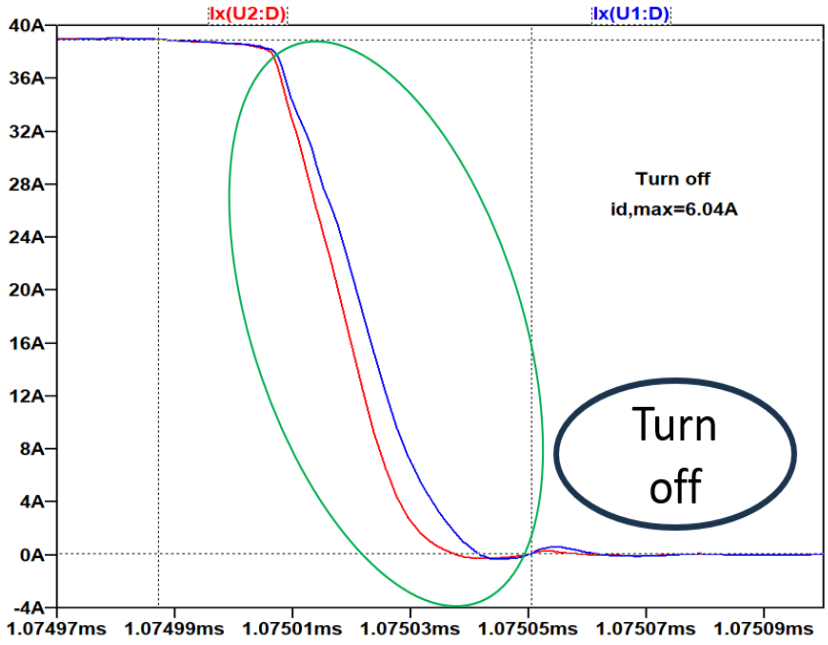


Figure (33) Simulation diagram of dynamic current imbalance at turn-off moment.

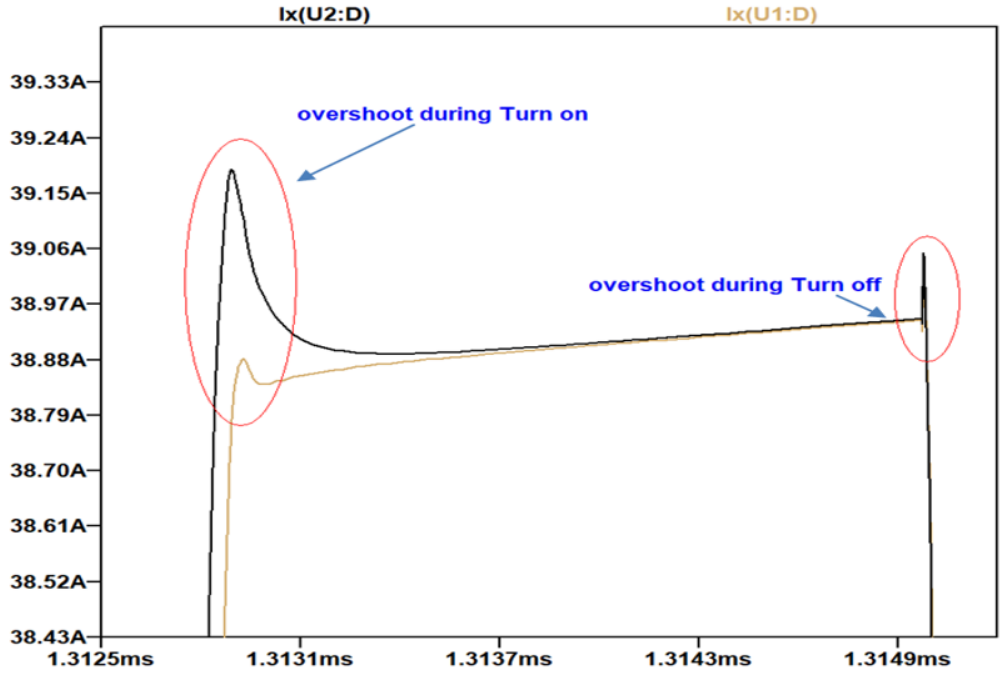


Figure (34) Simulation diagram of Overshooting dynamic current at turn-on/off moment.

Table (12) Performance indicators of Parallel SiC Mosfets.

	Turn on				**Turn off**			
parameter	$\frac{di}{dt}$ **(A/ns)**	$\Delta Imax$ **(A)**	**E(on) (mJ)**	t_{don} **(ns)**	$\frac{di}{dt}$ **(A/ns)**	$\Delta Imax$ **(A)**	**E(off) (µJ)**	t_{doff} **(ns)**
Mosfet1	0.21	6.44	10.53	295.38	1.29	6.04	806.69	63.27
Mosfet2	0.16		10.95	226.78	1.30		751.95	62.17

- ✓ The difference in currents between the two transistors is 6.44 A and 6 A for the On and Off operations, respectively.
- ✓ In the conventional method, the difference in the decline time between the two transistors is 1.1 ns, while the difference in the rise time is 68.6 ns.
- ✓ Switching losses reach 806.69 µJ and 751.95 µJ for the Off operation.

5- Conclusion

Parasitic parameters have a larger influence on Silicon Carbide (SiC) devices with an increase of the switching frequency. This limits full utilization of the performance advantages of the low switching losses in high frequency applications. A fast-switching double pulse test platform has been established to measure the individual effects of each parasitic parameter on the switching behavior. the influence of LG on the switching characteristics is relatively small. However, the influence of LD on oscillations and voltage spikes is significant. The source parasitic inductance LS has some inhibitory effect on oscillations and voltage spikes, but it increases the switching energy loss. The influences of parasitic capacitances on switching characteristics are also studied experimentally. The parasitic capacitances CGS and CGD have a great influence on switching times. With an increase of CGS and CGD, the turn-on and turnoff times are noticeably increased.

References:

[1]. Zhang S.(2023). Influence of driving and parasitic parameters on the switching behaviors of the SiC MOSFET. Front. Energy Res.
[2]. Jianing Guo. (2022). Analysis of Current Imbalance in Paralleled Silicon Carbide Power MOSFETs. Academic Journal of Science and Technology.
[3]. Haihong Qin. et al. (2018). Influence of Parasitic Parameters on Switching Characteristics and Layout Design Considerations of SiC MOSFETs. Journal of Power Electronics.
[4]. Y He. Et Al. (2024). Dynamic Current Balancing For Paralleled Sic Mosfets With Circuit Mismatches Considering Circulating Current In Drive Circuit. Cpss Transactions On Power Electronics And Applications.
[5]. M.Eko Sulistyo. Et Al. (2023). A New Method Of The Active Gate Driver For Current Balancing In The Parallel MOSFET Circuits. Journal Of Novel Carbon Resource Sciences & Green Asia Strategy, Researchgate.
[6]. Giannopoulos, N. Et Al. (2023). Active Autonomous Open-loop Technique For Static And Dynamic Current Balancing Of Parallel-connected Silicon Carbide Mosfets. Energies Journal.
[7]. Shuang Zhao. Et Al. (2023). Digital Close-loop Active Gate Driver For Static And Dynamic Current Sharing Of Paralleled Sic Mosfets. Ieee Journal Of Emerging And Selected Topics In Power Electronics.
[8]. Shuang Zhao. et al. (2023). Parallel Connection of Silicon Carbide MOSFETs – Challenges, Mechanism, and Solutions. IEEE Transactions on Power Electronics.