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Implementation of A Low Power Low Complexity VLSI Architecture for DSSS Signal Transmission and Reception.

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Abstract : *In this paper, a new approach to design VLSI architecture for DSSS is proposed and implemented. In this we aimed towards designing a low power and low complexity architecture. An extremely lucid technique is implemented in Generating the Pseudo Random Sequence, which is the principal component in the design. The various blocks of the design like encoder, decoder, linear feedback shift register etc., are realized using low power VLSI components with an ease of low complexity approach. The Design is implemented on XA9536XL CPLD using XILINX ISE simulator and XILINX XST synthesizer. The results reveal that the power consumption, number of slice registers and other combinational circuits are less compared to the existing architectures.*

Keywords: *DSSS, low power VLSI, VHDL, Pseudo Random sequence, CPLD, Linear feedback shift register.*

I. INTRODUCTION

Among the various spread spectrum techniques, direct sequence spread spectrum (DSSS) has various advantages like low power density spectrum, low probability of intercept and high immunity to noise. Hence it is widely used in military applications and modern commercial communications [1]. Generation of Pseudo Random sequence for encoding a message into DSSS signal is vital in DSSS communication. It involves spreading of message signal components with reference to the Pseudo Random sequence.

Direct-sequence spread spectrum (DS-SS) systems can enhance the signal-to-noise ratio (SNR) on the channel by collecting the time delayed energy of signals, increase user capacity by reducing multiuser interference, and prevent from intercepting the data by spreading them with pseudo noise (PN) codes. Because of these advantages, the DS-SS technique is adopted by many data formats and mobile communication systems such as IS-95 code-division multiple-access (CDMA) systems, Third-Generation Partnership Project (3GPP) and 3GPP2 standards, and global positioning systems and satellite navigation systems [5].

After researching on the complexity of processes involved in the traditional DSSS communication, a new approach which involves low complexity linear feedback shift register for generating Pseudo Random sequence bits for encoding is proposed and implemented. Various spreading techniques are discussed in this paper. The component details of the transmitter and receiver blocks along with other smaller blocks have been discussed. The results are compared with the existing architectures.

II. SPREAD SPECTRUM TECHNIQUE

Spread Spectrum has been defined as a means of transmission in which the signal occupies strategically spread bandwidth. The band spreading is accomplished by utilizing a code which is independent of the data. A synchronized reception with the code at the receiver is used for de-spreading the data thereby recovering it. The spread spectrum communication is widely used in military, avionics, scientific, industrial and civil usage. Spread spectrum has the following advantages [2].

- Low power spectral density
- Interference limited operation
- Privacy due to unknown random codes
- Reduction of multipath effects
- Random access possibilities
- Anti-jam performance

There are basically two types of spread spectrum modulation techniques [3]: frequency hopping spread spectrum (FHSS) and direct sequence spread spectrum (DSSS). These two techniques are equally competent in their performances. DSSS as the advantage of providing higher capabilities than FHSS spreading while used in point - to - multi point, short distance applications such as indoor wireless LANs in offices. The technique is efficient in long distance communication when used in point – to – point communication. This application is found in building to building links, point of presence (POP) to base station links in cellular communication etc.,

III. DSSS TECHNIQUE

The Process of DSSS Generation involves three parameters: Spreading code modulation, Message modulation and redundancy.

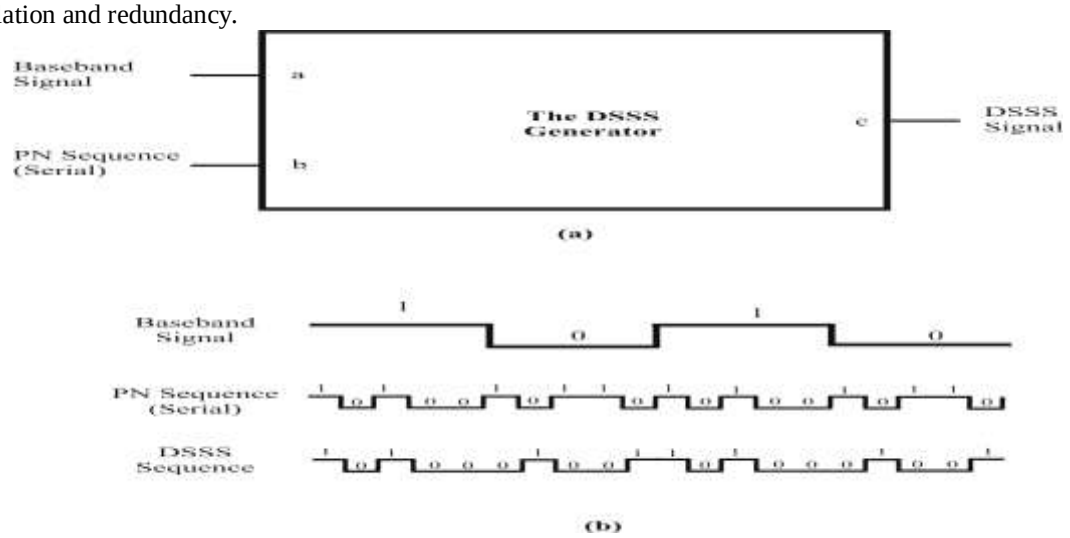


FIGURE 1

a) DSSS GENERATOR

b) DSSS SEQUENCE GENERATIONS WAVEFORMS

For the duration of every message bit, the carrier is modulated (PSK) following a specific sequence of bits (known as chips). The process is known as "chipping" and results in the substitution of every message bit by (same) sequence of chips. In DSSS systems, the spreading code is the chip sequence used to represent message bits.

For message bits "0", the sequence of chips used to represent the bit remains as dictated by chipping process. For message bits "1", the sequence of chips dictated by chipping process, is inverted. In this way message bits "0" and "1" are represented (over the air) by different chip sequences (one being the inverted version of the other one).

Redundancy is achieved by the presence of the message bit on each chip of the spreading code. Even if some of the chips of the spreading code are affected by noise, the receiver may recognize the sequence and take a correct decision regarding the received message bit.

The operation of DSSS Generator of Fig 1 (a) can be observed from the various sequences generated. The DSSS sequence of Fig 1 (b) is generated from the baseband signal and Pseudo Random sequence. A Pseudo Random sequence of five bits (10100) is considered for generating DSSS signal. When the base band signal is 1, the DSSS generator produces an output of 10100. When the baseband signal is 0 the output produce is 01011.

Error detection and correction is efficient in DSSS communication. From Fig 1, we can observe that the output DSSS signal can be either 10100 or 01011. This very feature makes the detection and correction easier thereby making DSSS to be robust.

IV. EXISTING DSSS ARCHITECTURES

A class D amplifier, also known as a switching amplifier using power FETs at output stage is used in DSSS architectures. These devices are attractive in portable electronic gadgets such as mobile phones, MP3 and other PDAs. This architecture is known for its efficiency but it suffers from the problem of electromagnetic inference (EMI) emission, both radiated and conducted in nature. This is because of the switching action at high frequencies. This problem is serious which may degrade power supply quality and disturb the operation of sensitive electronic equipment nearby [6].

V. DSSS TRANSMITTER

As spread spectrum signals are so wide, they are transmitted at a much lower power spectrum density than narrow band transmitters [2].

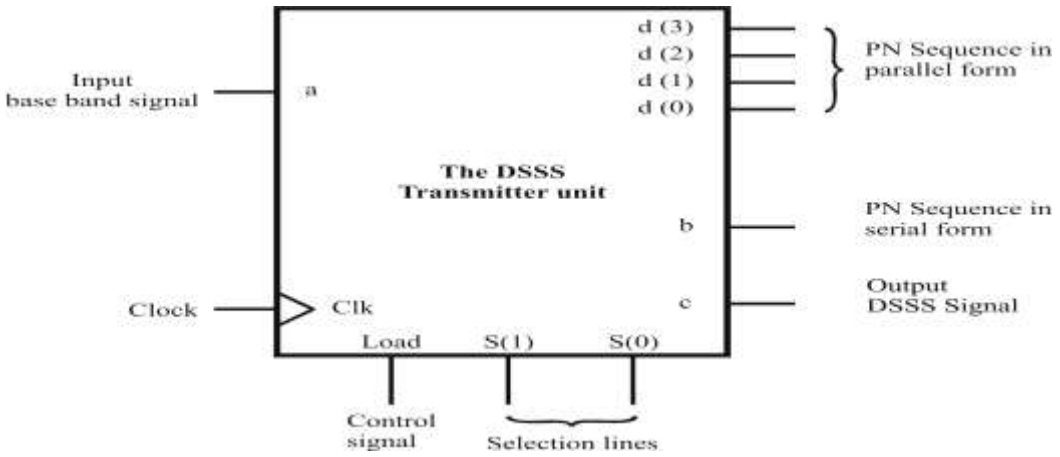


FIGURE 2 DSSS TRANSMITTER UNIT

In this approach, the base band waveform undergoes XNOR operation with Pseudo Random sequence to spread the signal therefore

$$S_{SS} = m(t) \odot p(t) \qquad (1)$$

Where S_{SS} is the DSSS signal,
m (t) is the data signal and
p (t) is the Pseudo Random sequence.

The proposed DSSS transmitter is shown in Fig (2). It contains 4 inputs and 6 outputs. The major input is the input base band signal which is supposed to be spread using automatically generated Pseudo Random sequence. The various blocks of a DSSS transmitter are shown in Fig. 3.

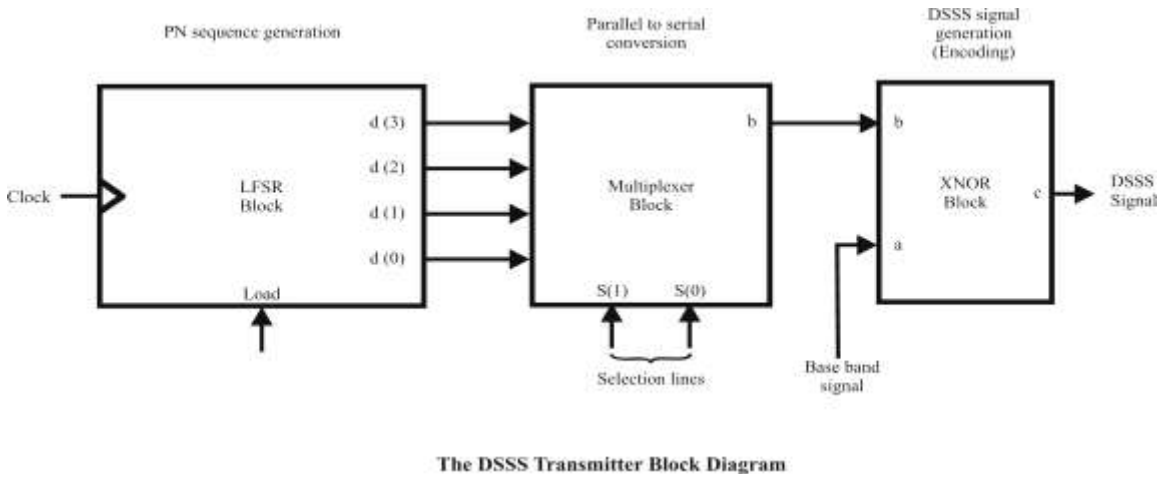


FIGURE 3 THE DSSS TRANSMITTER BLOCK DIAGRAM

It contains an LFSR block for generating a Pseudo Random sequence. The sequence thus generated is in parallel form which needs to be converted into serial form. This serial Pseudo Random sequence and the input baseband signal undergo XNOR operation to generate DSSS Signal.

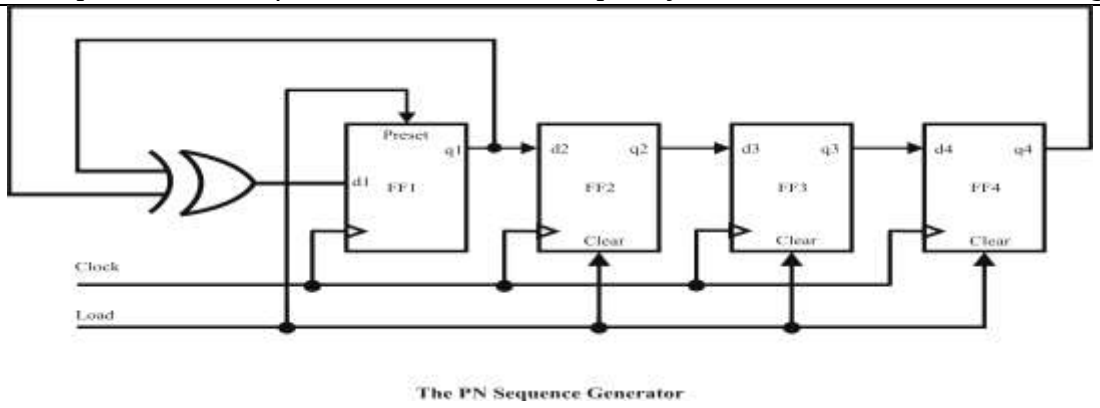
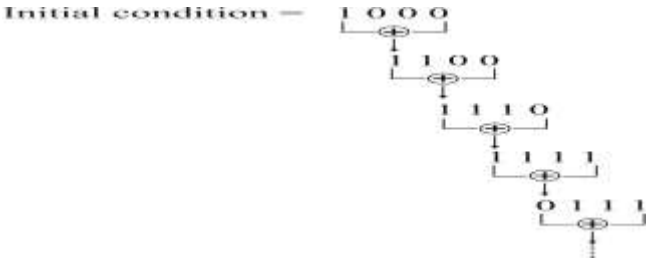


FIGURE 4 PSEUDO RANDOM SEQUENCE GENERATOR

LFSR BLOCK

Internally a Pseudo Random sequence needs to be generated for spreading the message signal. A 4 bit shift register with an XOR gate can serve this purpose. It is preloaded with an input sequence of "1000" as preset is applied to the first flip flop. XOR operation is done on the first and last bits to generate a Pseudo Random sequence. The process is as shown below.



The total set of Pseudo Random sequence codes are given below.

It can be observed that the Pseudo Random Sequence generator, Fig 4, can generate 15 unique codes continuously and then the cycle repeats. These codes are used as Pseudo Random sequence in our design.

The Pseudo Random sequence generated, Fig.4, is in parallel form. The simple 4X1 Multiplexer is used to convert the parallel data into serial data. It multiplexes the 4 input signals depending on the voltage level at the selection lines.

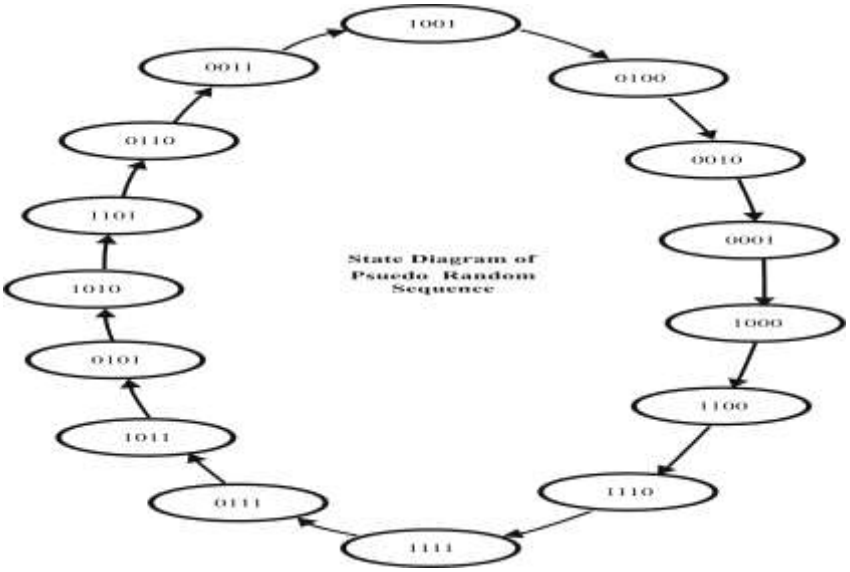


FIGURE 5 STATE DIAGRAM OF PSEUDO RANDOM SEQUENCE

PARALLEL TO SERIAL CONVERSION

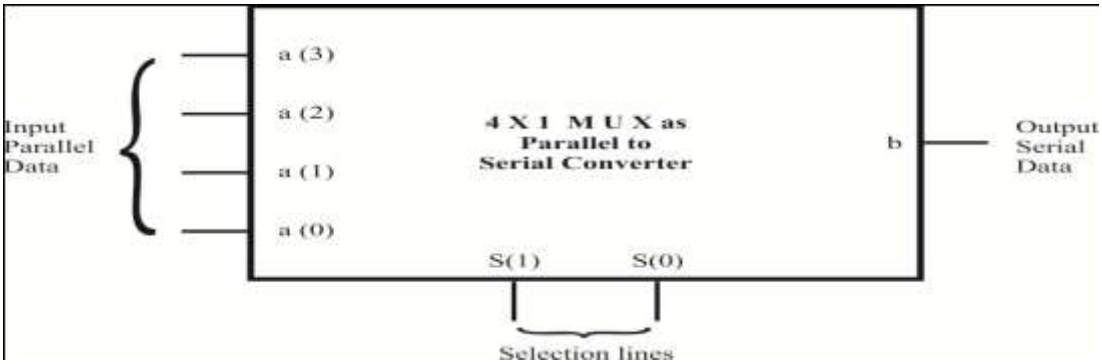


FIGURE 6 PARALLEL TO SERIAL CONVERTER

XNOR BLOCK

In equation 1, we observed that XNOR operation can be used for spreading the signal. The inputs to this block are Pseudo Random sequence and base band signal, Fig 2. It produces the desired DSSS signal.

VI. DSSS RECEIVER

The XNOR Operation between the DSSS signal and the Pseudo Random sequence can retrieve the original base band signal.

$$m(t) = S_{ss} \odot p(t) \qquad (2)$$

The Pseudo Random sequence is used not only for spreading but also for security. As the Pseudo Random sequence, which is used for encryption is shared only by the sender and the receiver, the DSSS communication is highly secure.

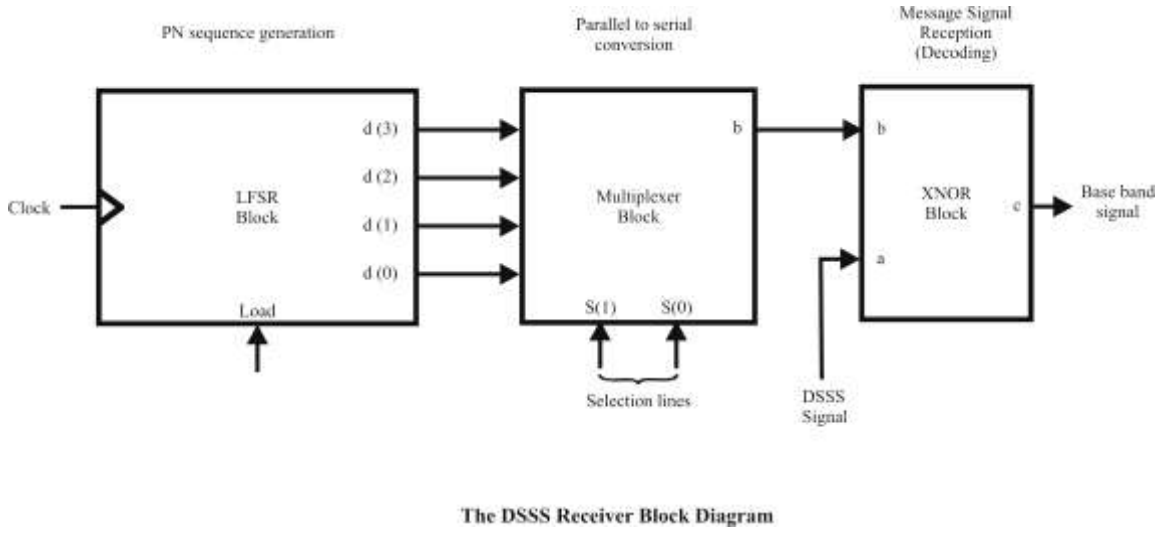


FIGURE 7 DSSS RECEIVER BLOCK DIAGRAM

VII. VHDL IMPLEMENTATION

The structural model VHDL is chosen for the coding of architecture and is implemented on XA9536XL CPLD using XILINX tools. The register transfer level schematic diagram of the transmitter is shown in Fig.8.

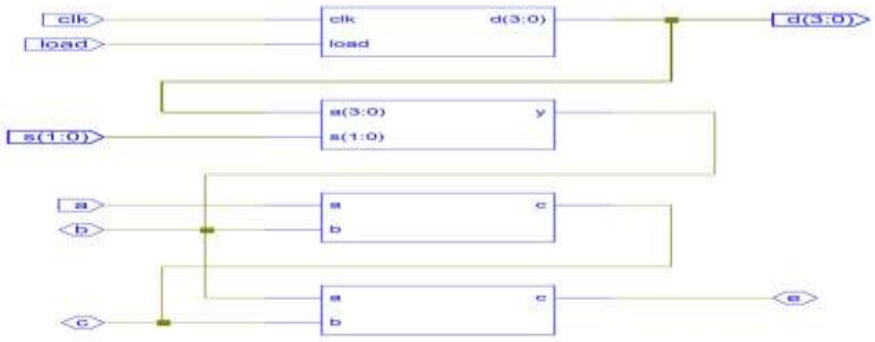


FIGURE 8 RTL SCHEMATIC DIAGRAM OF DSSS TRANSMITTER

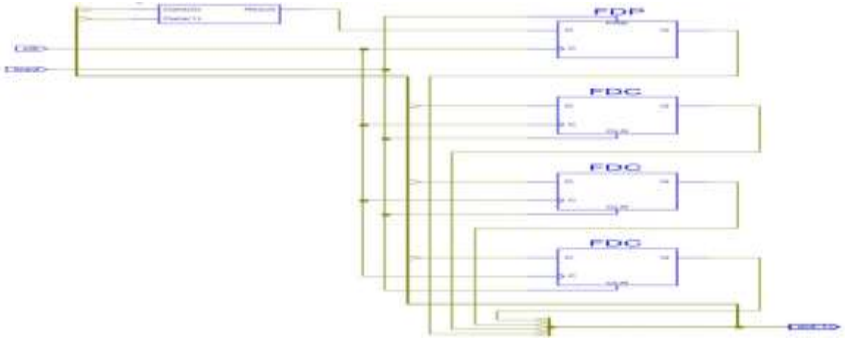


FIGURE 9 RTL SCHEMATIC DIAGRAM OF LFSR

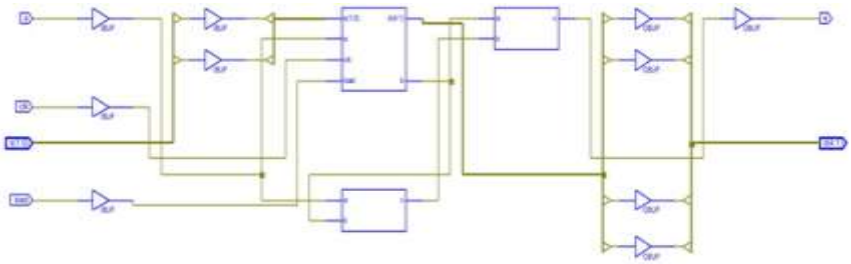


FIGURE 10 TECHNOLOGY SCHEMATIC DIAGRAM OF LFSR

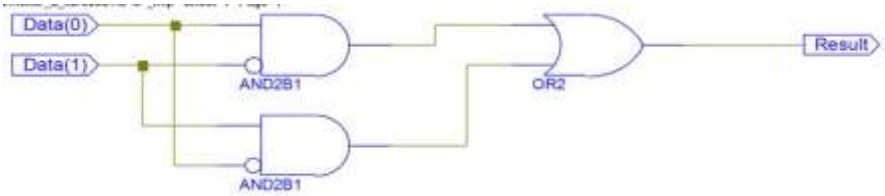


FIGURE 11 TECHNOLOGY SCHEMATIC DIAGRAM OF XOR GATE

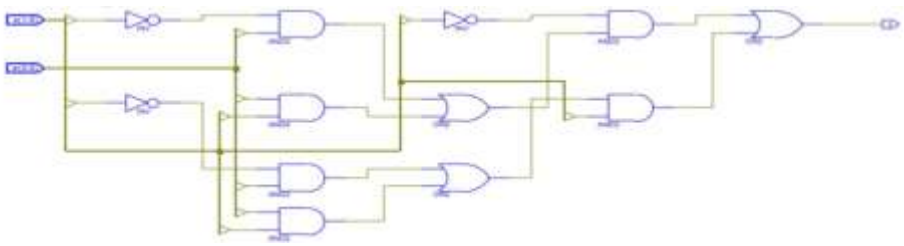


FIGURE 12 TECHNOLOGY SCHEMATIC DIAGRAM OF PARALLEL TO SERIAL CONVERTER

Its internal blocks, i.e. a linear feedback shift register, parallel to serial convertor and XOR, are shown in Fig 9, 10, 11 and 12 respectively.

VIII. SIMULATION AND RESULTS

The test bench setup and the simulation results thus obtained are shown in Fig 13 and 14 respectively.

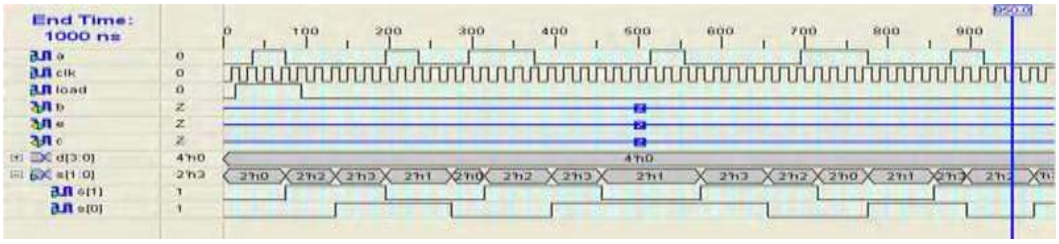


FIGURE 13 TEST BENCH SETUP FOR DSSS TRANSMITTER

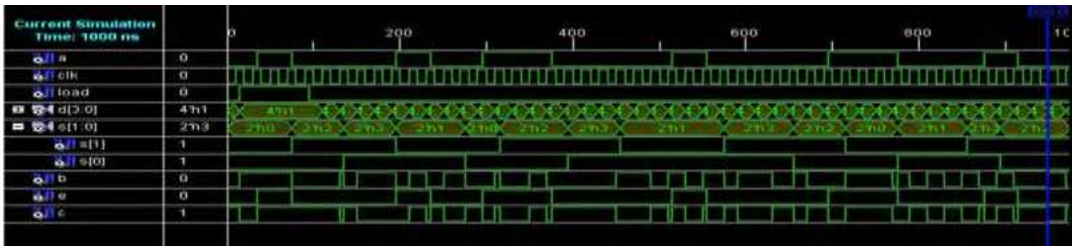


FIGURE 14 DSSS TRANSMITTER OUTPUT WAVEFORM

The results obtained are found to be accurate and physical realization on CPLD ensured minimum delay. It requires only one 4 bit register, one 1 bit 4X1 Multiplexer and three 1 bit XOR gates with 2 inputs. Hence the designed transmitter is of low complexity. It requires low power which can be observed from the fitting summary of CPLD shown in Table 1.

Summary

Design Name	dsss
Fitting Status	Successful
Software Version	J.36
Device Used	XA9536XL-15-VQ44
Date	9-20-2012, 2:51AM

RESOURCES SUMMARY

Macrocells Used	Pterms Used	Registers Used	Pins Used	Function Block Inputs Used
7/36 (20%)	11/180 (7%)	4/36 (12%)	12/34 (36%)	12/108 (12%)

PIN RESOURCES

Signal Type	Required	Mapped	Pin Type	Used	Total
Input	3	3	I/O	10	28
Output	7	7	GCK/IO	1	3
Bidirectional	0	0	GTS/IO	0	2
GCK	1	1	GSR/IO	1	1
GTS	0	0			
GSR	1	1			

GLOBAL RESOURCES

Signal mapped onto global clock net (GCK1)	clk
Signal mapped onto global output enable net (GSR)	load

POWER DATA

Macrocells in high performance mode (MCHP)	0
Macrocells in low power mode (MCLP)	7
Total macrocells used (MC)	7

TABLE 1 FITTING SUMMARY OF THE TRANSMITTER UNIT.

The test bench setup and the simulation results of the DSSS receiver are shown in Fig 15 and 16 respectively.

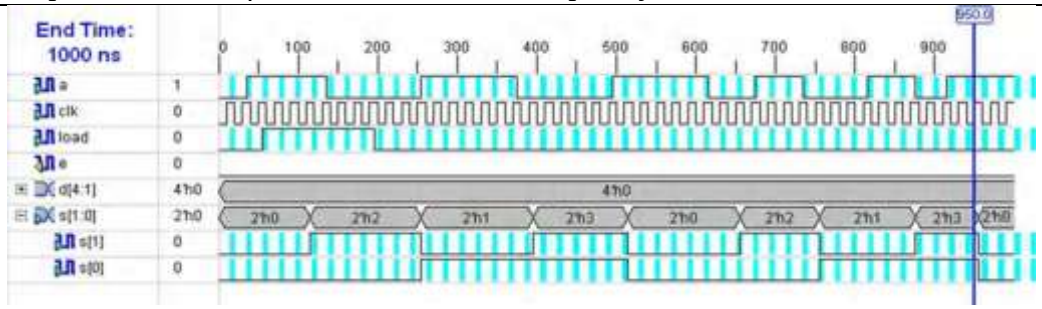


FIGURE 15 TEST BENCH SETUP FOR THE RECEIVER UNIT

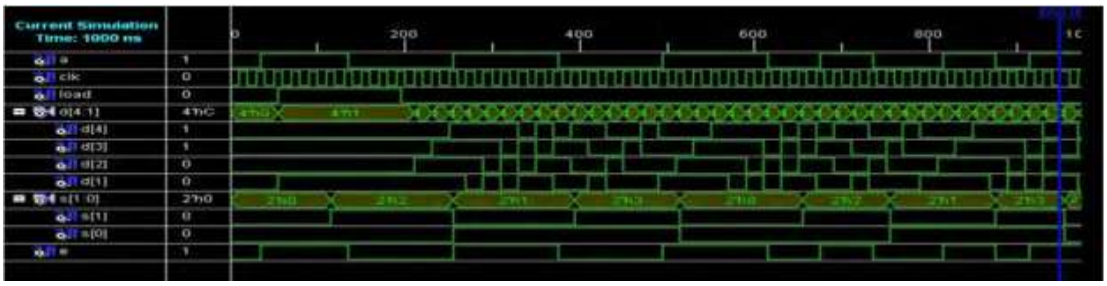


FIGURE 16 RECEIVER OUTPUT WAVEFORMS

Physical realization of these results on CPLD has proved that the implemented design is of low complexity and utilizes less power.

Summary

Design Name	dsssrec
Fitting Status	Successful
Software Version	J.36
Device Used	XA9536XL-15-VQ44
Date	9-20-2012, 2:48AM

RESOURCES SUMMARY

Macrocells Used	Pterms Used	Registers Used	Pins Used	Function Block Inputs Used
5/36 (14%)	5/180 (3%)	4/36 (12%)	8/34 (24%)	5/108 (5%)

PIN RESOURCES

Signal Type	Required	Mapped	Pin Type	Used	Total
Input	1	1	I/O	6	28
Output	5	5	GCK/IO	1	3
Bidirectional	0	0	GTS/IO	0	2
GCK	1	1	GSR/IO	1	1
GTS	0	0			
GSR	1	1			

GLOBAL RESOURCES

Signal mapped onto global clock net (GCK1)	clk
Signal mapped onto global output enable net (GSR)	load

POWER DATA

Macrocells in high performance mode (MCHP)	0
Macrocells in low power mode (MCLP)	5
Total macrocells used (MC)	5

TABLE 2 FITTING SUMMARY OF THE RECEIVER UNIT.

From Table 2, we can observe that the implemented design uses only 14 % of the total available macro cells in the CPLD and all the 5 macro cells used are of low power mode. It is implemented using only 5 slice registers.

IX. CONCLUSION AND FUTURE WORK

From the above simulation, the following results are observed:

- The performance of DSSS system was improved as the design was less complex and has less propagation delay.
- The architecture has the advantage of VLSI implementation which, intern, produces compact DSSS architecture and devices for future needs of 4G communication.
- Finally, the DSSS system has been implemented using lucid structures which are of low cost.

The future scope of this design is to use the implemented architecture along with an efficient modulation technique like QPSK and using it in advanced communication systems.

X. Acknowledgement

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