

Realization of FPGA based numerically Controlled Oscillator

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Abstract : Numerically Controlled Oscillator (NCO) is an important components in many Digital Communication Systems such as Digital Radio and Modems, Software Defined Radios, Digital Down/Up converters for Cellular and PCS base stations etc. A common method for digitally Generating a complex or Real valued sinusoid employs a Look-Up table based scheme. The NCO Design is first simulated and optimized on the software tool Xilinx 10.1 and then coded in VHDL for Hardware Realization. The Designs are tested on Xilinx Spartan2 FPGA Development Platform. The test Results are matching with theoretical and simulated results. This paper presents a FPGA-based Implementation method which can greatly improve the performance, shorten development cycle and reduces cost.

Keywords - Numerically Controlled Oscillator, FPGA, Look-up table, Register

I. INTRODUCTION

Numerically Controlled Oscillator (NCO) is an important component in many Digital Communication Systems such as Digital Radio and Modems, Software Defined Radios, Digital Down/Up converters for Cellular and PCS base stations, etc [1]. Quadrature synthesizers are used for constructing digital down and up converters, demodulators and implementing various types of modulation schemes, including PSK(phase shift keying),FSK(frequency shift keying), and MSK(minimum shift keying).A common method for digitally generating a complex or real valued sinusoid employs a lookup table which stores the samples of a sinusoid. A Digital integrator is used to generate a suitable phase argument that is mapped by the lookup table to the desired output waveform [1].

NCO is a new technology of Frequency synthesis; It is developed the using third generation of Frequency synthesis technology. The technique of NCO is gaining popularity as a method of generating sinusoidal signals and modulated signals in digital systems [2].

In this paper, a ROM-based NCO Architecture with an improvement for QPSK Modem is proposed using the current FPGA technology. This paper is organized as follows, in section II, the basic ROM-based NCO is described and the main challenges of NCO design are discussed. In section III, the NCO Architecture is presented. Implementation and simulation results on Xilinx FPGA are also discussed by comparing with other approaches .Finally; section IV concludes this paper with Summary.

II. OVERVIEW OF NCO

2.1 NCO Architecture

In the simplest case, Numerically Controlled Oscillator is constructed by a ROM with samples of a sine wave stored in it (sine look-up, LUT) [3].Fig.1 shows the block diagram of a NCO system. The NCO produces sinusoidal signals at a given frequency setting word (FSW) which determines the phase step. Once set, this digital word determines the sine wave frequency to be produced. The phase accumulator output than continuously produces proper binary words indicating the instantaneous phase to the table look-up function.

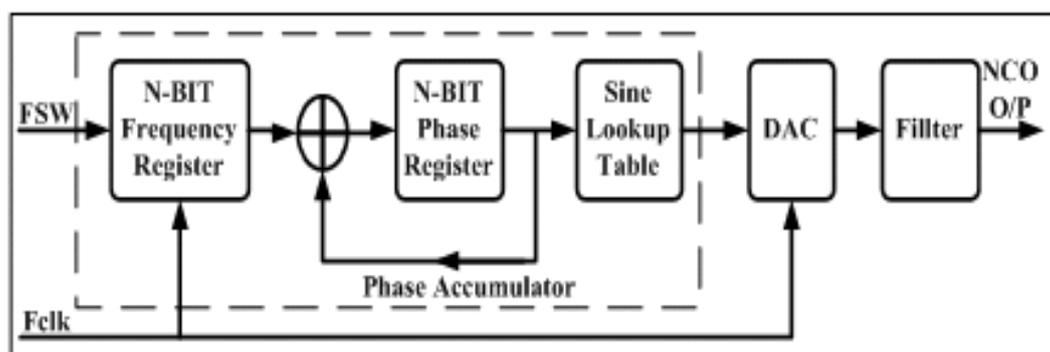


Fig 1. Block Diagram of a NCO system

In other words, the phase accumulator is used to “calculate” the successive addresses of the sine look-up table, which generates a digital sine-wave output. In this way, the samples are swept in a controlled manner i.e. with a step depending on the Frequency Setting Word. The NCO translates the resulting phase to a sinusoidal waveform via the look-up table, and converts the digital representation of the sine-wave to Analog form using a Digital-to-Analog converter followed by a low pass filter (LPF).

The digital part of the NCO consists of the phase accumulator and the LUT. The frequency of the output signal for signal N-bit system is determined by following equation

$$f_{out} = \frac{K \times f_{clk}}{2^N} \quad \text{----- (1)}$$

Where K is the FSW, N is the number of bits that the phase accumulator can handle and f_{clk} is system clock.

2.2 NCO SPECIFICATION

TABLE I

SR NO.	SPECIFICATION	PARAMETER VALUES
1.	Phase Resolution(Bits)	9
2.	Spur level (dB)	54.18
3.	Frequency Resolution(Bits)	24
4.	Output signal	Sine & cosine
5.	Output Data Width	9 bits

Table-I give the Design Specification of NCO- MATLAB Simulink model is developed to meet the designed specifications. As Shown in fig 2 simulink model of NCO.

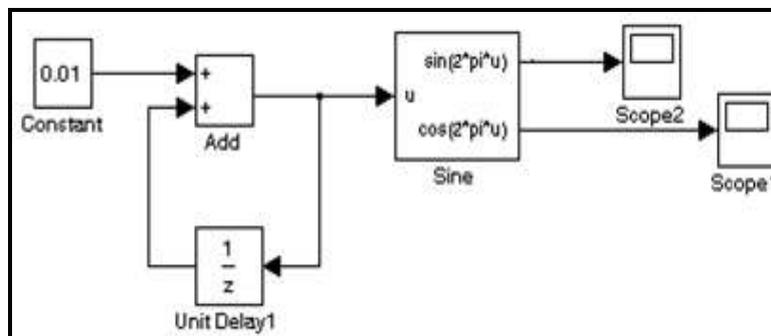


Fig. 2 Simulink model of NCO

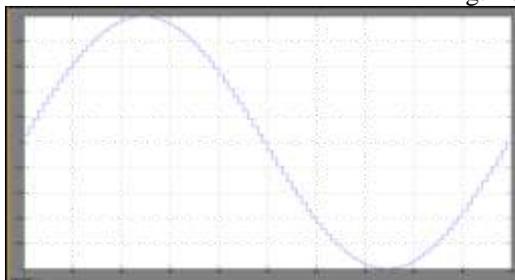


Fig. 3 sine waveform of a NCO

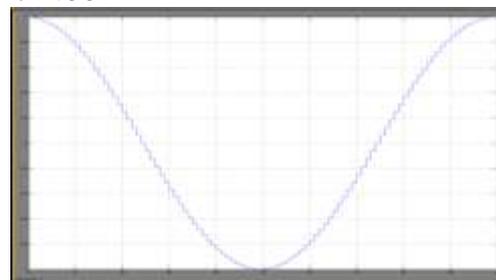


Fig. 4 cosine waveform of a NCO

III. DESIGN AND FPGA IMPLEMENTATION

We have used Xilinx ISE10.1 Environment for synthesis as well as simulation. It supports both VHDL and Verilog design flow. Bit file is generated for XC2S200 development board.

3.1 VHDL realization

Configuration register is defined to control the NCO frequency. The design needs system clock, sample clock and FSW and produces both sine and cosine wave form. Phase is incremented at each sample clock and corresponding sin/cosine value is fetched from the sin/cosine ROM table and produced at output port. Fig 5 Shown the VHDL module of NCO.

3.1.1 Simulation results

Test bench is written for 2.5MHz frequency. Output and internal signals are captured in ISIM simulator. Fig 6 shows the functional simulation results of NCO.

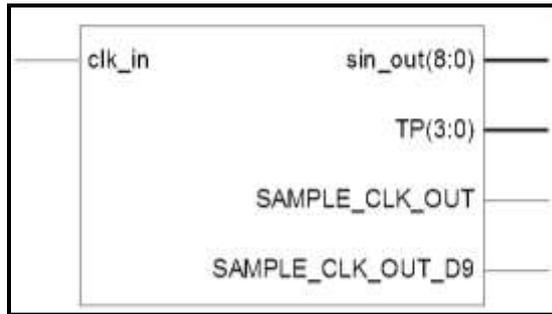


Fig.5 VHDL module of NCO

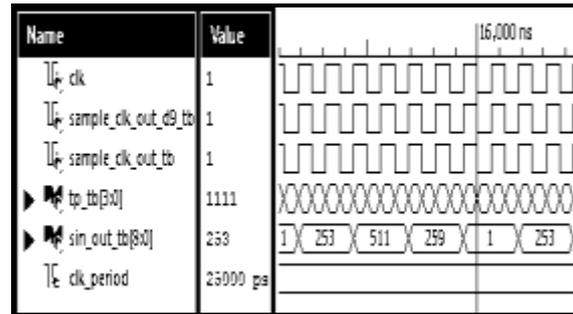


Fig.6 The output wave form of NCO

3.1.2 Results of hardware verification

The SPARTAN-2 FPGA development board is programmed with load bit file through JTAG [4]. The digital information provided to the DAC must represent the instantaneous amplitude of the RF waveform. NCO Hardware test set up was made as Shown in fig 7 and output was observed on spectrum analyser as well as oscilloscope. The implementation details of 24 bit FSW is shown in TABLE II. Various frequencies have been generated to check different parameters of NCO.

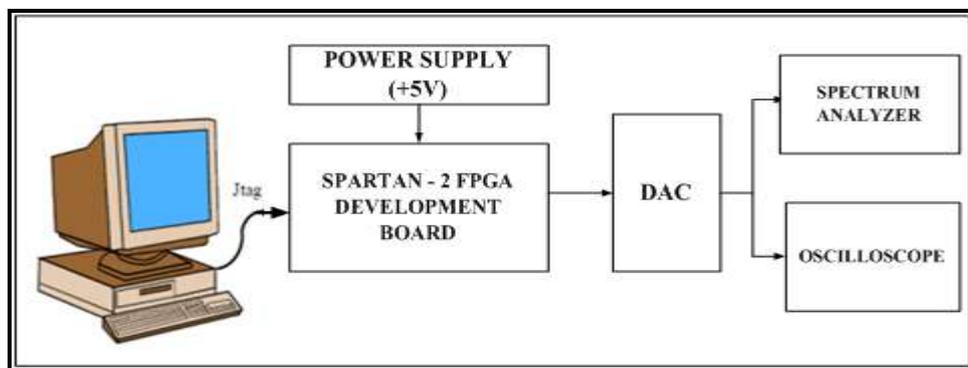


Fig.7 Block Diagram of Experimental Setup

TABLE II
FPGA IMPLEMENTATION RESULTS

SR NO.	HEX Values	Decimal Values	NCO Center Frequency(MHz)	Spectrum's observe Value(MHz)
1	100000	1048576	1.250000	1.249992
2	110000	1048592	1.328125	1.328127
3	200000	2097152	2.500000	2.500000
4	400000	4194304	5.000000	5.000000
5	400001	4194305	5.000001	5.000001
6	400010	4194320	5.000019	5.000019
7	600000	6291456	7.499963	7.499963



Fig.8 The output signal of NCO implemented in FPGA

Fig 8 Shows the example of NCO Signal captured at 2.5 MHz on the spectrum analyser.

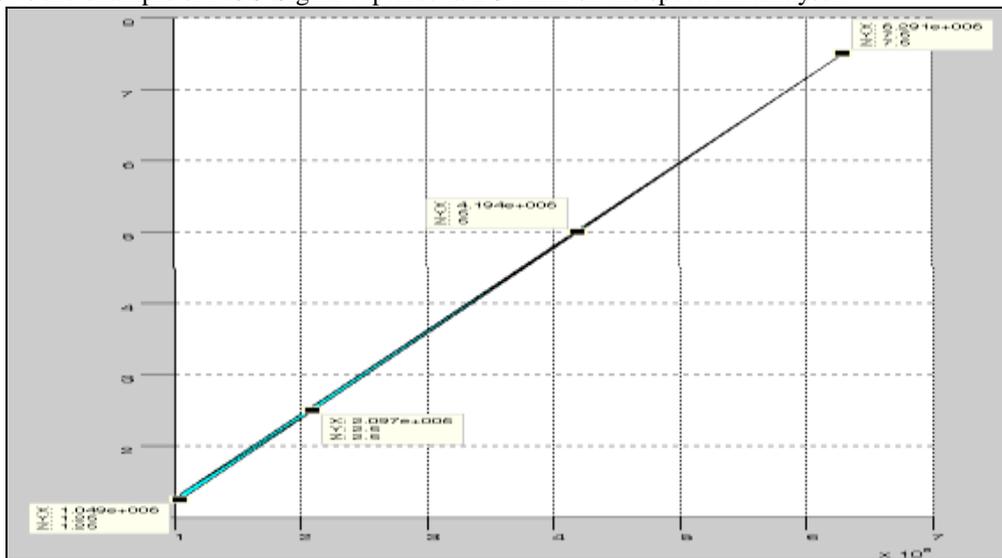


Fig.9 MATLAB Simulation Results

MATLAB results are shown in fig 9, where in Frequency spectrum is observed for wide Range of FSW and graph is plotted. The hardware results and simulation results match each other. The results have also been verified on Digital Storage oscilloscope and Spectrum analyzer.

IV. CONCLUSIONS

This paper presents the simulation and Implementation of NCO. The Design and Realization of NCO include sub modules like phase Accumulator and Look-Up Table. Area resources are optimized by using Coefficients for only quarter cycle of sinusoidal waveform and for remaining part the same has been flipped and for negative cycle it has been inverted. This NCO is designed to be used for the Costas loop [5].

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