IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 10, Issue 5, Ser. I (Sep. - Oct. 2020), PP 25-31
e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197
www.iosrjournals.org

10-Bit 1-MSB Current Steering Digital Analog Converter Utilizing Op-Amps as A Load

Mohd Azim Mohammad Alias, Mohd Tafir Mustaffa
(School of Electrical and Electronic Engineering, Universiti Sains Malaysia, Engineering Campus 14300, NibongTebal, Pulau Pinang, Malaysia)
Corresponding Author:Mohd Tafir Mustaffa

Abstract:
In this research, the Dynamic Element Matching Technique (DEM) algorithm is used, known as Partial Binary Tree Network (PBTN), been proposed from previous research that aims to push the boundaries from 8-bit to 10-bit. PBTN is used because it has a lower complexity circuit and fewer glitches produced at the output signal. Besides, in this research, the Current Controlled Current Source (CCCS) used to magnify the output in previous research is replaced with an operational amplifier (op-amp). The 8-bit 1-MSB achieved a power consumption of 16.7 mW, much lower compared to the previous research. For 10-Bit 1-MSB, the circuit achieved DNL of -0.535378495 LSB, INL of 0.955382 LSB, with a power consumption of 66.31 mW.
Keywords:*Partial Binary Tree Network, Dynamic Element Matching, current steering DAC, INL, DNL,10-BIT 1-MSB*

Date of Submission: 25-11-2020 Date of Acceptance: 09-12-2020

I. Introduction

In the world of integrated circuit (IC) designs, uncertainties in photolithographic edge definition is inevitable, result in mismatch value of components such as resistor ratios. Moreover, temperature gradients across the circuit, alignment error, component aging, and component noise could cause a component mismatch. Several techniques were applied and introduced to reduce the effects of component mismatch errors such as special VLSI layout techniques, laser trimming, digital calibration, self-calibration, error averaging, or element sizing [1].

In this research, a Dynamic Element Matching Technique (DEM), Partial Binary Tree Network algorithm (PBTN) is used which was introduced in previous researches [2-5]. PBTN is a DEM algorithm which possesses relatively lower hardware complexity. The design of such a technique requires much fewer transmission gates compared to conventional Binary Tree Network (BTN); hence,offeringmuch lower hardware complexity and reduced glitches.

Previous research in [3] had designed and validated up until 8-bit 1-MSB PBTN DEM DAC.This leaves PBTN of higher bits to be designed and validated in this work.

II. Methodology

This work aims to redesigntwo 8-bit PBTN DEM DACs based on the work done in [3] using the op-amps andCurrent Controlled Current Source (CCCS)as a load and to increase the resolution from 8-bit to 10-bit. The following discusses the step by step of the design and implementation of the PBTN DEM DAC.

Design of 10-bit 1-MSB PBTN

In general, a B-bit PBTN will require a 2^B unit of DAC and with a total number of $(2^{B+1}-2)$ transmission gates [2]. To build 10-bit 1-MSB PBTN, lower stages are to be constructed in the hierarchical method, starting with 3-Bit 1-MSB PBTN, which is proceeded by 4-bit, 5-bit, 6-bit, 7-bit, and then 8-bit and 9-bit. The design of 3-bit 1-MSB PBTN is illustrated in Figure 1, revisited here from work in [3].

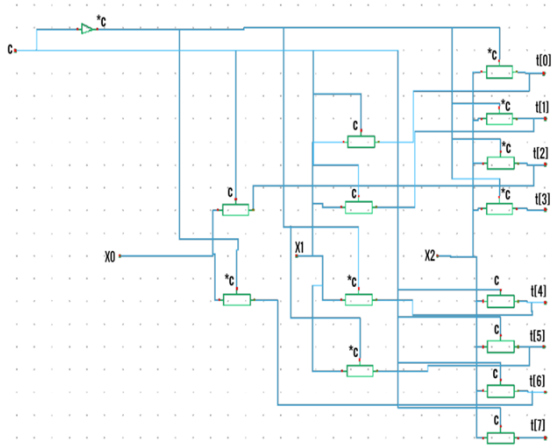

Figure 1. 3-Bit 1-MSB PBTN [3]

After 3-bit PBTN is established, 4-bit PBTN can be built by connecting two of 3 bit 1-MSB PBTN. The first 3 bits of binary code input was connected to 2 blocks of 3-bit 1-MSB PBTN. LSB X0 of the input bit was connected to 2 extra transmission gates, and its output was connected to output line t3 and t7 as shown in Figure 2. The 10-bit 1-MSB PBTN can be built after 9-bit PBTN is established.

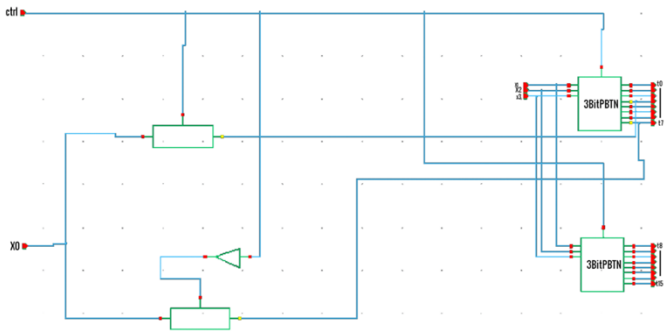

Figure 2.4-Bit 1-MSB PBTN [3]

Operational Amplifier (Op-amps)

Op-amps are used in this research to magnify the output current from DAC and to convert it to output voltage. In this work, the output voltage is designed to be 1V. For this purpose, two types of op-amps are used which are transimpedance amplifier (TIA) and inverting amplifier.

Figure 3 shows the configuration of the TIA.TIA is providing simple linear signal processing using an op-amp and a resistor for dissipating current. The current from DAC can be calculated by using Eq. (1) where N is the number of bits and the Vout is derived from Eq. (2). The Eq. (2) is obtained when using Kirchhoff's Current Law (KCL), in which the sum of all currents flowing into a node is zero and by assuming that the op-amp is ideal meaning no current flows into the op-amp +/- inputs [6-7]. The value of the resistor (R) depends on the number of bits of the DAC in which can be calculated by using Eq. (3)as the targeted value for output voltage is 1V.

$$I = (2^N - 1) \times 20uA \quad (1)$$

$$I + \left(\frac{Vout - 0}{R}\right) = 0 \quad (2)$$

$$Vout = -IR (3)$$

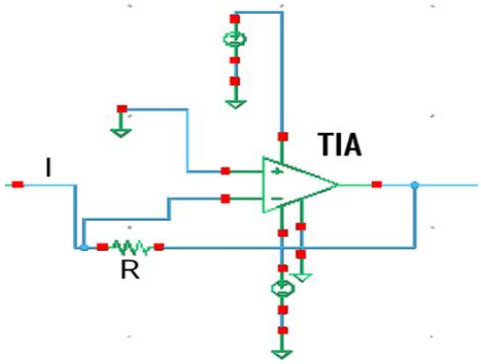

Figure 3. Configuration of TIA

Figure 4 shows the configuration of the inverting amplifier. Since the output voltage produced from the TIA is negative, the inverting amplifier is needed to invert the output voltage to be 1V. There are two resistors used in this configuration which are Rin and Rf. The voltage gain of the amplifier can be calculated by using Eq. (4). The voltage gain for this project is set to be -1 so that it will not interrupt the output voltage from TIA. Thus, the values of Rin and Rf are set to be the same 10K ohm as an ideal option. The output voltage, Vout for the PBTN DAC can be calculated by using Eq. (5).

$$Gain\ (Av) = -\frac{Rf}{Rin} \quad (4)$$

$$Vout = Av \times Vin \quad (5)$$

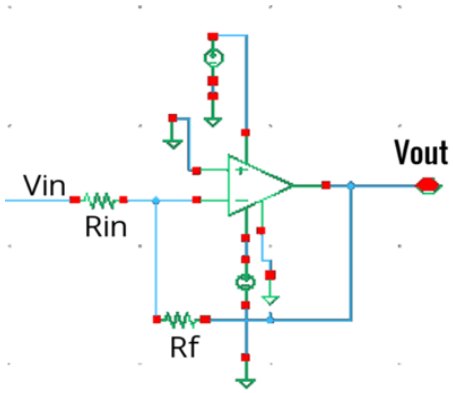

Figure 4. Configuration of Inverting Amplifier

10-Bit 1-MSB PBTN DEM DAC

Figure 5 shows the block diagram of 10-Bit PBTN DEM DAC with an input code of X0 to X9 and 1024 current steering DAC. Figure 6 shows the 10-Bit PBTN DEM DAC connection in Cadence. Input X0 to X9 are varied from bits '0000000000' to '1111111111' by using a Vpulse. The Vpulse period of the control bit is set to 256 ms to emulate the random bit. Table I shows the Vpulse period of each input code X0 to X9.

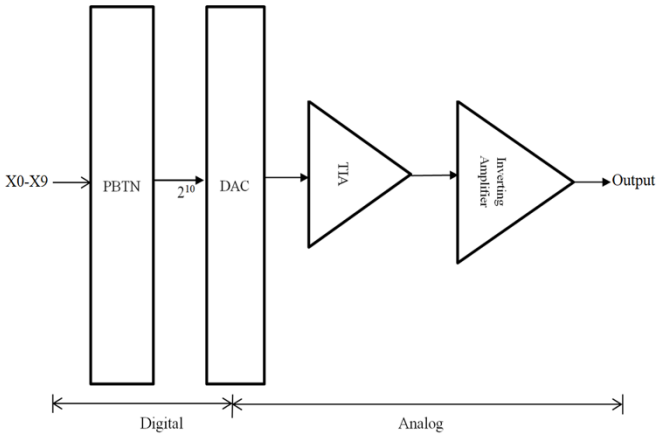

Figure 5. Block Diagram of 10-Bit PBTN DEM DAC

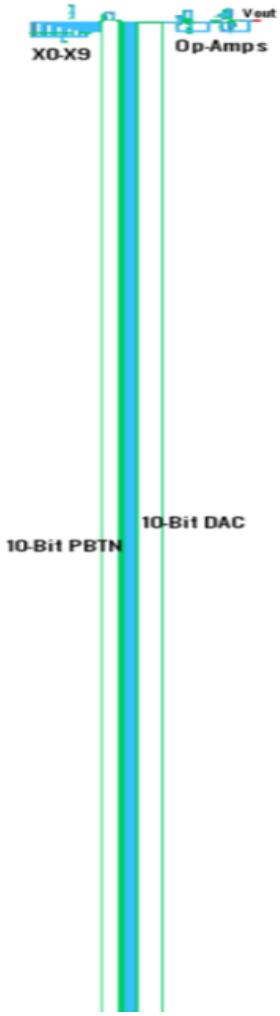

Figure 6.10-Bit PBTN DEM DAC in Cadence

Table I. The period of each Vpulse

Input code	Period (ms)
X0	1
X1	2
X2	4
X3	8
X4	16
X5	32
X6	64
X7	128
X8	256
X9	512

III. Results

The simulation result of 10-bit 1-MSB PBTN DAC is shown in Figure 7. From the simulation, this design has an offset error of 7.979 mV. The maximum glitch is 507.94 mV at 258.1 ms and this happens when digital inputs transition from '0111111111' to'1000000000'. The output voltage achieved the target which is 1.023 V. The extracted simulation data of the output of 10-bit 1-MSB PBTN has INL of 0.955382 LSB and DNL of -0.535378495 LSB and the maximum dynamic power consumption is 66.31 mW, shown in Figure 8.

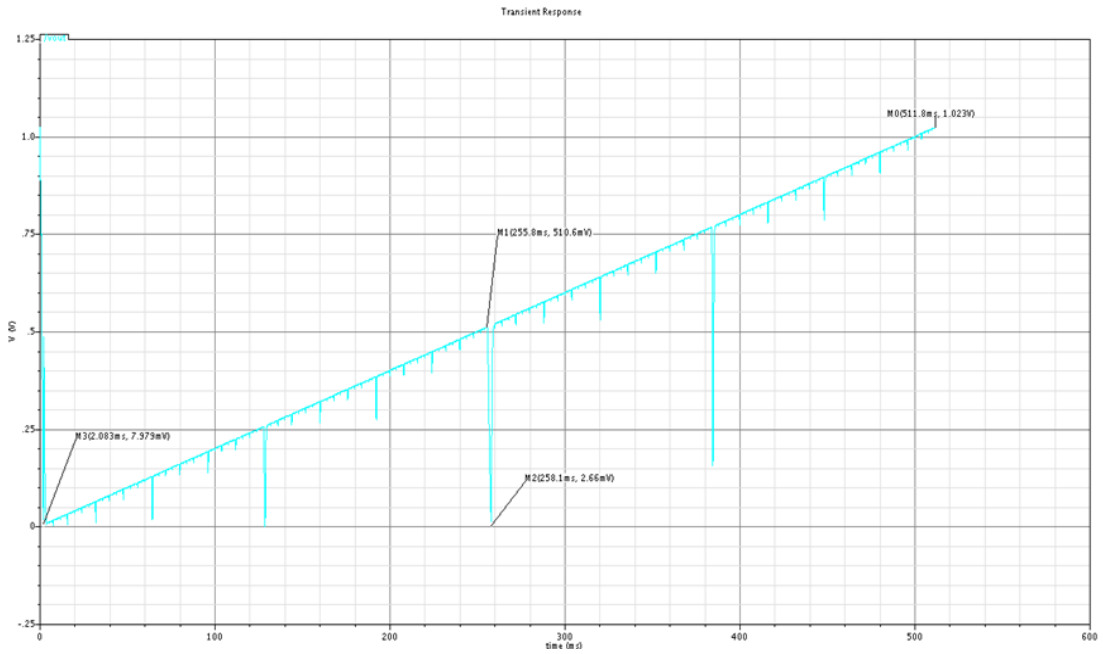

Figure 7. Simulation results of 10-Bit

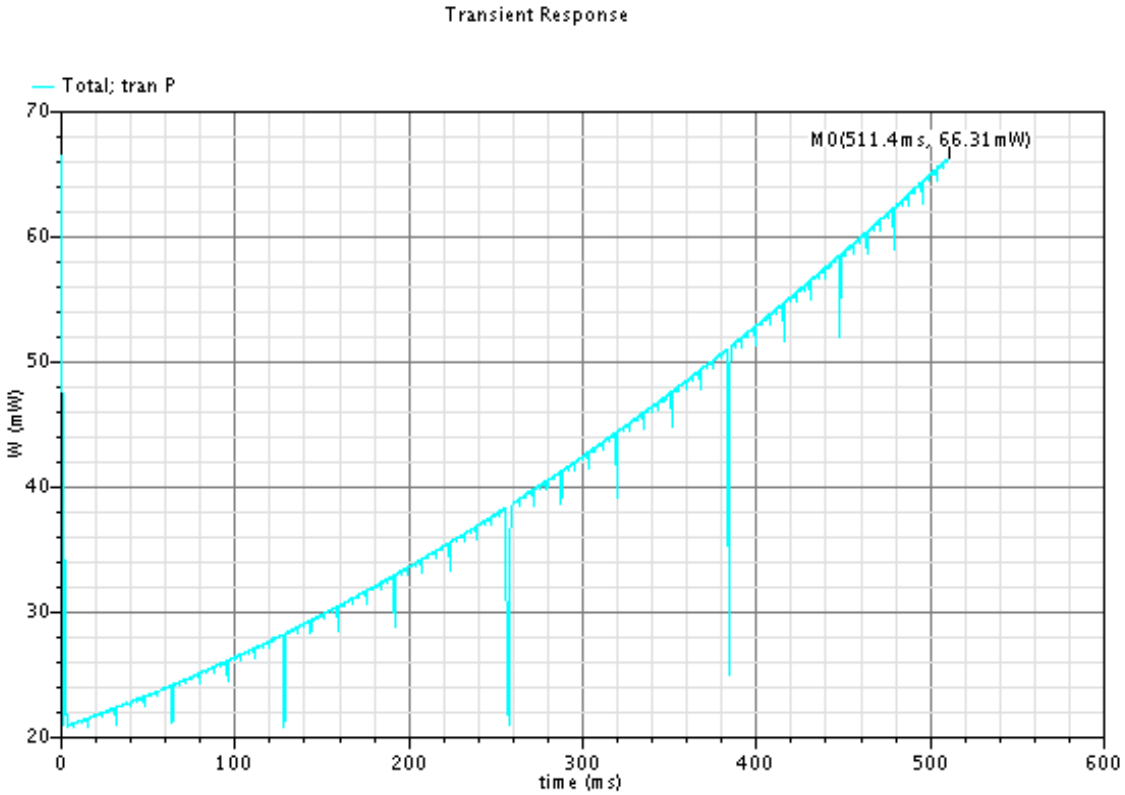

Figure 8. Dynamic power consumption of 10-Bit PBTN DAC

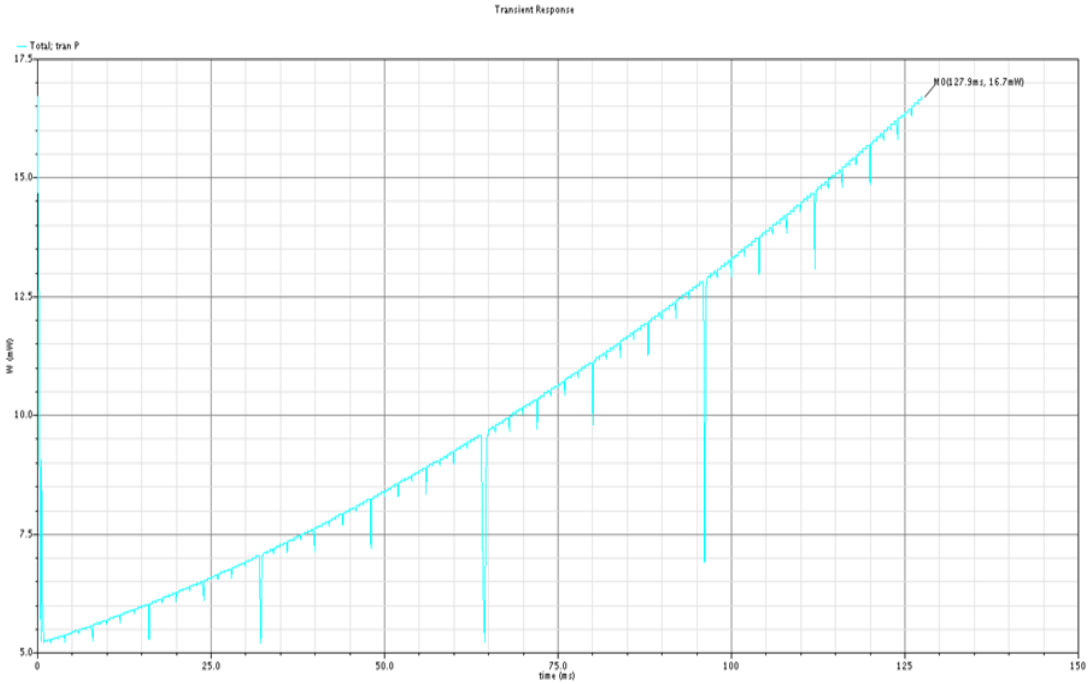

Figure 9. Dynamic power consumption of 8-Bit PBTN DAC

The simulation results of both dynamic power consumption of two 8-bit 1-MSB PBTN DACs is shown in Table II and Figure 9(only DAC with op-amps is shown here) respectively. The 8-Bit DAC with op-amps achieved the maximum power consumption of 16.7mW versus the power consumption of 115.4 mWof the DAC with CCCS. The use of Op-amps achieved much lower power consumption as compared to CCCS with a difference of 98.7 mW or a reduction of about 86%.

Table II. Simulation results comparison

Specification	**Previous Method:** CCCS [3]	**This research:** Op-Amps
Power **Consumption**	115.4mW	16.7mW

IV. Conclusion

This research aimed to design and simulate 8-bit PBTN DEM DAC in terms of power consumption in which also validates the concept of PBTN which is a form of DEM, performed by previous research. In terms of power consumption, this research has been successfully improved to provide much lower power consumption.

Another goal of this research is to push the limits of PBTN into producing higher resolution outputs. The design and simulation of the 10-Bit 1-MSB PBTN successfully produced a promising result. The simulation of the 10-bit is evaluated in terms of INL, DNL, and power consumption.

This research also made a significant change in which the CCCS from previous research was replaced with the op-amps. As a result of the change, the power consumption of PBTN DAC reduced much lower.

The limitation encountered in this research is to ensure that the output voltage achieves the target 1V. Thus, the selection of suitable type and configuration of the op-amps and the chosen values of the resistors must be proportional to the output voltage.

Acknowledgments

The authors would like to thank Universiti Sains Malaysia for funding this work under Research University Individual (RUI) grant number (1001/PELECT/8014010) and CEDEC USM for providing the facilities to do this work.

References

[1]. Robert Gregoire, B. & Moon, U.K. Reducing the effects of component mismatch by using relative size information. Proceedingof the IEEE International Symposiumon Circuits and Systems. 2008;512-515.
[2]. Mustaffa, M. T., Lim Y. C., Teh C. Y. Current Steering Digital Analog Converter with Partial Binary Tree Network (PBTN). Indonesian Journal of Electrical Engineering and Computer Science. 2017;5(3):643-649.
[3]. William Yeap, K.S.& Mustaffa, M. T. A 0.13-um 6 to 8-bit PBTN DEM Current Steering DAC. IOSR Journal of VLSI and Signal Processing.2019;9(5):1-10.
[4]. Myderrizi, I. &Zeki, A. Current-Steering Digital-to-Analog Converters: Functional Specifications, Design Basics, and Behavioral Modeling. Antennas and Propagation Magazine, IEEE.2010; 52:197-208.
[5]. Galton, I. Why Dynamic-Element-Matching DACs Work. IEEE Transactions on Circuits and Systems II: Express Briefs. 2010; 57:69-74.
[6]. Bruce, C. & Ron, M.Op-Amps for Everyone.5th Edition, Newnes.2017.
[7]. Tavernier, F.&Steyaert, M. From current to voltage—The transimpedance amplifier. In: High-Speed Optical Receivers with Integrated Photodiode in Nanoscale CMOS. Analog Circuits and Signal Processing. vol 5. Springer, New York, NY. 2011.

Mohd Tafir Mustaffa, et. al. "10-Bit 1-MSB Current Steering Digital Analog Converter Utilizing Op-Amps as A Load." *IOSR Journal of VLSI and Signal Processing (IOSR-JVSP),* vol. 10, no. 5, 2020, pp. 25-31.