

## VHDL-AMS Macro models of MOSFET. Consideration of Gate Length Variability And Single-Electron-Transistors

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**Abstract :** *The integrated circuit/system designers are faced with problems that involves nano-scale devices with far less than ideal characteristics, very high integration densities (i.e. giga-scale complexity), very high operation speeds and data transmission rates, and system-level integration of analog and digital functions. The single-electron tunnelling (SET) devices might be scaled down almost to the molecular level. Gate length variability due to intra or inter die variations can lead to considerable mismatch between devices even inside the same chip. This variability has to be considered in detail and new device models should be developed, aiming in modelling its effects on the electrical characteristics of the devices. In the current article, a simple mosfet model is extended to incorporate gate length variability. The model is coded in VHDL-AMS in order to be used for simulation of circuit behavior within the framework of suitable system simulation software. Also first results of VHDL-AMS macro-modelling techniques for the compact simulation of single-electron circuits are presented. The macromodel of the SET, which is much more efficient than the corresponding Monte-Carlo calculations, is developed and can become a reasonably accurate tool for the simulation of complicated single-electron circuits.*

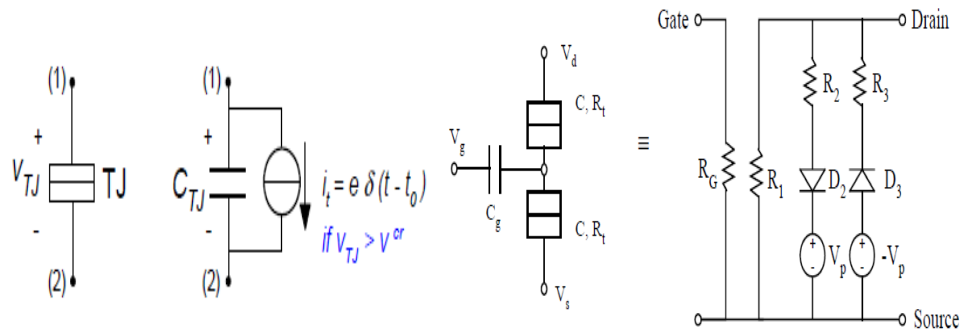
**Keywords:** *mosfet, line-width-roughness, vhdl-ams, digital-gates, single-electron-transistor, coulombblockage, compact-device-modelling*

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### I. Introduction

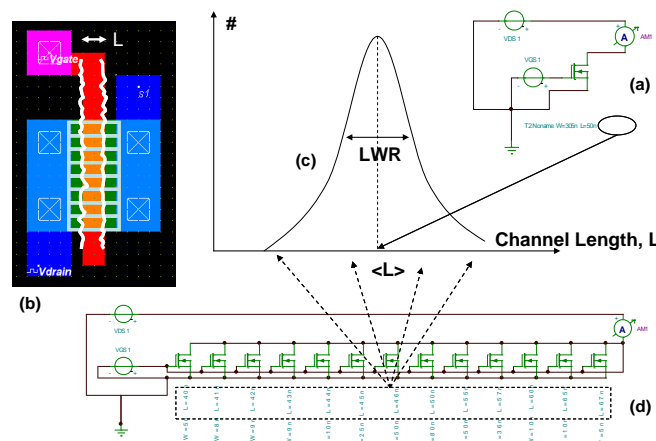
According to technology roadmap, semiconductor device dimensions are shrinking to lower than 10 nm, introducing a wide range of design challenges in terms of accurate modelling of device and interconnect behavior, robustness and reliability. At the same time, the number of devices in integrated systems (System-on-Chip, SoC) will continue to increase at an exponential rate, far exceeding 1 billion devices. Thus, the integrated circuit/system designers are confronted with a multi-faceted problem that involves nano-scale devices with non-ideal characteristics, very high integration densities (i.e. giga-scale complexity), very high operation speeds and data transmission rates, and system-level integration of analog and digital functions. Gate length variability, in the form of line-width roughness (LWR), due to intra or inter die variations can lead to considerable mismatch between devices even inside the same chip. This variability has to be considered in detail and new device models should be developed, aiming in modelling accurately the electrical characteristics of the devices under the presence of quantifiable LER or LWR. Single electron device effects should also be considered and reliable models should be provided as well, to the designer of next generation circuits.

The single electron transistor (SET) junction consists of two conductors with a very thin insulator in between (Fig. 1a). This structure therefore could behave like a normal capacitor when no tunnelling occurs. However, due to the extremely thin insulator, tunnelling of electrons through the insulator becomes possible. The typical feature sizes of the SET devices are in the nanometer range, therefore SET devices belong to the group of nano-electronics. SET devices can be faster and consume less power than comparable devices implemented in CMOS or bipolar technologies. An equivalent circuit model has been developed for a single SET junction. This model is called the impulse circuit model for a single SET junction (Fig 1a). The model is suitable for both circuit analysis and design purposes. Basically, the impulse circuit model consists of a lumped capacitor with a delta-function current source placed in parallel to it. When the voltage across the SET junction exceeds a certain critical voltage, the current source is triggered and a charge of one electron, which equals the elementary charge  $e$ , is effectively transferred between the nodes of the SET junction. When the voltage across the junction is below the so called 'critical voltage level', the value of the current source equals zero and the model behaves like a true capacitor. A single-electron transistor can be designed using two SET junctions as shown in Fig. 1b [1].



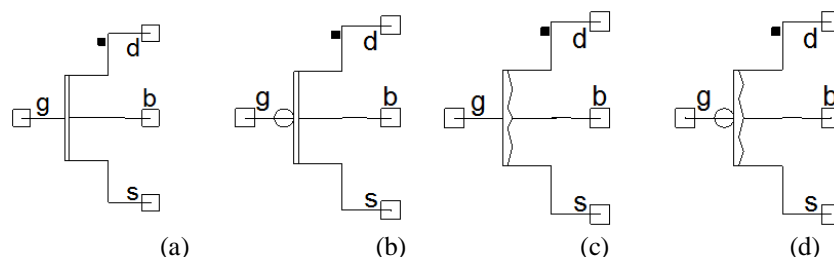
**Figure 1.** (a). Macro-modelling of an single-electron tunnelling junction. (b) The equivalent circuit of a single-electron transistor and its SPICE macro-model.

In the current work a simple mosfet model is extended to incorporate gate length variability [2]. This is introduced by segmenting the device width into sub-units following a Gaussian gate length distribution, with controlled LWR. Figure 2 shows a qualitative example of a mosfet-gate layout with LWR. The mosfet macromodel is coded in VHDL-AMS in order to be used for simulation of circuit behavior within the framework of suitable system simulation software. Initially, a VHDL-AMS model of ideal nmos and pmos transistor are defined and then they are used to create the basic digital gate of the inverter. Gate length variability is introduced in the basic models of nmos and pmos so as to be possible to quantify its effects on digital gates functionality. Along this line of work, one can use more elaborate state-of-the-art models of the mos transistor more appropriate for the gate lengths currently used in semiconductor devices. The equations and second order phenomena should have to be updated, but the presented process of creating the transistor models is the same..



**Figure 2.** (a) Conventional designs assume constant  $L, W$  values for the devices. (b), (c) Process variability results in gate length variability. (d) An accurate representation of the nmos device shown in (a), with LWR consideration.

Finally, as a second example of the applicability of VHDL-AMS abilities, a macromodel of a SET is developed and its successful simulation is presented.



**Figure 3.** Mosfet symbols used in this work (a) ideal nmos, (b) ideal pmos, (c) nmos with LWR, (d) pmos with LWR.

**Vhdl-Ams Implementation of Simple Pmos And Nmos**

Every VHDL-AMS implementation of a device model, consists of an entity and an architecture. The entity is a representation of the inputs and outputs of the device as well as of any generic physical parameters required for its simulation. All entities have a generic part and a port part. Figure 3a and Fig. 3b show the symbols of ideal nmos and pmos and (c) and (d) their corresponding symbols when LER is taken into account.

The name of the entity is different in each case to define each different device. The nmos and pmos with LER have one more generic parameter, the LER of their channel length. The way each model performs, is described in the corresponding architecture. In this work each architecture describes device behavior using simple semiconductor physics equations. The corresponding models can be made as advanced as are required, simply by increasing the complexity of the corresponding equations describing current - voltage relationships through incorporating second order or short channel effects. Table 1 shows an example of entity – architecture for the ideal nmos.

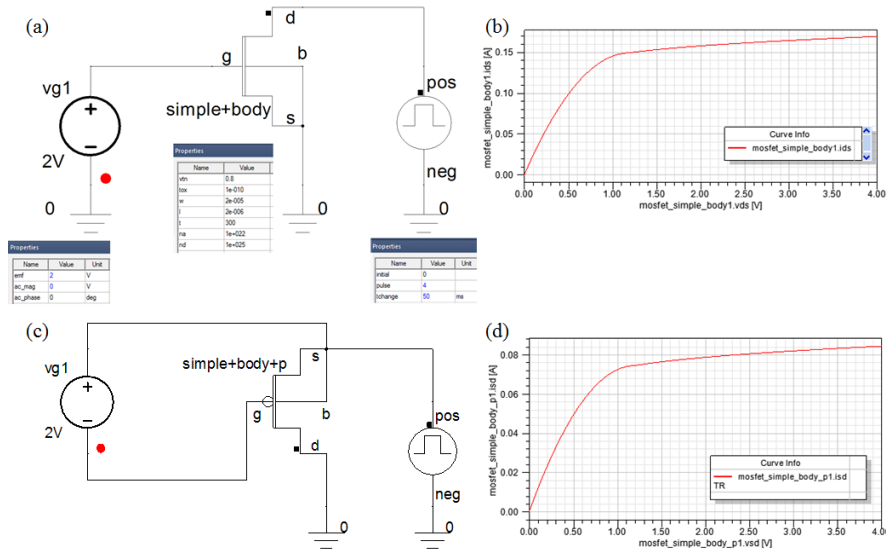
The architecture should reference only one entity. All required constants and temporary variables needed should be defined in the architecture’s block space. Physical constants are defined before the “begin...end” part of the architecture body and used in the definition of functions and concurrent equations later in the architecture-body. Quantities represent the variables that describe the voltages and currents of the device and have to be defined using the keywords “across” and “through” (for voltage and current respectively) by referencing appropriately the port terminals of the entity. Functions could be defined as needed, in order to make code readability and manipulation easier.

<pre> LIBRARY Ieee; use Ieee.electrical_systems.ALL; use Ieee.math_real.ALL; ENTITY mosfet_simple_body IS generic ( Vtn : real := 0.8; -- threshold voltage in V tox : real := 1.0E-10; -- oxide thickness in m W : real := 20.0E-6; -- device width in m L : real := 2.0E-6; -- device length in m T : real := 300.0; -- [K], temperature NA : real := 1.0E22; -- [holes/m3], acceptor concentration ND : real := 1.0E25 -- [electrons/m3], electron concentration ); port (terminal g,s,d,b : electrical); END ENTITY mosfet_simple_body;  ARCHITECTURE arch_mosfet_simple_body OF mosfet_simple_body IS constant eps0 : real := 8.855E-12; -- [F/m], dielectric constant constant Kox : real := 3.9; -- [F/m], relative permittivity of SiO2 constant Ks : real := 11.8; -- [F/m], relative permittivity of Si constant mun : real := 0.06; -- [m^2/(V*s)], mobility of electrons near the silicon surface constant ni : real := 1.5E16; -- [carriers/m3] constant kB : real := 1.38E-23; -- [JK-1], Boltzmann's constant constant q : real := 1.602E-19; -- [C], electron charge constant VT : real := kB*T/q; -- [V], thermal voltage  quantity Vds across ids through d to s; quantity Vgs across g to s; quantity Vbs across b to s;         </pre>	<pre> function phi0(VT,NA,ND,ni:real) return real is begin return VT*log(NA*ND/(ni*ni)); end;  function kds(Ks,eps0,q,NA:real) return real is begin return sqrt(2.0*Ks*eps0/(q*NA)); end;  function clm(kds,Vds,Vgs,Vtn,L,Vdg,phi0:real) return real is begin return 1.0 + kds*(Vds- Vgs+Vtn)/(2*L*sqrt(Vdg+Vtn+phi0)); end;  function gamma(q,NA,Ks,eps0,Cox:real) return real is begin return sqrt(2.0*q*NA*Ks*eps0)/Cox; end; function vtnbody(vtn0,vsb,phi0,gamma:real) return real is begin return vtn0 + gamma * ( sqrt(vsb+abs(2*phi0))-sqrt(abs(2*phi0)) ); end;  function current(Ks,eps0,q,NA,ND,ni,VT,mun,Cox,Vgs,Vds,Vbs,Vtn ,W,L:real) return real is variable kds_v : real := kds(Ks,eps0,q,NA); variable phi0_v : real := phi0(VT,NA,ND,ni); variable vtnbody_v : real := vtnbody(Vtn,- Vbs,phi0_v,gamma(q,NA,Ks,eps0,Cox)); begin if (Vgs-vtnbody_v &lt; 0.0) then return mun*Cox*(W/L)*exp((Vgs-vtnbody_v)/VT); else if (Vgs-vtnbody_v &gt; Vds)then return mun*Cox*(W/L)*((Vgs-vtnbody_v)*Vds - 0.5*Vds*Vds ); else return 0.5*mun*Cox*(W/L)*(Vgs-vtnbody_v)*(Vgs- vtnbody_v)*clm(kds_v,Vds,Vgs,vtnbody_v,L,Vds- Vgs,phi0_v); end if; end if; end; BEGIN ids == current(Ks,eps0,q,NA,ND,ni,VT,mun,(Kox*eps0/tox),Vgs,V ds,Vbs,Vtn,W,L); END ARCHITECTURE arch_mosfet_simple_body;         </pre>
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**Table 1.** VHDL-AMS entity and architecture for the ideal nmos incorporating body effect and channel length modulation parameter.

## II. Analysis of Gate Length Variability

The coding is performed within ANSYS's SIMPLORER software environment [3]. Figure 4a shows the ideal nmos VHDL-AMS model connected in a circuit for testing. The gate voltage is provided by a constant source. The drain-source voltage is provided by a pulse function. Figure 4b shows the transient analysis of the  $I_{DS}$ - $V_{DS}$  curve of the ideal nmos simulated. Accordingly, Fig. 4c shows the connection of the ideal pmos model and Fig. 4d the corresponding  $I_{SD}$ - $V_{SD}$  characteristic.



**Figure 4.** (a) nmos function test circuit. (b) I-V relationship for nmos. (c) pmos function test circuit. (d). I-V relationship for pmos.

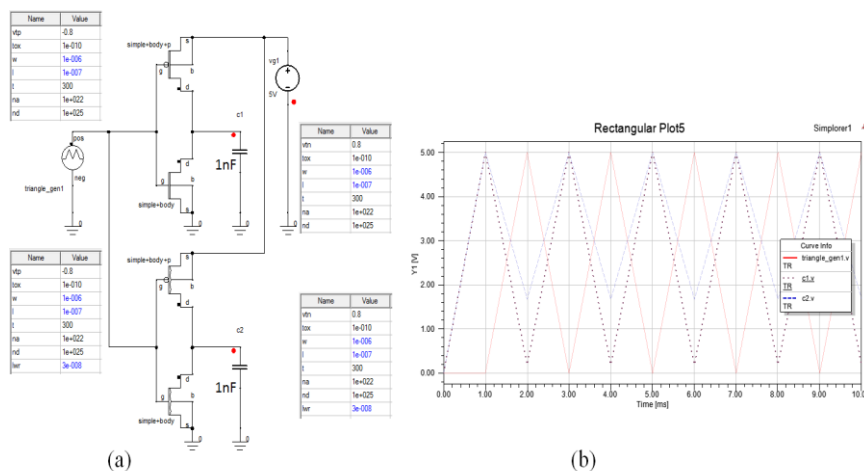
Gate length distribution due to process variations is given by a Gaussian distribution:

$$f(L, L_0, \sigma) = \frac{1}{\sqrt{2\pi}\sigma} \exp\left[-\frac{(L - L_0)^2}{2\sigma^2}\right] \quad (1)$$

where  $L_0$  is the nominal gate length, and  $\sigma$  is LWR value. In the drain current equation is all regions of MOSFET operation, the fraction  $W/L$  is always present as a multiplication factor. It is through this term, that LER affects drain current. In the presence of LER, this fraction is transformed into the following sum:

$$R_F = \sum_{i=1}^N \frac{W_i}{L_i} = \frac{L_0}{W} \sum_{i=-3\sigma}^{3\sigma} \frac{Wf(L_0 + i, L_0, \sigma)}{L_0 + i} \quad (2)$$

and is termed roughness-factor in this work. It is used to express the LWR effect on drain current equation, through a single multiplicative factor, in the architecture of the macromodel. Figure 5 shows a comparison of inverter timing analysis in the case of a gate without LWR and  $L=100\text{nm}$  and one with  $LWR=30\text{nm}$ . Using this models in other digital gates one is able to quantify the effects of LWR in overall circuit performances.



**Figure 5.** (a) Test circuit of an inverter gate using ideal nmos, pmos (above) and non-idea (below). (b). Transient analysis results of input signal and capacitor c1, c2 voltages.

### III. Set Modeling

Along the same line of work a simple SET macromodel is also developed. Example of the VHDL-AMS code is shown in Fig. 6. By biasing the device as shown in Fig. 7a, it is possible to replicate the IV characteristic of Fig. 7b, showing the Coulomb blockade region which is the characteristic trademark of single-electron device operation. More complex model of digital gates could be designed along this line of work showing the applicability and limitations of single-electron devices as functional elements in state-of-the-art circuits.

<pre> ----- VHDLAMS MODEL single_electron_transistor ----- ENTITY DECLARATION single_electron_transistor LIBRARY Ieee; use Ieee.electrical_systems.ALL; use Ieee.math_real.ALL; ENTITY single_electron_transistor IS PORT ( TERMINAL G : electrical; TERMINAL S : electrical; TERMINAL D : electrical; END ENTITY single_electron_transistor;         </pre>	<pre> ----- ARCHITECTURE DECLARATION arch_single_electron_transistor ----- ARCHITECTURE arch_single_electron_transistor OF single_electron_transistor IS CONSTANT vth : real := 0.02; CONSTANT pii : real := 3.14159265358979; CONSTANT cf1 : real := 40.0; CONSTANT cl2 : real := 2.0e-010; CONSTANT cr1 : real := 300000000.0; CONSTANT cr2 : real := 100000000.0; CONSTANT vp : real := 0.02; QUANTITY R1 : resistance; QUANTITY R2 : resistance; QUANTITY R3 : resistance; QUANTITY i through d TO s; QUANTITY v across d TO s; QUANTITY vds across g TO electrical_ref; BEGIN R1 == cr 1+cr2 *cos(cf1*pi*vds); R2 == cvp/(cl2-2.0*vp/(cr1+cr2*cos(cf1 *pi*vds))); R3 == cvp/(cl2-2.0*vp/(cr1+cr2*cos(cf1 *pi*vds))); IF v'above (vth) USE i == (v*(R1+R2)-vp*R1)/(R1 *R2) ; ELSEIF v &lt; -vth USE i == (v*(R1+R3)+vp*R1)/(R1 *R3); ELSE v=i*R1; END USE; END ARCHITECTURE arch_single_electron_transistor; ----- END VHDLAMS MODEL single_electron_transistor -----         </pre>
(a)	(b)

Figure 6. VHDL-AMS code for single-electron transistor model. (a) Entity. (b) Architecture. Coding is realized within ANSYS’s SIMPLORER software platform.

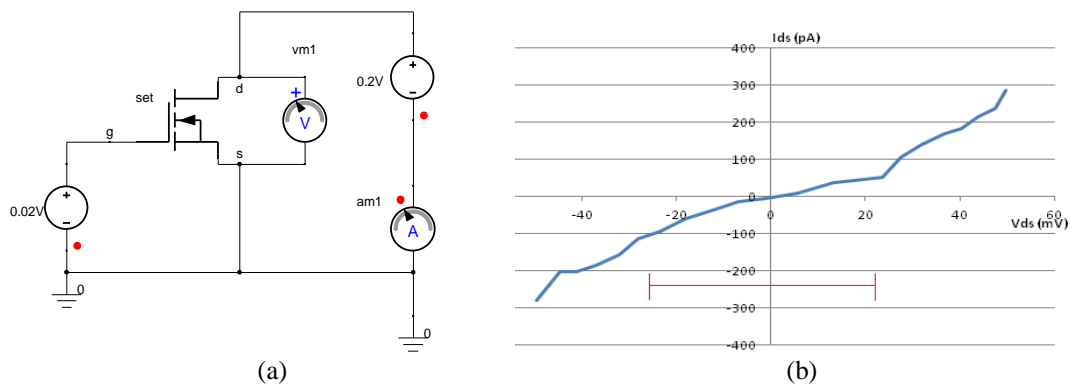


Figure 7. (a). Biasing circuit for single-electron transistor. (b). Corresponding IV curve. The bar marks the Coulomb blockade region.

### IV. Conclusion

VHDL-AMS offers the ability to incorporate changes in standard semiconductor device models and be able to quickly validate them in simulations. Along this line, the effects of line-width roughness were incorporated on a simple model for nmos and pmos transistor and its effects were observed on the behaviour of more complex device model. Also a first version of a single electron transistor is developed as a basic unit for more complex circuits and systems. Such macromodeling procedure can be extended for the quantification of many vital physical phenomena of circuit operation.

### References

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- [2]. G. P. Patsis, Modelling MOSFET gate length variability for future technology node, Phys. Stat. Sol. (a) 205 (11), 2008, 2541-2543. Ansys site: <http://www.ansys.com/>