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Study of an n-MOSFET by Designing at 100 nm and Simulating using SILVACO ATLAS Simulator

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Abstract:
In this paper, the design steps of an n-MOSFET have been described and then the electrical characterization of this MOSFET is simulated at 100 nm by using the SILVACO ATLAS software, which is a process and device simulation software tool. The MOS device is virtually fabricated using ATHENA in SILVACO and simulations have been performed with help of ATLAS software, and all graphs are plotted using TONYPLOT in the SILVACO. The simulated results are then analyzed to study the n-MOSFET device's mesh structure, transfer and output characteristics of the same, doping and carrier concentration plot, etc. From the simulation study, we found that the designed device is working well for various bias conditions.
Key Words*: MOSFET; SILVACO; Device Design; ATLAS; Device Simulation.*

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I. Introduction

A digital electronic circuit is one of the principal functioning components of any digital system, for example, a microprocessor circuit, or a mobile device [1]. These digital circuits are primarily composed of transistors, such as MOS transistors. This is the elementary constructional unit of any digital circuits or systems [2]. In the VLSI circuit design, therefore, it is an important task to study the behavior of MOS transistors correctly because the performance of any digital circuits or systems depends highly on the proper selection and design of these transistors. A large number of arithmetic and logical operations is being performed by the various types of VLSI circuits, like a digital signal processor, microcontrollers, and microprocessors when these are being applied in real-time systems [3-5]. Therefore, before going into the manufacturing stage of any structure of a MOS transistor commercially, it is imperative to get the actual characteristics and to analyze the performances of that device using any Technology Computer-Aided Design (TCAD) software tools that may provide effective results by simulating the device structure under various steady-state and transient conditions. SILVACO ATLAS is such a commercial process and device TCAD simulator software through which we can analyze the electrical characteristics and electro-thermal parameters, like output current, built-in potential, electric field, gate leakage current, localized heating, lattice temperature rise, etc. [6]. Variation of such parameters widely may lead to the device's structural failure. In this paper, we will provide a detailed description of the design steps of an n-MOSFET structure using SILVACO ATLAS commercial TCAD software and will apply it to plot various device characteristics at different bias conditions to verify the functionality of the device. Our analysis demonstrates the designed MOS device worked very well.

Technology Computer-Aided Design (TCAD) design and simulation tool is a virtual platform to design, fabricate, and then operate the semiconductor devices, such as Bipolar Junction Transistor (BJT), Metal Oxide Semiconductor Field Effect Transistor (MOSFET), etc. by running the simulation of this software. This is essential to understand and test the functionality of the designed device structure to investigate the complete device performances before going for the real-time fabrication process. This also helps to extract the device parameters by studying the simulated characteristics of the device. Besides, this can save the overall time and cost compared to the real-time fabrication procedure.

DeckBuild is the front-end Graphical User Interface (GUI) of SILVACO's virtual platform-based wafer fabrication program. The framework of this program links a wide range of process and device simulation tools that are available under SILVACO and lets them work in an organized fashion without a glitch and efficiently. DeckBuild's pull-down menus help to make syntax and offer basic simulation controls. ATLAS is a multi-dimensional device simulation framework. Therefore, n-MOSFET can be generated in the ATLAS simulation environment using its layout-based simulation syntax; though we are focusing on the design, simulation, and characterization of the MOS device before starting the real-time fabrication in the industry.

The paper provides a detail literature review in section II, then an overview of the MOS device design steps in SILVACO ATLAS in section III, and after that, it presents all the results and their explanations in section IV. Finally, the paper ends with the concluding remarks in section V.

II. Literature Review

Silicon technologies are being progressed faster every year due to the incessant scaling down of the sizes of semiconductor devices due to the ever-increasing necessity of high performance (for example, faster-operating speed or higher operating frequency, etc.) devices based on the Field Effect Transistors (FETs) and other transistors. However, reducing the size of a transistor is not going to be an easy job because this has increased the circuit complexity and has created many serious problems especially when the dimension goes down into the sub-100 nm regime. One of the challenges with the downsizing of the transistor is the short channel effects (SCEs). However, to overcome these problems, new circuit design techniques are being introduced for the newer technologies and novel architectures are also coming out. For example, to combat short channel effects, non-traditional FETs were introduced at the nanometer level [7]. Therefore, before the mass scale fabrication, the device designed in the nano-scale regime must be simulated using any software, such as MEDICI, SILVACO, MINIMOS, COMSOL Multiphysics, LT-SPICE, MATLAB, etc. used for the novel semiconductor device design, its process simulation, and characterization.

Short Channel Effect (SCE) suppression of the pocket implanted n-MOSFET was been investigated using MEDICI, a powerful device simulation software earlier [8]. In this device, lateral channel engineering is done to combat SCE.

A novel integrated Metal Oxide Semiconductor Field Effect Transistor (MOSFET)-based microelectromechanical systems (MEMS) mechanical pressure sensor circuit has been designed using the finite-element method (FEM) computations via the COMSOL Multiphysics software. Besides, the circuits have been analyzed for varying circuit and Complementary Metal Oxide Semiconductor (CMOS) parameters, viz. the supply voltage (V_{DD}) and threshold voltage (V_t), respectively using the COMSOL Multiphysics software tool. The sensor circuit is simulated electrically in the LT-SPICE tool via a MATLAB script. MOSFET parameters have been extracted using the FEM [9].

At present, the CMOS and MEMS technologies are being widely materialized for different microsensors for healthcare and biomedical-related integrated on-chip electronic circuits [10]. For example, Blood Pressure (BP) is one of the most important factors to specify the human health status [11]. In such applications, the pressure sensor is the key to measuring intra-arterial blood pressure directly [12], [13]. There are various types of pressure sensing methods, such as piezoresistive, piezoelectric, and capacitive techniques. Of them, the piezoresistive effect in MOSFET [14], [15] is one of the most promising and developing sensing tools for smart sensors. In this context, a paper reported on the design and optimization of a current mirror sensing-based MOSFET at 5 μm CMOS technology. Here also FEM-based COMSOL Multiphysics is used to simulate the pressure sensor and then to estimate the characteristics of the pressure sensing circuits for the current mirror, T-Spice has been engaged [16].

Currently, Transition Metal Dichalcogenides (TMDs) group materials are being utilized to develop electronic devices as a new trend. For example, Molybdenum Disulphide (MoS_2) has been employed to design profoundly scaled Field Effect Transistors (FETs). As such, in an article, the authors did a simulation of a full-wave model of a device using this material in COMSOL Multiphysics for 2 dissimilar thicknesses [17].

In another work, the authors presented a novel simulation atmosphere to analyze the electro-thermal interaction in power semiconductor devices. This is based on the combined use of ELDO-COMSOL simulators in an iterative pattern along with an electrical 2-D SPICE network and 3-D FEM thermal solver [18].

The MINIMOS simulator has been used to investigate the parasitic effects at the channel edge on MOS device characteristics by another group of researchers. They used an automatic grid-refinement algorithm to create the particular grid [19].

The evolution of CMOS technology is directed largely through a down-scaling of the device sizes over the last few decades. One of the strategic questions regarding future VLSI/ULSI technology is whether it is possible to scale down the CMOS device sizes beyond 100 nm channel length to get continuous improvement in terms of the packing density and operating speed improvement. In a paper, the design, fabrication, and characterization of high-performance and low-power MOS devices were explained at the 90 nm node. Virtual Wafer Fabrication (VWF) SILVACO TCAD tool was used to fabricate and simulate the CMOS transistor, for example, ATHENA and ATLAS [20].

In another work, the researchers studied the process variation effects on the threshold voltage of a floating gate device through the simulations at CMOS 180 nm process using the TCAD tools ATHENA, DevEdit3D, and ATLAS [21].

MATLAB programming has also been used for the analytical model verification of threshold voltage and surface potential models of the pocket-implanted n-MOS device in the nanoscale regime [22], [23].

A paper described an analytical drain current flicker noise model for pocket implanted n-MOSFET in the nanoscale regime based on the two linear pocket profiles from the source and drain ends, and the analytical flicker noise model was simulated for various device and bias parameters using MATLAB software tool [24].

Vertical III-V nanowire MOSFETs were designed by COMSOL Multiphysics to minimize the parasitic capacitances of the scaled devices, such as gate-drain capacitance to 17 aF/wire, corresponding to 0.2 fF/μm at 20 nm gate length of the device [25].

In another work, the researchers designed a triangular-shaped silicon nanowire (Si NW) FET of 300 nm channel length based on the Finite Element Method (FEM) tool, COMSOL Multiphysics software, and then its Short Channel Effect (SCE) parameters were extracted [26].

In the literature survey, it was also found that the electrical characterization of a 65 nm NMOS transistor was simulated by using the ATLAS simulator, and then their results were compared with the experimental results found in the literature. The input and output characteristics of the NMOS transistor structure were studied also using the same simulator [27].

Another paper explained the characteristics of 65 nm PMOS technology with strained Si in terms of electrical parameters like drain current, gate voltage, etc. employing the ATHENA fabrication simulator to fabricate while ATLAS simulator to characterize the device electrically [28].

A Ternary Logic Decoder (TLD) has been revealed with double-gate silicon-nanowire (DG Si-NW) MOSFETs to check the viability of a mixed-radix system. At first, the DG Si-NW MOSFETs were fabricated and characterized and then the electrical characteristics were modeled, fitted, and analyzed semi-empirically in the SILVACO ATLAS TCAD simulator [29].

In another work, the authors have downscaled a planar PMOS device to 14-nm of channel length using La_2O_3 as the high-k gate dielectric material. The device was fabricated and electrically characterized virtually via the TCAD simulation tool, SILVACO. The study of the variation of the process parameters and interaction effects delivered the optimized values of the process parameters to attain the desired output. The results found through the SILVACO simulations were in good agreement with the nominal values of the PMOS device as anticipated by the International Technology Roadmap for Semiconductors (ITRS) [30].

In another paper, the authors presented their SILVACO simulation results for a 3-D Silicon On Insulator (SOI) n-FinFET device at 8 nm channel length. The impacts of the changes of the key electrical parameters, such as threshold voltage, subthreshold slope, transconductance, drain induced barrier lowering, on current, leakage current, and on/off current ratio were obtained and then analyzed [31].

III. Device Design and Simulation Method

The schematic device structure of a bulk n-MOSFET is depicted in Fig. 1. The structure uses a p-type Si as the substrate material with a uniform doping concentration of 10^{17} cm^{-3}. The source and drain regions are heavily doped n^+-type with a uniform doping concentration of 10^{20} cm^{-3}. The insulating layer in the gate region is a SiO_2 layer with a gate length of 100 nm and an oxide thickness of 3 nm.

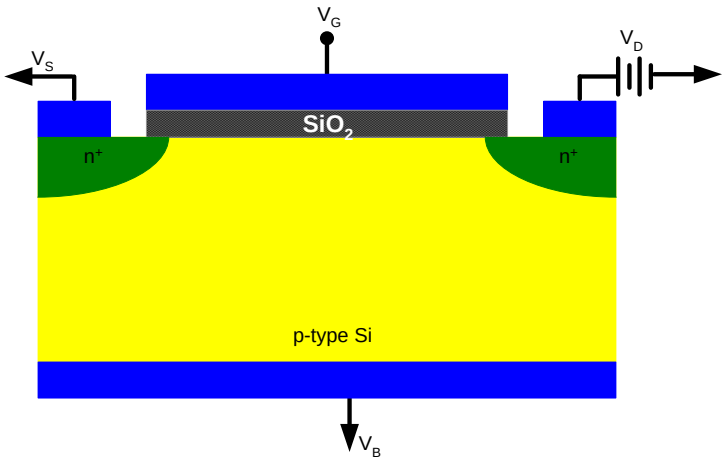

Figure 1. The schematic device structure of a bulk n-MOSFET

The mesh structure of this n-MOSFET structure has been defined using SILVACO's ATHENA and then re-meshing is done using DevEdit. Input and output characteristics have been obtained using ATLAS software. To write a program file, at first, we need to define the process flow for the MOS transistor structure in ATHENA. The defined mesh sometimes may not be optimum for the process and device simulations. In such cases, the mesh needs to be re-created by the mesh generation tool, DevEdit. This might happen if the mesh of

the semiconductor region possesses zero obtuse triangles. Then the refinement is performed as a function of several solution quantities inside the mesh (for example, the net doping concentration). To create a set of commands in the DeckBuild command window, DevEdit's Popup Windows may be used. However, the DevEdit GUI may be used by opening the structure file from ATHENA, re-meshing it using DevEdit GUI, and saving a DevEdit command file from where the mesh syntax may be copied and pasted into DeckBuild [32].

In ATLAS, the transfer characteristic was generated by fixing the drain-to-source voltage at a fixed value, e.g., 0.5 V, 1.5 V, and 2.0 V, and then ramping the gate voltage from 0 V to 4 V with the step of 0.1V using a sequence of SOLVE statements of the program. The threshold voltage is adjusted using the work function parameter from the gate contact statement to 4.6 V. The output characteristic is obtained by setting the gate voltage above the threshold value, e.g., 0.75 V, 1 V, 1.5 V, etc. and then ramping up the drain-to-source voltage from 0 V to 1.1 V using a sequence of SOLVE statements with the step of 0.1V. All terminal characteristics are saved to a log file as specified in the LOG statement. Using the log-off statement, one can save several log files for later use. The results are saved to a solution file. The extract statements are used to measure the threshold voltage and other SPICE parameters of the designed device. Finally, the three curves for each characteristic are overlaid using the TonyPlot [32].

To include the drain and source contact resistances in the characteristic curve, a drain contact resistance is added using the statement contact name, drain. To perform the ac analysis, the AC parameter must be turned on above the solve statement. To load and run the file, we need to select the load button in DeckBuild. This copies the input file and any other support files to the currently active folder and then we need to select the Run button in DeckBuild to execute the file. The designed mesh structure is shown in Fig. 2.

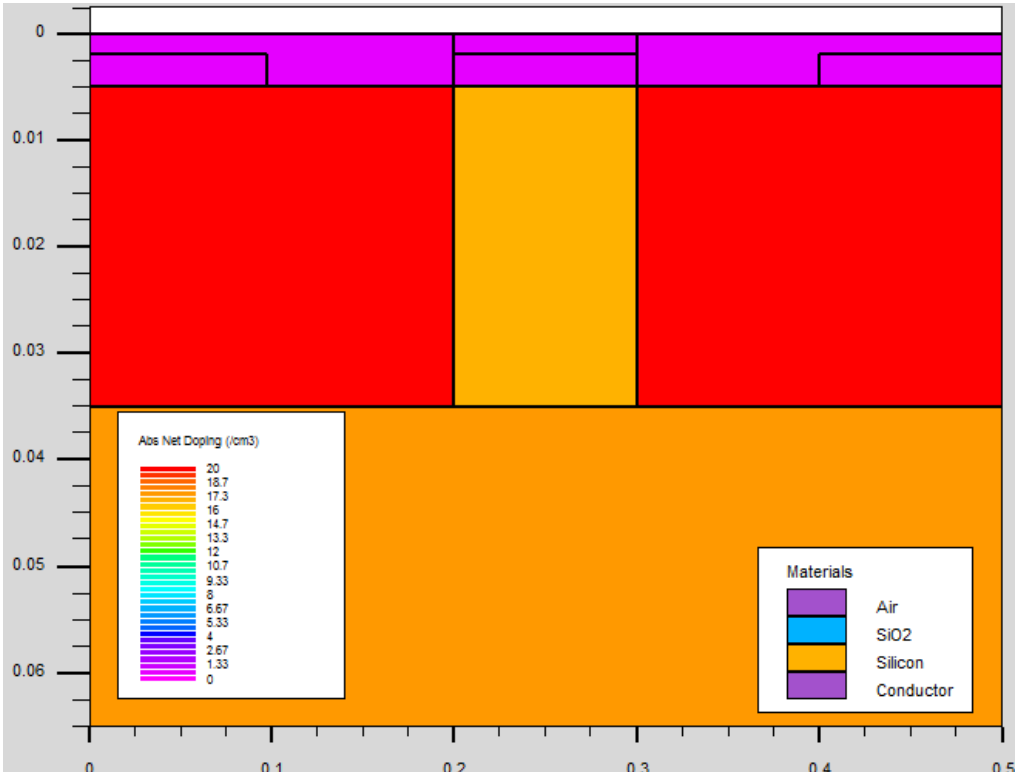

Figure 2. The mesh structure of the n-MOSFET; the values of *x*- and *y*-axis are given in micrometers

Figure 2 shows the absolute doping structure of various regions on the left side and the materials of various regions on the right side. Various colors are used to define various regions, for example, red color is used for source and drain regions, the yellow color is for channel and substrate regions, and the violet color is for metal contacts.

IV. Simulation Results and Discussions

Figure 3 shows the doping concentration profile along the channel. It shows the source and drain regions have the same amount of uniform doping density of 10^{20} cm^{-3} and the substrate or the region just beneath the gate oxide has the uniform doping concentration equal to 10^{17} cm^{-3}.

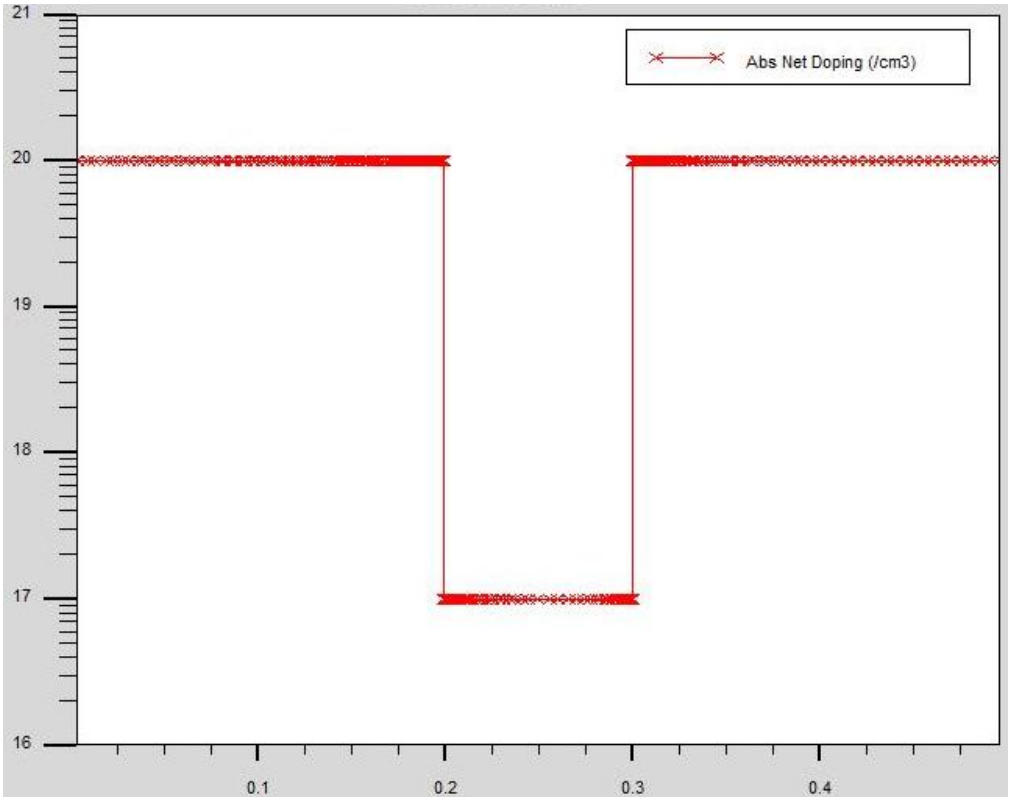

Figure 3. Absolute doping concentration along the channel direction from the source to the drain sides

Figure 4 shows the energy diagram of the conduction and valence bands along the horizontal distance. As we go along the line, we see that the conduction band energy level decreases from almost 0 eV to -1 eV, and the valence band energy level decreases from almost -1 eV to -2 eV.

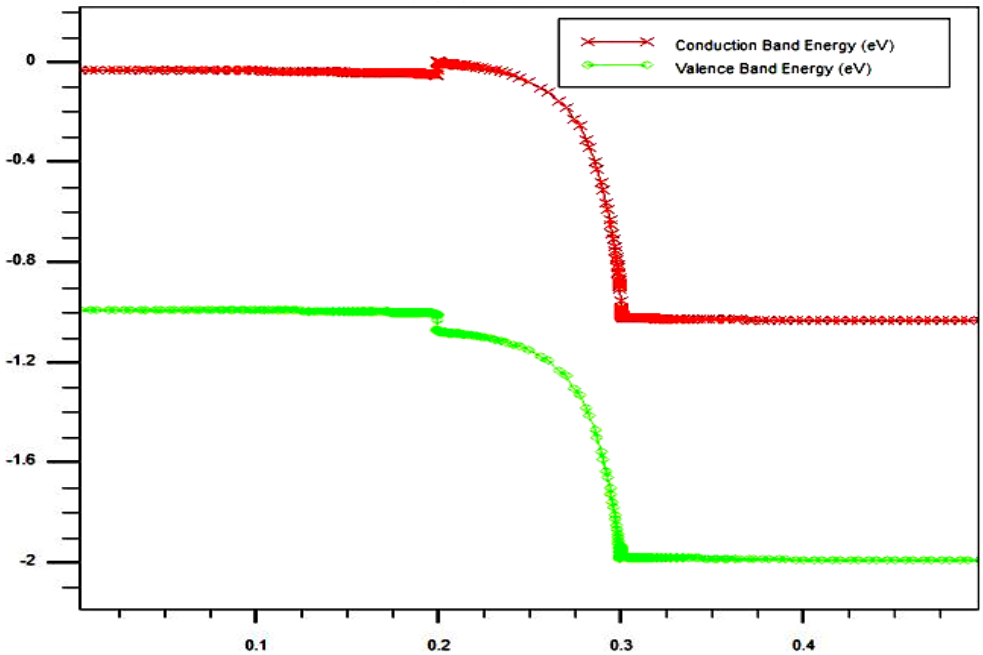

Figure 4. Energy Diagram of the Conduction and Valence Bands

Figure 5 shows the electron and hole mobility profiles along the channel. Electron mobility is higher in all regions than that of the hole because of the higher values of the effective mass of the latter. This matches with the theoretical prediction of carrier mobilities of semiconductor devices [11].

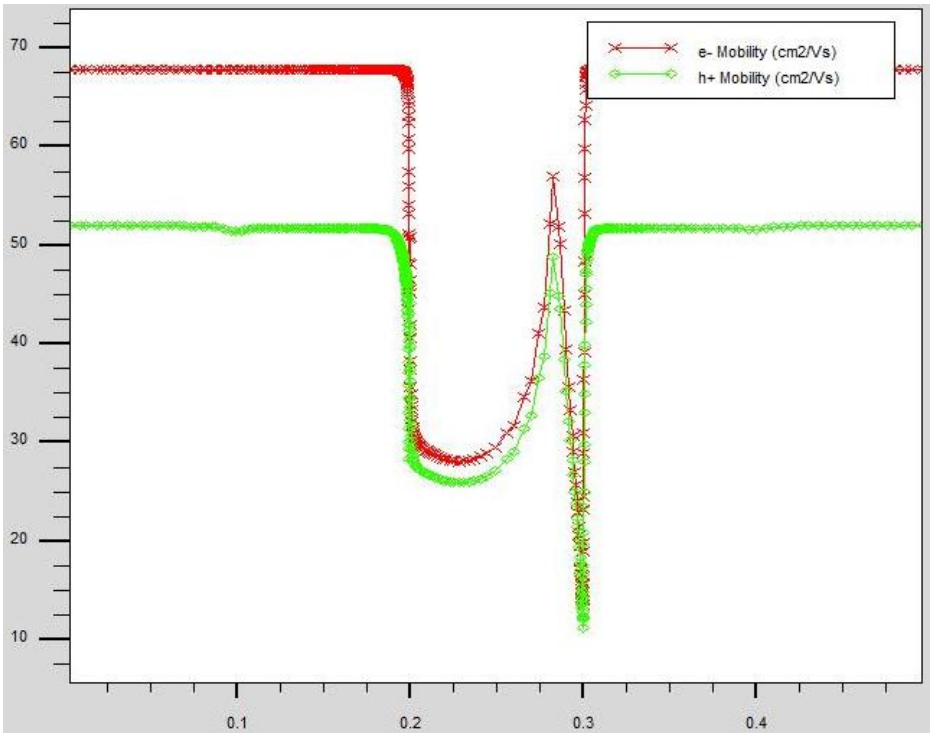

Figure 5. Electron and hole mobility profiles

Figure 6 shows the electron concentration profile along the channel. In the channel, we see that the electron concentrations have been raised both at the source and drain sides. However, at the source side, the concentrations are higher than that of the drain side. The surface concentration in the channel is higher than the substrate doping concentration, i.e., $n_s > N_a$. It ensures that the channel has been inverted.

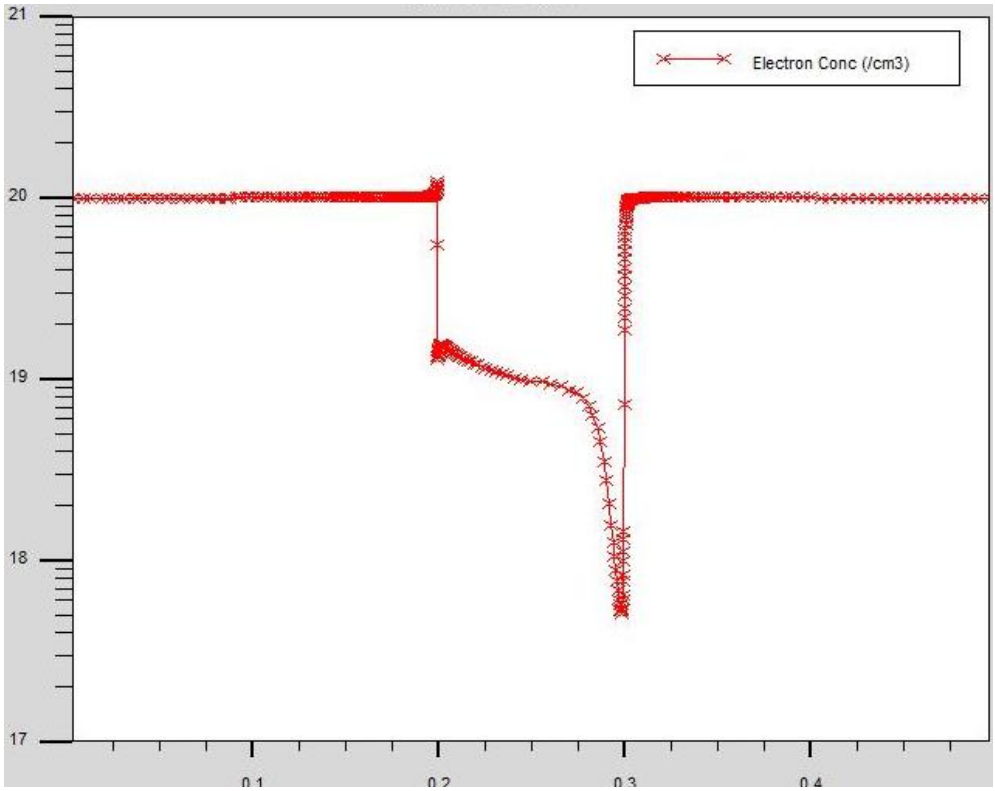

Figure 6. Electron concentration profile along the channel

Figure 7 illustrates the recombined electron concentration plot along the channel. We observe that most of the electron recombination occurs at the source side and there is almost no recombination at the drain side. However, under the middle of the gate oxide almost no recombination has been observed.

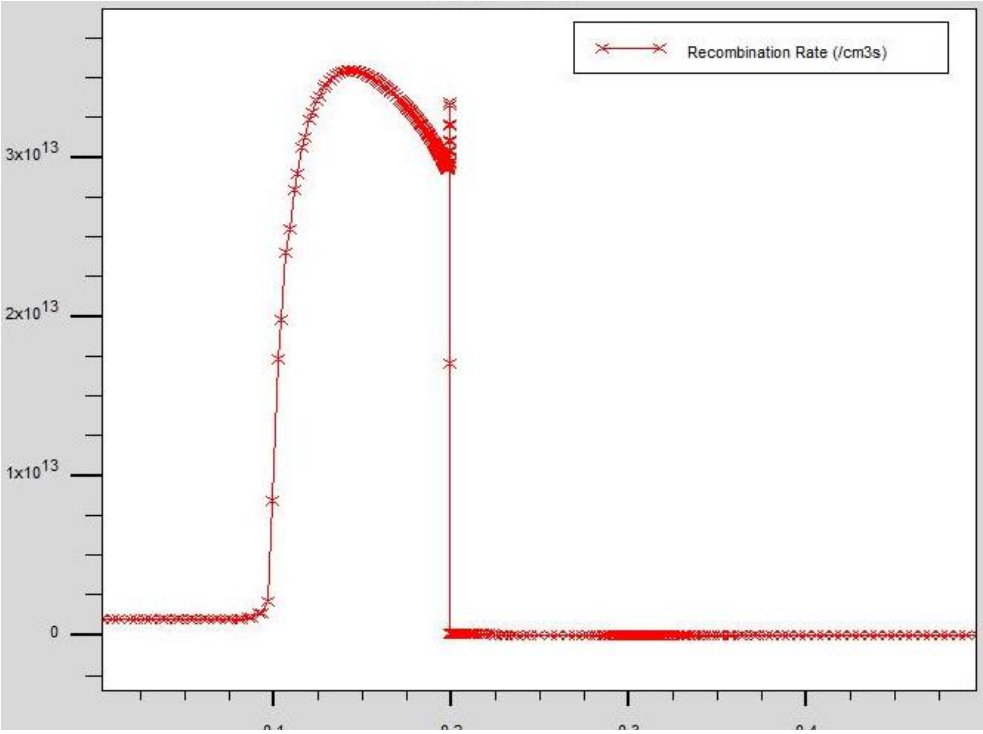

Figure 7. Recombined electron concentration profile along the channel

Figure 8 illustrates the transfer characteristics comprising drain-to-source current vs. gate-to-source voltage for several drain-to-source fixed bias voltages of 0.5 V, 1.5 V, and 2.0 V. We observe that below the threshold voltage, there is no drain-to-source current but above the threshold voltage, the drain current rises exponentially with the gate voltage. Also, if the drain-to-source bias voltage is raised from 0.5 V to 2.0 V then the drain-to-source current also rises for a certain gate-to-source voltage.

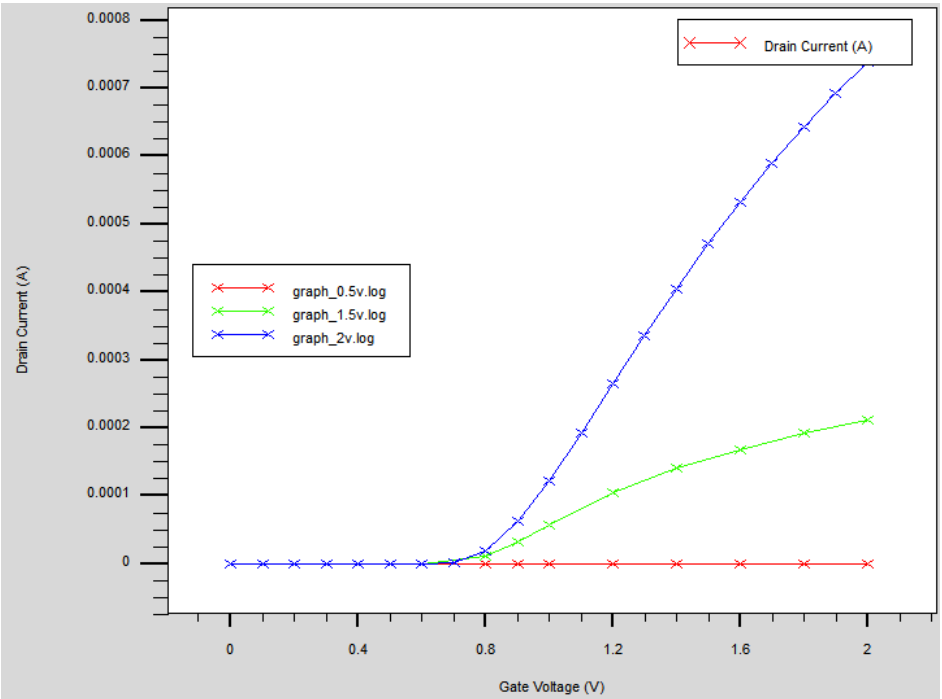

Figure 8. Transfer characteristics (drain current vs. gate voltage) for several drain voltages of 0.5, 1.5, and 2 V

Figure 9 shows the output characteristics (drain-to-source current vs. drain-to-source voltage) for several gate-to-source voltages of 0.75 V, 1 V, and 1.5 V. We observe that below the pinch-off voltage, the drain-to-source current rises almost linearly with the drain-to-source voltage above the threshold voltage, but the drain-to-source current becomes saturated with the rise of the drain-to-source voltage above the pinch-off voltage. Also, if the drain-to-source voltage is raised from 0 V to 1.1 V then the drain-to-source current also rises for a specific drain-to-source voltage below and above the pinch-off voltage.

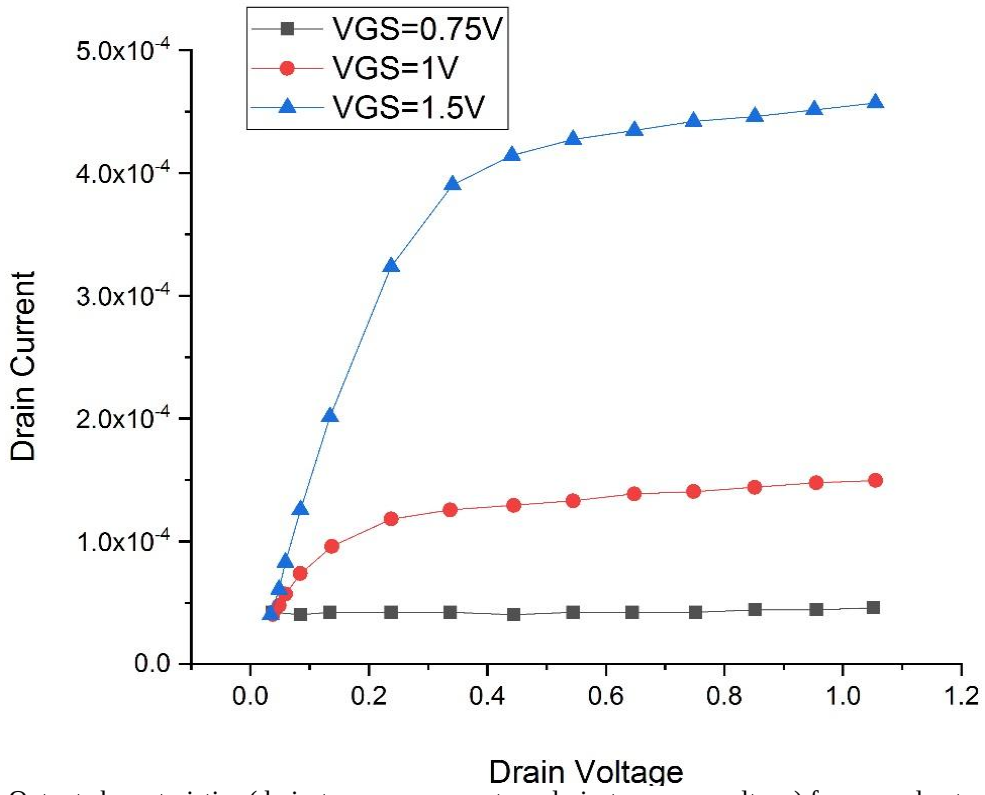

Figure 9. Output characteristics (drain-to-source current vs. drain-to-source voltage) for several gate-to-source voltages of 0.75, 1, and 1.5 V

V. Conclusion

We designed a general bulk n-MOSFET and analyzed the electrical characteristics of it using SILVACO ATLAS Simulator. The characteristics are very much similar to that of an n-MOSFET that are found in the literature. Recently, more novel MOS structures are evolving, like Double Gate (DG) MOSFET, Double Gate Double Metal Contact (DGDM) MOSFET, Double Gate Tripple Metal Contact (DGTM) MOSFET, SOI MOSFET, Gate All Around (GAA) FET, etc. and those are found promising in VLSI and ULSI circuit design. These novel MOS structures are highly reliable, low-cost, low- and ultra-low-power consumption and dissipation as well. Therefore, the study of such structures through design and simulation using the SILVACO software at nano-scaled regime would be very useful in the electronics industry to check whether all the requirements are fulfilled or not for the sustainable design of ICs before going into its successful hardware implementation in the mass scale.

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