IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)
Volume 12, Issue 4 (Jul. - Aug. 2022), pp.08-17
e-ISSN: 2319-4200, p-ISSN: 2319-4197
www.iosrjournals.org

Ultra High multi channel clock frequency(THz, PHz, EHz, ZHz,YHz,XHz,WHz) baud rate speed PRBS Transceiver HDL RTL ASIC Design for Ultra High long Distance Wireless Communication Engineering Smart Computing Products/ Applications

Prof. Executive Dean. P.N.V.M Sastry[1], Prof. Dean. Dr.S.Vathsal[2]
[1](VLSI Design Dept.,, Silicon Interfaces Pvt., ltd, India)
(Former Principal Engineer- VLSI DV-FPT Software India Pvt., ltd.,& Cornami Inc., USA),Staff Engineer Mirafra software Technologies, Sr. Manager Tessolve Semiconductor and Global contingent Manager-Intel DV, Contract/tmp, Synopsys Inc.,Verification Group, USA)
[2](Prof. **EEE,** Institute of Aeronautical Engineering, India (Former Prof and Dean, JBIET, Retd.Director Incharge DRDO, Scientific Officer F DRDO Hyderabad, Scietific Officer E Vikram Sarabhai space center ISRO,Post Doctoral Research Fellow NASA Flight Center,USA)

Abstract: *The Key Objective is HDL RTL Design Architecture of Ultra high multi Clock Frequency Speed Rate (MHz, GHz, THz, PHz, EHz, ZHz, etc) Bits Per Second Baud Rate) P.R.B.S(Pseudo Random Binary Sequence) Transceiver Soft A.S.I.C IP Core product for identification of the property of Different Pseudo Random Binary Sequence Patterns (Seed Words) of $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 tapped elements as per C.C.I.T.T-I.T.U Standards and IEEE-754 Single and Double Data Rate Data Precision Standards (32 bit & 64 Bit Data Width) suited for Very Advanced Futuristic Hi-tech Smart High Speed Long Distance Wireless Digital Communication A.S.I.C Products / Applications like Space/Satellite, Aerospace and Large Data Processing and computing like High Speed Internet and Cloud Computing based Hi-Fi Industrial Data Automation Standard Ultra High Speed Wireless Communication A.S.I.C products and Applications-3G,4G,5G etc. The Multi channel PRBS Transceiver consists Transmitter and receiver of different PRBS patterns- $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 NRZ. The data input transmitted and received serially in the form bit by bit. These different pattern sequences are Designated as per CCITT ITU 0.151/O.152/O.153 & AT&T Standards. The Aim and purpose of invention of Ultra high multichannel Clock frequency PRBS Transceiver is for transmit and receive data serially by using Tx_in and Tx_out, rxin, rxout signals and The Transceiver is processed the low frequency signal input with different high speed carrier wave frequencies in the form of different PRBS pseudo random binary sequence seed word bit/byte patterns -$2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 NRZ and also on receiver side processed with the above patterns.*

Materials and Methods: *Transmission and reception of Data serially based on the Deterministic random seed word pattern methods of different PRBS $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 tapped sequence Elements and All these PRBS are purely synchronized with Ultra high clock frequency(MHz, GHz, THz, PHz, EHz, ZHz, YHz, XHz, WHz). The Soft IP Core Designed by System Verilog HDL/ Verilog HDL. RTL Design Simulation done by Synopsys VCS 2020.1 software and Altera Model-Sim Software and Logic Design Flow & Synthesis done by Xilinx ISE and Altera Quartus EDA Tools.*

Results: *Generation of Simulation Display and waveform for Ultra High Clock frequency(MHz, GHz, THz, PHz, EHz, ZHz, YHz, XHz, WHz) Synchronized Pseudo Random Binary Sequence (PRBS) Register Transfer Level (RTL) Generators, Transceiver for efficient and effective High Quality Data transmission and Reception of Various tapped sequence patterns for Identification of property of different PRBS patterns$2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 NRZ of Ultra high speed Long distance wireless engineering Applications/ products.*

Keywords. *P.R.B.S- Pseudo Random Binary Sequence, RTL- Register Transfer Level, F.P.G.A – Field Programmable Gate Array, C.C.I.T.T- Consulting Committee for International Telegraph and Telephone, I.T.U- International Telecommunication Union, A.S.I.C- Application Specific Integrated Circuit, E.D.A- Electronic Design Automation, H.D.L- Hardware Description Language, IP- Intellectual Property.*

Date of Submission: 28-08-2022 Date of Acceptance: 30-09-2022

I. Introduction

In Modern Wireless Communication Engineering and Technology World , P.R.B.S Design have many advantages like Reduction of Random Noise, Improvement of Communication Performance and Speed. Speed is an major constraint factor Due to that I Designed P.R.B.S Receiver of Weka Bits Per Second Data rate Speed for Processing and controlling Large Wireless Data Packets and Frames for High Speed Transmission and Reception ,for that I used P.R.B.S Technique, In Modern Communication Technology world PRBS Plays vital role for high Speed Transmission and Reception. P.R.B.S – Pseudo Random Binary Sequence ,Pseudo means Deterministic, Random – Repeated , Binary Sequence – 0 and 1 sequence. The Length of P.R.B.S is 2^{m-}1,after 2^m-1 sequence repeated to starting sequence for Improvement of speed and performance large data frame sequences. This Receiver mainly for designed for High Speed Data Packets reception.

In Modern Hi-tech Wireless Communication Systems, High Speed Data Communication is very Important for future generated wireless data communication applications and products like internet and cloud computing, Data Speed is in terms number of bits transmitted and received per second , due to this , I Designed Ultra high multichannel Clock Frequency Speed - P.R.B.S Transceiver Designed for Very Futuristic Advanced L.T.E A.S.I.C Wireless Communication products Space/Satellite, Aerospace, high Speed Internet and Large Data based Cloud Computing Products and also for Advanced Long Distance Wireless Communication Protocols. Due to this I Designed for Ultra high multichannel Clock Frequency Rate PRBS Receiver for Identification of Different PRBS Patten Code sequences of Different Tapped lengths - 7,10,15,23,28,31,48,52,63 according to IEEE single and double precision & ITU CCITT Standards.

Transmission, Reception of Data is in the RANDOM Sense, This PRBS Generator, Receiver is Designed for Identification property of Different Tapped PRBS Sequences like 10 e power 7, 10 e power 10, 15 , 23 , 31,48,52,63 at a Weka Hertz Clock frequency and the Carrier speed is in terms of Mega, Giga, Tera, Peta, Exa, Zetta, Yotta, Xona, Weka bits per Second baud rate and also multi clock frequency generator provides high speed data rate frequencies like Giga/Tera/Peta/Zetta/Yotta/Xona/Weka Bits Per Second ,like G.b.p.s/T.b.p.s/P.b.p.s/E.b.p.s/ Z.b.p.s / X.b.p.s / Y.b.p.s/W.b.p.s. The Length of PRBS sequence is 2^L-1. 2^L-1 times repeated the sequences. this is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like Satellite GPS Data Acquisition, GSM Communication Systems, Wi-Fi, LTE Computing, wireless internet computing, cloud computing etc because of Ultra High speed Communication Rates in terms G.b.p.s(Giga Bits per Second),T.b.p.s(Tera Bits Per Second), P.b.p.s(Peta Bits Per Second), E.b.p.s-Exa Bits Per Second, Z.b.p.s-Zetta Bits Per Second, Y.b.p.s- Yotta bits Per Second, X.b.p.s- Xona Bits Per Second, W.b.p.s- Weka bits Per Second, All these PRBS LFSR Sequences are designed by tapping different points according to ITU O.150, O.151, and O.152 Standards. This PRBS Receiver Design Consists of Multiplexer, PRBS Registers of different tapped sequence points, Clock Frequency Generators of G.b.p.s/T.b.p.s/P.b.p.s/E.b.p.s/Z.b.p.s/X.b.p.s/Y.b.p.s/W.b.p.s Speed Rate. The Advantages of these PRBS Generators having In Built Checkers, Bit Error Rate Detection & Correction by using PRBS Checkers. these are simply Linear Polynomial Checkers & CRC. Improvement of Speed and Performance and Reliable Communication and Reduction of Chip Complexity, Power Consumption, NOISE. Reduction Data Traffic and Loss. The Applications are Wireless and Telecommunication, Image & Video Processing, Data Encryption and Decryption, Cryptographic, Portable Multimedia and wireless consumer electronics products, the advantages are high speed data computing Tx/Rx.

This new innovative Ultra high multi clock frequency P.R.B.S Transceiver A.S.I.C I.P Core is having many advantages compared to current generation of P.R.B.R Transceiver , These are the improvement

of the reliability , Automatic In Built Testing and Error rate Analysis of large/big data frames , easily Recognize/ identified the P.R.B.S Pattern Sequences as per I.T.U Standards and I.E.E.E , reduction of number of gate components in the A.S.I.P S.O. C IP Core, receives the large number of multiple data frames with more accuracy for large data computing applications like wireless internet and cloud computing applications. Speed of the data is very very far away compared to current generation ASIC products available in the market, because of by synchronizing with Mega, Giga, Tera, Peta, Exa, Zetta, Yotta, Xona,Weka Hertz Clock Frequency. Compatibility and flexibility, data accuracy more compared to current existing products, also this product is very suit to interface with High Speed Serial communication protocols to test and analyze the data frames at weka Hertz clock Frequency for improvement of high speed in serial communication. Very less time takes to decrypt the PRBS Data Pattern Sequences and Frames of different pattern sequences. Very flexible clock and data recovery and synchronization and time delay. Chip Complexity is drastically reduced in this product, just in terms multiple hundred gates used in the ASIC IP Core instead of multiple thousands of gates used in the current generation ASIC Products. Reduction number of errors like bit slip, error count etc. This is the universal receiver to interface with all electronic data automation products and applications wireless and telecom, consumer mobile multimedia, graphics processing , image ,video processing, data communication and networking, satellite, space, aerospace and autotomotive industrial automation applications . Also one more advantage of the product is to decrypt the multiple data frames at a time due to different parallel ports with very high bit rate speed weka bits per second speed. It is very smart digital computing A.S.I.C product by many more merits. The limitations are speed and performance, because of very futuristic ASIC Product.

Using the different PRBS Polynomial sequences can easily analyze the bit error rate using just like CRO/ Wave form Analyzers. These Polynomial sequences are analyzed by using different data pattern lengths. Error rates can easily analyzed in very high standard industrial data interface cards PCI ,PXI,PCI SATA, Serial Communication Protocol cards RS -232,485,SPI,USB,CAN,LIN etc. Due to Different to Different PRBS Sequence Lengths having standard deviation of bit error rates of every Protocol cards , For Example Standard deviation – If it is less than $10e^{12}$ error rate less and if it is > $10e^{12}$ the error rate more , like that every PRBS Data Frame Sequences-7,10,23,31,48,52,63 data frame sequences having Standard Deviation of Bit Error Rates. Similarly for all Very High standard industrial Serial data Acquisition cards having Standard Deviation of Bit error Rates of different width and lengths..

II. Ultra High multi channel Clock Frequency PRBS Transceiver Design Architecture

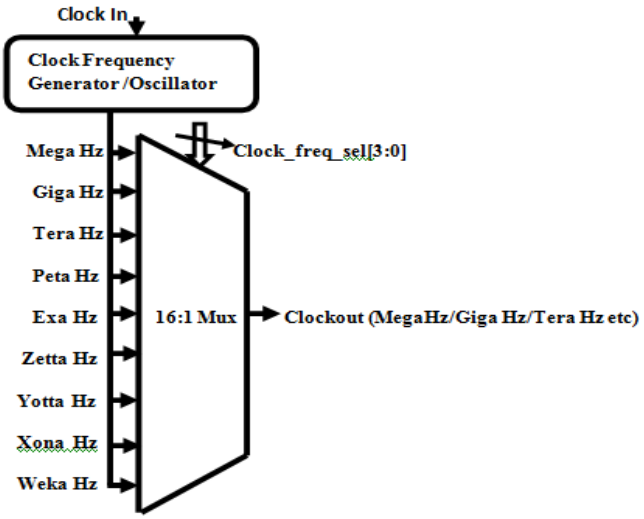

Fig.1: Multi Clock Frequency Generator

Description—Multi Clock Frequency Generator consists Clock Frequency Generator/Oscillator, 8:1 Multiplexer. Clock Frequency Generator . Generator consists Counter to Generates Different Clock Frequencies, MHz, GHz, THz, PHz, EHz, ZHz,YHz,XHz,WHz of 10^6 or 2^{20}, 10^9 or 2^{30}, 10^{12} or 2^{40}, 10^{15} or 2^{50} ,10^{18}or 2^{60} ,10^{21}or 2^{70}, 10^{24}or 2^{80}, 10^{27}or 2^{90} , 10^{30}or 2^{100} Clock Cycles. 9:1 Multiplexer Selects The one the above

frequencies to generate Baud Rate of Specific Clock. These frequencies are act as a clock input to the PRBS Receiver Design of Different Tapped Pattern Sequences.

Multi channel- PRBS Generators for Identification of property of various seed word patterns $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 Tapped sequences

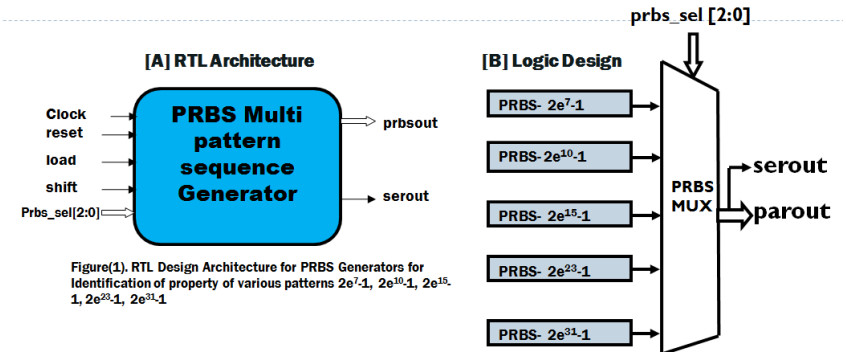

Fig. 2: Multi channel- PRBS Generators for Identification of property of various seed word patterns $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 Tapped sequences

Description: The $2e^7$-1 PRBS Generator consists 8 bit Linear feedback shift register. The Linear feedback shift register contains 8 D type Flip flops with feedback tapped DFF element positions(7,6) and the tapped positions 7 and 6 are XORED (compared) bit by bit and generates output. The output is feed back as input to the 8- bit LFSR(Linear feedback shift Register). Similarly Other PRBS generators of various data bit lengths of (10, 16, 24, 32 Dtype Flip Flops) with feed back tapping position DFF elements (10,3),(14,15),(18,23),(28,31) are xored and generates serial and parallel output of specified PRBS $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1. The purpose of tapping the elements of PRBS is for generate standard specific high frequency and baud rate as per CCITT & ITU (O.150/O.151/O.152) standards. The PRBS generates 256 random seed word numbers repeatedly. Based on the concept of n bit PRBS, The PRBS Generator contains n number of D type Flip flop elements. The Maximum length of PRBS is 2^L-1. The above figure(2) shows Logic Design Architecture for PRBS Generators of identification of property of various PRBS Patterns-$2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1. This PRBS generator consists of 8:1 multiplexer and 3 PRBS select lines The PRBS selector select particular PRBS pattern of above mentioned and generates PRBS output in the form of serial and parallel output.

Ultra High Frequency Multi channel PRBS Generator Design Architecture

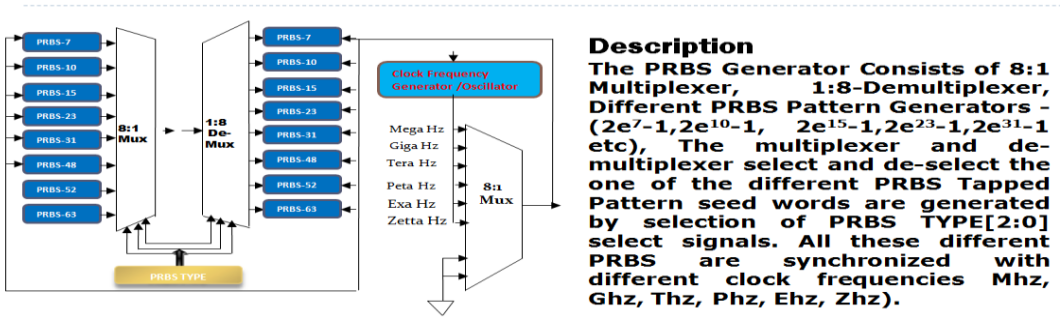

Fig.3: Multi Clock (Mega, Giga, Tera, Peta, Exa, Zetta Clock Frequency Multi Channel PRBS DESIGN ARCHITECTURE

Multichannel PRBS Receiver Architecture

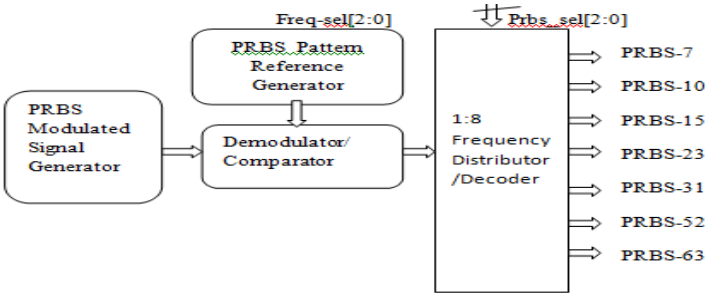

Fig.4: Multichannel PRBS Receiver Architecture

Description. The Architecture Consists of PRBS Reference Generator, Frequency De-multiplexer / Distributor Circuit (1:16), Comparator. The Comparator Receive one of the Different PRBS Transmitted Pattern Sequences (2^7-1,2^{10}-1,2^{15}-1,2^{23}-1,2^{31}-1 etc) and compare with PRBS Reference Pattern Sequence of specific PRBS Frame Sequence , and Deselect the sequence by 1:8 De-multiplexer for Receiver Output. Due PRBS Reference Generator , can easily Recognize different PRBS Pattern Sequence of pattern data lengths. The PRBS Modulated Signal Generator consists (2^7-1,2^{10}-1,2^{15}-1,2^{23}-1,2^{31}-1 etc) PRBS Carrier sequence merged with base band signal and easily detect these frame sequences by using PRBS Reference Generator and compared. The Frequency De-multiplexer/Distributor decodes all these PRBS Data Frame Sequences by identification of property of different pattern lengths. The advantages are that the random sequences are having repeat modes. Generate eye diagrams easily with specific high jitter tolerance.

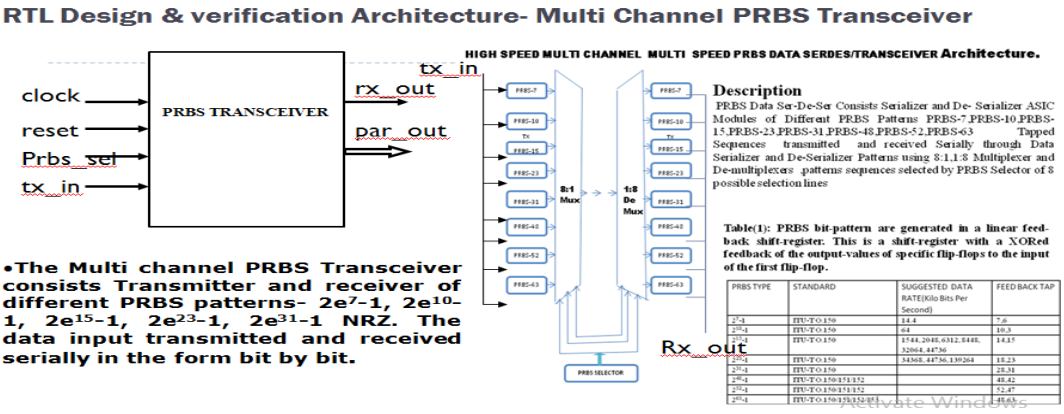

Fig.5: Multichannel PRBS Receiver Architecture

This Design is mainly intended for High Speed Multi pattern PRBS Generator of Sequence $2e^7$-1,$2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 ,$2e^{48}$-1, $2e^{52}$-1, $2e^{63}$-1 for Ultra High Speed Wireless Communication Engineering Applications 3rd&4th Generation of wireless communication & network products & Technologies (CDMA, GPS, GSM, WIFI, WIMAX, GiFi, Optical etc)as per CCITT- ITU Standards.

The PRBS Design Implemented based on the linear feedback shift register (LFSR).The family of Shift Registers are used to generate pseudo random binary sequences for Multi Kbps, Mbps & Gbps Speed.

Ultra High Frequency(MHz, GHz, THz, PHz, EHz, ZHz, YHz, XHz, WHz) clock MultiChannel PRBS Transceiver

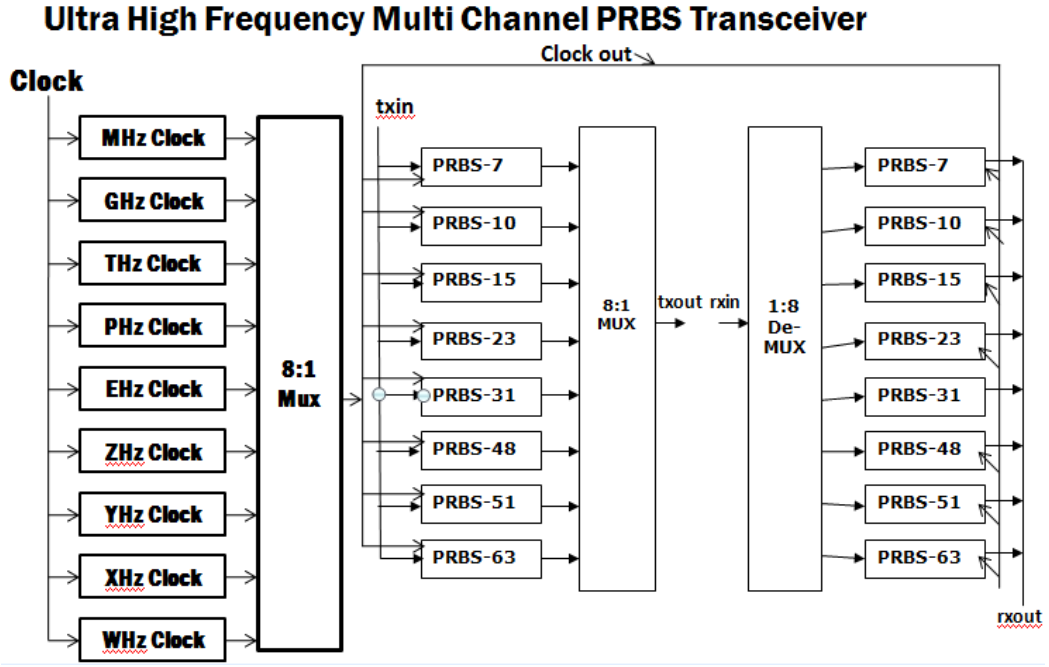

Fig. 6: New Invented PRBS Transceiver Design Architectures

The Above figure shown Ultra High Frequency (Mhz, Ghz, Thz, Phz, Ehz, Yhz, Xhz, Whz clock) multichannel PRBS Transceiver consists Transmitter and receiver of different PRBS tapped Carrier frequency generator patterns ($2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1).The low frequency transmitter input is modulated with these different high frequency carrier PRBS tapped sequence patterns to generate transmitted output. At the receiver side the same transmitted output is demodulated /decoded to generate original low frequency base band signal receiver output. All these multi channel PRBS Transceiver is synchronized with ultra high clock frequencies(Mhz, Ghz, Thz, Phz, Yhz, Xhz, Whz). These clock frequencies are generated by using 20, 30, 40, 50, 60, 70, 80, 90,100 bit counters and these clock frequencies(Mhz, Ghz, Thz, Phz, Ehz, Zhz, Yhz, Xhz, Whz clock) are generated by synchronizing and toggling at every posedge of $2^{20}/2$, $2^{30}/2$, $2^{40}/2$, $2^{50}/2$,$2^{60}/2$, $2^{70}/2$, $2^{80}/2$, $2^{90}/2$, $2^{100}/2$ clock cycle period with respect to main reference clock.

Due to ultra high frequency clock synchronization, The PRBS Transceiver suit for Very Advanced ASIC /SOC Communication engineering -Wireless & engineering communication SOC Applications and products. By using the SOC, could easily transmit and receive large packet transactions data with zero latency time and improve system performance and bandwidth of Any SOC Application/product.

The purpose of PRBS Transceiver is designed for very high speed long distance communication suit for Applications /products (CDMA, GPS, Satellite/space products) in terms of multiple thousands/lacks of km's.

RTL Design & Verification done by System Verilog/ Verilog RTL DUT and Test bench software.

Design Architecture For PRBS Multi Pattern Sequence Generator- PRBS ITU and AT&T Standard Design '

Architectures of Different Pattern Sequences $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1,$2e^{23}$-1, $2e^{31}$-1, $2e^{52}$-1, $2e^{63}$-1.

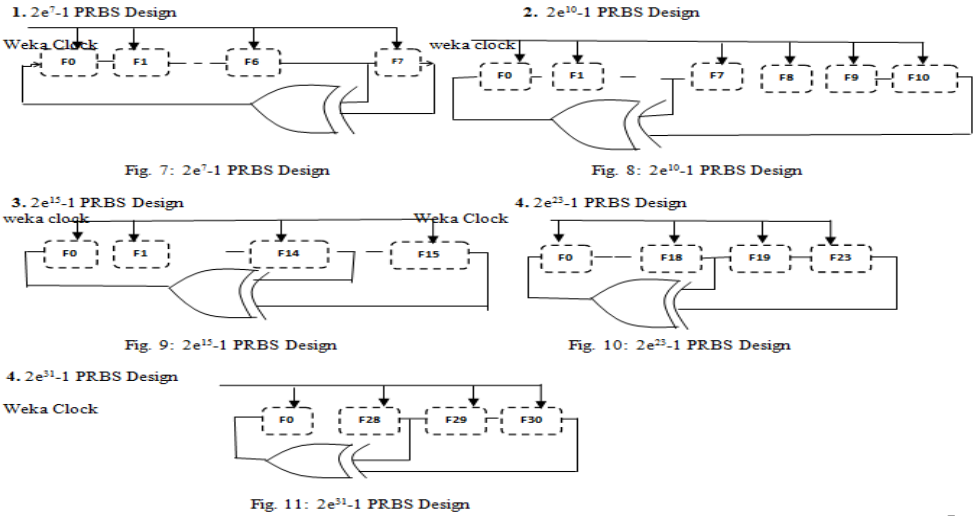

Fig. 7: $2e^{7}$-1 PRBS Design

Fig. 8: $2e^{10}$-1 PRBS Design

Fig. 9: $2e^{15}$-1 PRBS Design

Fig. 10: $2e^{23}$-1 PRBS Design

Fig. 11: $2e^{31}$-1 PRBS Design

Description: Fig. 7 shows PRBS-7 Sequence with tapping points 7 and 6 and sequence length is 2^{7}-1times the repeat sequences generated. Fig1.6 PRBS-10 Sequence with tapping points 10 and 7 and sequence lengths is 2^{10}-1times repeat the sequence.similalry other PRBS Sequences 15,23,31,48,52,63 with repeated pattern sequence lengths are 2^{15}-1,223-1,2^{31}-1,2^{48}-1,2^{52}-1,2^{63}-1.

PRBS Polynomial Data Equations

For PRBS 7^{th} Tapped Sequence , Mathematical equation is $Y = 1+X^{6}+ X^{7}$ (1.1)
For PRBS 10^{th} Tapped Sequence , Mathematical equation is $Y = 1+X^{3}+ X^{10}$ (1.2)
For PRBS 15^{th} Tapped Sequence , Mathematical equation is $Y = 1+X^{14}+ X^{15}$ (1.3)
For PRBS 23^{rd} Tapped Sequence , Mathematical equation is $Y = 1+X^{18}+ X^{23}$ (1.4)
For PRBS 31^{st} Tapped Sequence , Mathematical equation is $Y = 1+X^{28}+ X^{31}$ (1.5)
For PRBS 52^{nd} Tapped Sequence , Mathematical equation is $Y = 1+X^{47}+ X^{52}$ (1.6)
For PRBS 63^{rd} Tapped Sequence , Mathematical equation is $Y = 1+X^{52}+ X^{63}$ (1.7)

Description: The PRBS Sequences $2e^{7}$-1, $2e^{10}$-1,$2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1, $2e^{48}$-1, $2e^{52}$-1, $2e^{63}$-1 above Design Diagrams are represented in the form mathematical polynomial sequence models algorithms, can easily analyze the PRBS sequences.

Table 1.1 CCITT-ITU PRBS STANDARD TABLE- Single & Double Precision Standards

PRBS Type, Tap	Standard	Data Rate(kbps)	Feedback
$10e^{7}$-1	ITU-T O.150	14.4	7^{th} ,6^{th}
$10e^{10}$-1	ITU-T O.150	64	10^{th} ,3^{rd}
$10e^{15}$-1	ITU-T O.150	1544,2048,6312 , 8448,32064,44736	14^{th} ,15^{th}
$10e^{23}$-1	ITU-T O.150	34368, 44736,139264	18^{th} ,23^{rd}
$10e^{31}$-1	ITU-T O.150	$1.5 * 10^{6}$, $1.2*10^{6}$	28^{th},31^{st}
$10e^{48}$-1	ITU-T O.150/O.151/O.152	$1.5*10^{9}$, $1.2*10^{9}$	48^{th},42^{nd}
$10e^{52}$-1	ITU-T O.150/O.151/O.152	$1.5*10^{12}$,$1.2*10^{12}$	52^{nd},47^{th}
$10e^{63}$-1	ITU-T O.150/O.151/O.152	$1000*10^{12}$,$1200*10^{12}$	59^{th} ,63^{rd}

Note: Table Designed as per ITU, IEEE-754 Standards

VLSI – IC Software Design Flow Chart

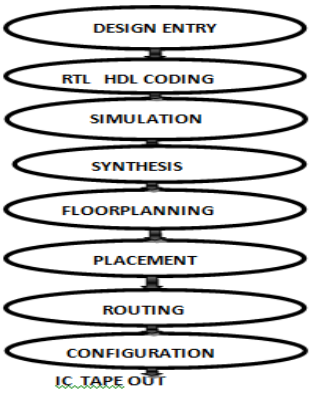

Fig. 12: VLSI IC- EDA Software Design Flow Chart

Description: This is Standard Industry Design Flow Chart for Delivery of VLSI IC Chip Design Soft IP Core Products/Designs. Initially entering RTL Design through Design Entry Step, After That RTL VHDL & / Verilog HDL Coding Done through HDL RTL Design Software Editor of both behavioral and Data flow models. Verification & Running the Functionality of RTL HDL Design Description through by Simulation and Abstract the Description in to Gate Level Net list using Synthesis, subsequently Place & Routing through FPGA Placed Design & Router and Programming and Debugging Done through Reconfiguration using JTAG Debugger. All the Design flow reports generated by using Xilinx ISE 10.1i ISE Software Design Tool.

III. Simulation and Synthesis Results

Chronologic VCS simulator copyright 1991-2020
Contains Synopsys proprietary information.
Compiler version Q-2020.03-SP1-1; Runtime version Q-2020.03-SP1-1; Jul 12 08:41 2022
15prbs7 tapped seq tx_in = 0,tx_out = 0, rx_in = 0, rxout = 0, tx =
000000000000000000000000000000000000000000000000000000000000000000000000, rx =
000000000000000000000000000000000000000000000000000000000000000000000000
35prbs7 tapped seq tx_in = 1,tx_out = 1, rx_in = 1, rxout = 1, tx =
000000000000000000000000000000000000000000000000000000000000000000000001, rx =
000000000000000000000000000000000000000000000000000000000000000000000001
55prbs7 tapped seq tx_in = 1,tx_out = 1, rx_in = 1, rxout = 1, tx =
000000000000000000000000000000000000000000000000000000000000000000000011, rx =
000000000000000000000000000000000000000000000000000000000000000000000011
75prbs7 tapped seq tx_in = 1,tx_out = 1, rx_in = 1, rxout = 1, tx =
000000000000000000000000000000000000000000000000000000000000000000000111, rx =
000000000000000000000000000000000000000000000000000000000000000000000111
95prbs7 tapped seq tx_in = 0,tx_out = 0, rx_in = 0, rxout = 0, tx =
000000000000000000000000000000000000000000000000000000000000000000001110, rx =
000000000000000000000000000000000000000000000000000000000000000000001110
135prbs10 tapped seq tx_in = 1,tx_out = 1, rx_in = 1, rxout = 1, tx =
000000000000000000000000000000000000000000000000000000000000000000000011, rx =
000000000000000000000000000000000000000000000000000000000000000000000011
155prbs10 tapped seq tx_in = 1,tx_out = 1, rx_in = 1, rxout = 1, tx =
000000000000000000000000000000000000000000000000000000000000000000000111, rx =
000000000000000000000000000000000000000000000000000000000000000000000111
285prbs15 tapped seq tx_in = 0,tx_out = 0, rx_in = 0, rxout = 0, tx =
000000000000000000000000000000000000000000000000000000000000000000000110, rx =
000000000000000000000000000000000000000000000000000000000000000000000110
305prbs15 tapped seq tx_in = 0,tx_out = 0, rx_in = 0, rxout = 0, tx =
000000000000000000000000000000000000000000000000000000000000000000001100, rx =
000000000000000000000000000000000000000000000000000000000000000000001100
385prbs24 tapped seq tx_in = 0,tx_out = 0, rx_in = 0, rxout = 0, tx =
000000000000000000000000000000000000000000000000000000000000000000001100, rx =
000000000000000000000000000000000000000000000000000000000000000000001100

405prbs24 tapped seq tx_in = 1,tx_out = 1, rx_in = 1, rxout = 1, tx =
00000000000000000000000000000000000000000000000000000000011001, rx =
00000000000000000000000000000000000000000000000000000000011001
465prbs32 tapped seq tx_in = 0,tx_out = 0, rx_in = 0, rxout = 0, tx =
00000000000000000000000000000000000000000000000000000000000100, rx =
00000000000000000000000000000000000000000000000000000000000100
525prbs48 tapped seq tx_in = 0,tx_out = 0, rx_in = 1, rxout = 1, tx =
00000000000000000000000000000000000000000000000000000000010011, rx =
00000000000000000000000000000000000000000000000000000000010011
V C S S i m u l a t i o n R e p o r t
Time: 1500 ns
CPU Time: 0.400 seconds; Data structure size: 0.0Mb
Tue Jul 12 08:41:16 2022
Finding VCD file...
./dump.vcd
[2022-07-12 08:41:16 EDT] Opening EPWave...
Done

Simulation waveforms and FPGA Layouts

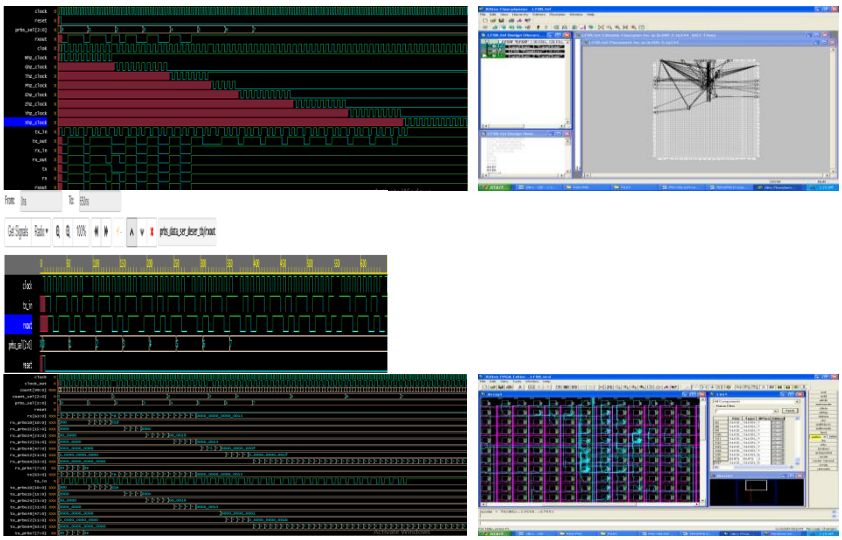

Fig. 13: Multi channel PRBS Transceiver Simulation wave and FPGA Synthesis layouts.

IV. Conclusion

Designed and Verification of new invention HDL clock generators- mega, giga, tera, peta , exa, zetta, Yotta, xona, weka hertz frequencies synchronized PRBS RTL Design TRANSCEIVER ASIC FOR IDENTIFICATION OF PROPERTY OF $2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, and 2e31-1 TAPPED PATTERN SEQUENCES AS PER C.C.I.T.T- I.T.U STANDARDS FOR ULTRA HIGH SPEED long distance SMART DIGITAL WIRELESS COMMUNICATION PRODUCTS & APPLICATIONS space and satellite distance level with various features like performance, speed, high quality modulation and demodulation, standard encryption and de-cryption, large data computing and data serialization and deserialization, error rate anlaysis and fault injection, detection and simulation for advanced future usage.

Future Scope: For ultra high speed long distance communication applications

Acknowledgements

I Sincerely Thankful to our Co-Author for their Valuable Support w.r.t this

References

[1]. "ITU-T Recommendation O.150". October 1992.
[2]. Tomlinson, Kurt (4 February 2015). "PRBS (Pseudo-Random Binary Sequence)". Bloopist. Retrieved 21 January 2016.
[3]. Paul H. Bardell, William H. McAnney, and Jacob Savir, "Built-In Test for VLSI: Pseudorandom Techniques", John Wiley & Sons, New York, 1987.
[4]. Wikipedia, "http://en.wikipedia.org/wiki/ Pseudorandom_binary_sequence"
[5]. Wikipedia "http://en.wikipedia.org/wiki/ Linear_feedback_shift_register"
[6]. SY Hwang, GY Park, DH Kim, KS Jhang, "Efficient Implementation of a Pseudorandom Sequence Generator for High-Speed Data Communications", ETRI Journal, Volume 32, Number 2, April 2010.
[7]. ITU – CCITT Reference Document [1] A Chow, WS Coats, D Hopkins, "A Configurable Asynchronous Pseudorandom Bit Sequence Generator", 13th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 07), Page(s): 143 - 152, March 2007.
[8]. Xilinx Data Sheet XAPP884 (v1.0) January 10, 2011
[9]. 1730Ahmad, A., Nanda, N. K., and Garg, K., MAC WILLIAMS, FJ 1976, Pseudo Random Sequences & Arrays , IEEE Proc., 1715- "An efficient design of maximal length of pseudorandom test pattern generators," Proceedings of IEEE international conference on signals & systems
[10]. *Riccardi, Daniele; Novellini, Paolo (10 January 2011).* "An Attribute-Programmable PRBS Generator and Checker (XAP884)" (PDF). Xilinx. *Table 3:Configuration for PRBS Polynomials Most Used to Test Serial Lines*. Retrieved 21 January 2016.
[11]. "O.150 : General requirements for instrumentation for performance measurements on digital transmission equipment"
[12]. https://www.intel.com/content/www/us/en/docs/programmable/683621/current/prbs-pattern-generator.html
[13]. Paul H. Bardell, William H. McAnney, and Jacob Savir, "Built-In Test for VLSI: Pseudorandom Techniques", John Wiley & Sons, New York, 1987.
[14]. SY Hwang, GY Park, DH Kim, KS Jhang, "Efficient Implementation of a Pseudorandom Sequence Generator for High-Speed Data Communications", ETRI Journal, Volume 32, Number 2, April 2010.
[15]. Ahmad A. and Elabdalla A. M., "An efficient method to determine linear feedback connections in shift registers that generate maximal length pseudo-random up and down binary sequences," *Computer & Electrical Engineering - An Int'l Journal (USA),* vol. 23, no. 1, pp. 33-39, 1997 [7] Ahmad, A., Al Musharafi, M.J.,

Prof. Executive Dean. P.N.V.M Sastry, et. al. " Ultra High multi channel clock frequency(THz, PHz, EHz, ZHz,YHz,XHz,WHz) baud rate speed PRBS Transceiver HDL RTL ASIC Design for Ultra High long Distance Wireless Communication Engineering Smart Computing Products/ Applications." *IOSR Journal of VLSI and Signal Processing (IOSR-JVSP)*, vol. 12, no. 4, 2022, pp. 08-17