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Investigation The Effect Of Gate Oxide Thickness On PD SOI MOSFET Characteristics

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Abstract: *Silicon on insulator (SOI) technology permits a good solution to the miniaturization as the MOSFET size scales down.This paper is about to compare the electrical performance of partially depleted (PD)SOI MOSFET at various gate oxide thickness.The performance is compared and contrasted with the help of threshold voltage, subthreshold slope, on-state current and leakage current. Interestingly, by decreasing the gate oxide thickness, the leakage current and on-state current is increased but the threshold voltage is decreased and the sub-threshold slope is improved. Silvaco two-dimensional simulations are used to analyze the performance of the proposed structures.*

Key Word*: MOSFET, Silicon on Insulator, Subthreshold Slope, Leakage Current, Threshold Voltage.*

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I. Introduction

Silicon on Insulator Metal Oxide Semiconductor Field Effect Transistor (SOI-MOSFET) has various unique features like enhanced sub-threshold slope, less parasitic capacitance, lower noise, minimal short channel effects (SCEs) as well as protection from electrostatic discharge [1–3]. Today devices of minimized area, reduction in power and increased performance have a great need in the industry of microelectronics. Different structures such as partially depleted (PD) SOI, fully depleted (FD) SOI and multiple-gate architectures have been proposed to resolve this issue. Reduction of junction capacitance and benefit of reduced area of source and drain regions are the intrinsic advantage making these devices a potential candidate for reduced voltage and power applications [4-6]. The thicker substrate which is the active region makes PD SOI easier to manufacture than FD-SOI [7]. PD-SOI is an evolutionary technology advance from bulk silicon devices adding only the oxide layer. So the technology for bulk can be easily adapted for PD SOI technology [8]. The silicon film thickness in PD SOI devices has less impact in the threshold voltage variation. Consequently, several better performance and low-power chips are designed using the PD SOI. So it becomes essential to explore the PD-SOI device since it is a potential candidate for downscaling of the CMOS technique. The competitive market will also benefit from the investigation of PD SOI.

This paper presents partially depleted SOI devices in terms of electrical characteristics. TCAD Silvaco software is used for simulation study of SOI devices. Simulation results revealed that the electrical characteristics such as threshold voltage, sub threshold slope, on-state current and leakage current of partially depleted SOI devices vary with gate oxide thickness.

II. Methodology

To study the electrical parameters on PD SOI MOSFET a schematic cross-sectional view of the SOI MOSFET is simulated using Silvaco TCAD device simulator, is shown in Fig. 1. We assumed light channel doping concentration (1×10^{17} cm^{-3}) to avoid degrading of carrier mobility and more V_t variations. The doping concentration of source/drain region is kept at 1×10^{20} cm^{-3}. Gate length of the device that had been concentrated is 1 μm. Gate oxide (SiO2) thickness and BOX thickness are 25 nm and 0.4 μm respectively. Besides, thickness of silicon film is 0.3 μm. The total device length including drain, channel and source is 3 μm. Shockley-Read-Hall recombination, Lombardi CVT mobility model and impact ionization model from Selberherr [9] are used for the simulation. Numeric methods used for simulation are Newton methods. We assumed n channel device and simulated the device for different gate oxide thickness of PD SOI MOSFET.

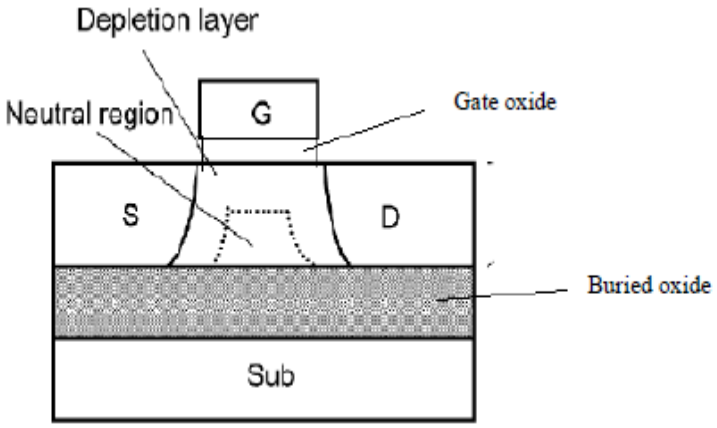


Fig.1. Schematic view of PD SOI MOSFET

III. Results and Discussion

The simulation and investigation of electrical parameters of n-channel PDSOI MOSFET has been carried out by using Silvaco TCAD simulation software. The SOI structures are created using Atlas syntax and the simulation results are displayed in TonyPlot. The thickness and material are defined when specifying the structure region. Fig.2 shows the simulated PD SOI structure with gate oxide thickness of 25 nm and Fig.3 shows doping profile of simulated PD SOI MOSFET.

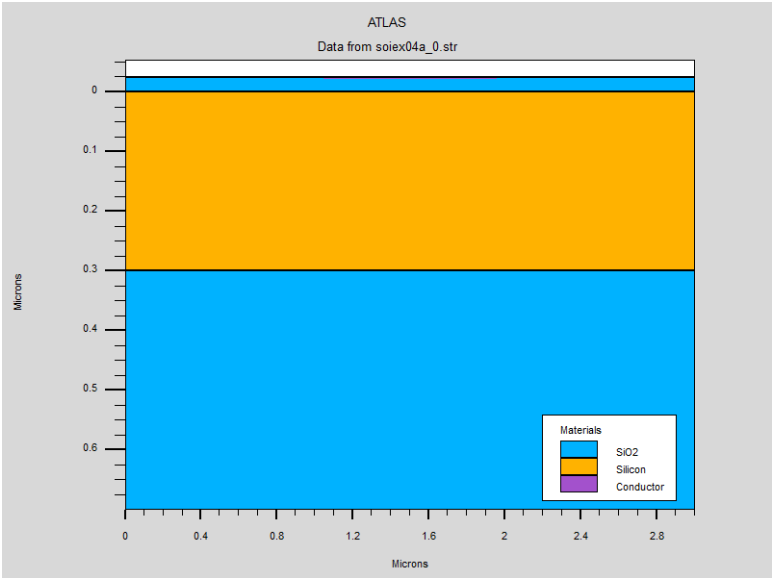


Fig.2. Simulated structure of N-channel PD SOI MOSFET

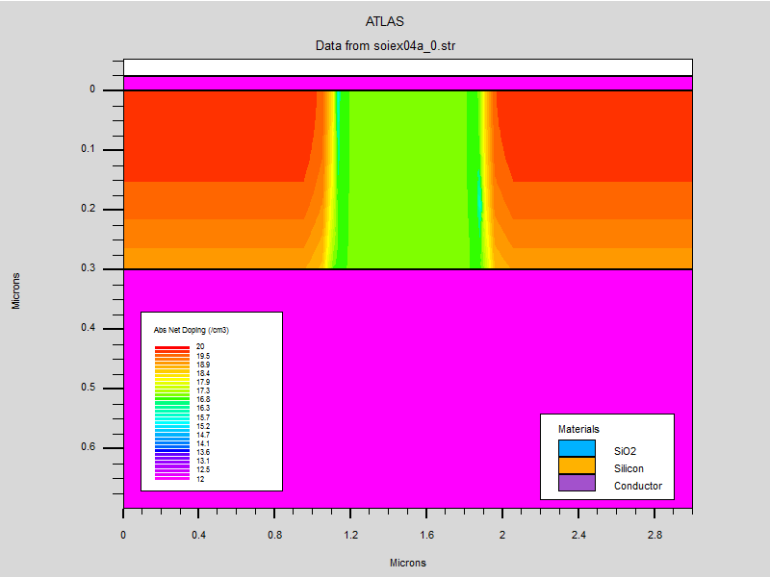


Fig. 3 Doping profile of simulated PD SOI MOSFET

By changing the gate oxide thickness, the electrical parameters of PD SOI MOSFET are recorded as shown in Table 1. The results in Table I are analysed and graph of electrical characteristics versus gate oxide thickness are plotted.

Table no 1. Shows electrical characteristics of PD SOI n-MOSFET at different gate oxide thickness with 0.3 μm of silicon on 0.4 μm oxide substrate.

Gate Oxide Thickness,Tox(nm)	Threshold Voltage,Vth(V)	Subthreshold slope(mV/dec)	On-state current, I_{on} (A)	Leakage current, I_{off} (pA)
2	0.00166	65.64	0.00086	924052
5	0.12175	70.5083	0.000333	16573.1
10	0.33704	80.4805	0.00013	56.7037
15	0.5577	90.7023	6.25E-05	0.88936
20	0.78056	100.964	2.99E-05	0.051
25	1.00312	110.884	1.30E-05	0.00616

Fig. 4 shows the comparison of Ids/Vgs characteristics of PDSOI n-MOSFET. Initially, drain current remains zero and the current raises as the gate voltage increases until it reaches the threshold voltage. With technology scaling, smaller value of threshold voltage is needed to satisfy high performance of device [10]. From the result, it can be said that the threshold voltage of PDSOI n-MOSFET is smaller for smaller gate oxide thickness.

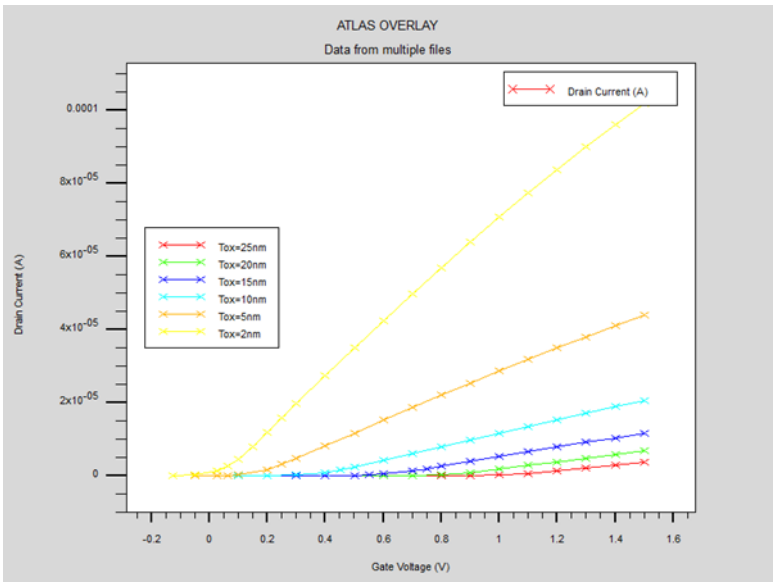


Fig. 4 Simulated transfer characteristics Ids-Vgs of PDSOI n-MOSFET with channel length L=1 μm and for various gate oxide thickness Tox

By varying the gate oxide thickness, the result of threshold voltage has been recorded and the graph of threshold voltage versus gate oxide thickness is plotted and shown in Fig. 5. From Fig. 5, it can be said that the thinner the gate oxide thickness, higher the gate oxide capacitance and consequently the lower the threshold voltage.

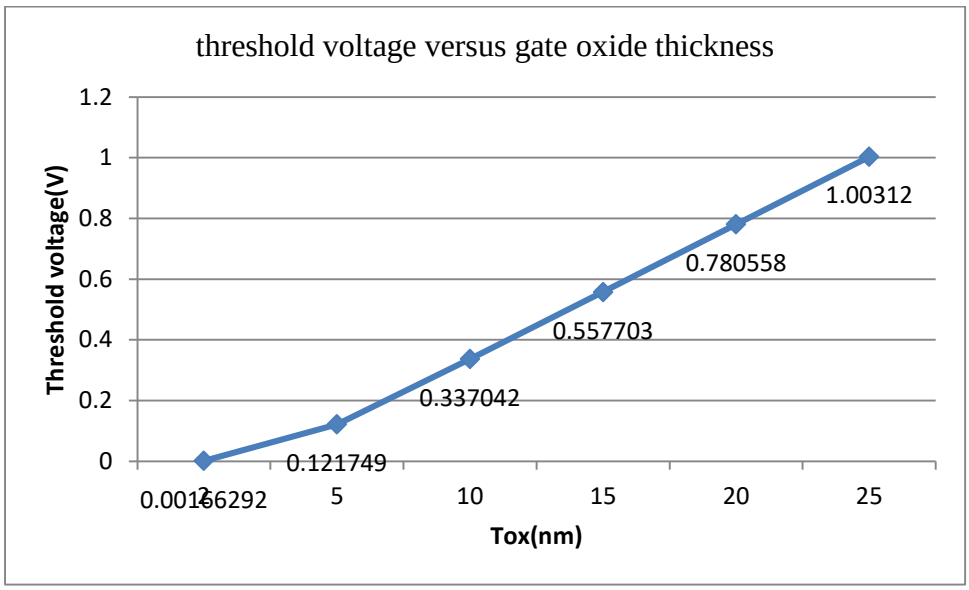
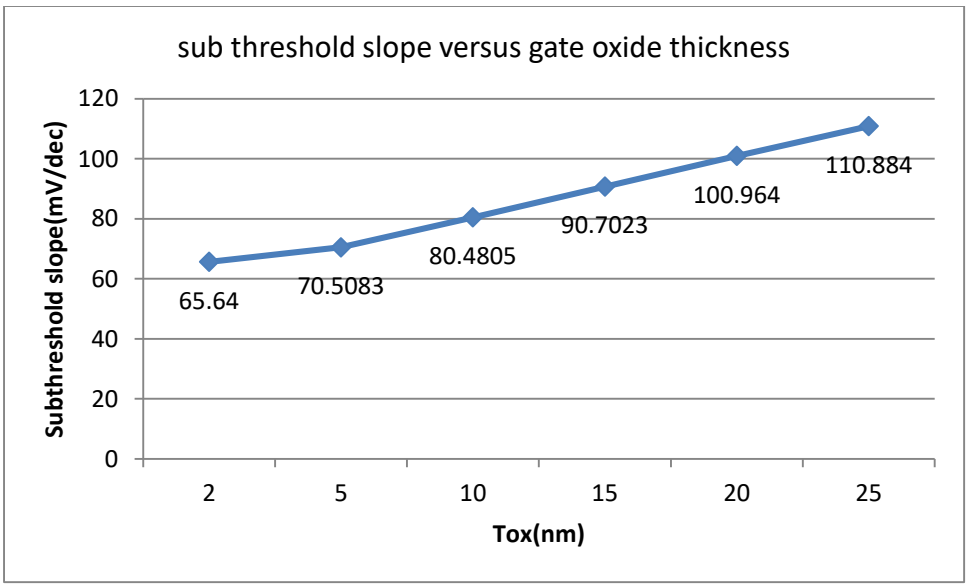


Fig.5 Graph of threshold voltage versus gate oxide thickness of PD SOI

The reason of fast operation is because of a sharper sub-threshold slope and threshold voltage reduction which allows a more rapidly switching of MOSFET [11].Subthreshold slope is a measure of how quickly the transistor can be turned on/off. The smaller subthreshold value indicates the device rapidly switches from off to on state.The graph of subthreshold slope versus gate oxide thickness is shown Fig.6. As gate oxide thickness decreases, the steeper subthreshold slope becomes as from Fig.6 which strongly increases the device speed.



. Fig.6 Graph of sub threshold slope versus gate oxide thickness of PD SOI

Fig. 7 (a), (b), (c),(d),(e) and (f) shows the subthreshold slope of PDSOI at various gate oxide thickness. As gate oxide thickness decreases from 25 nm to 2 nm, subthreshold slope improves from 110.884 mV/dec to 65.64 mV/dec.

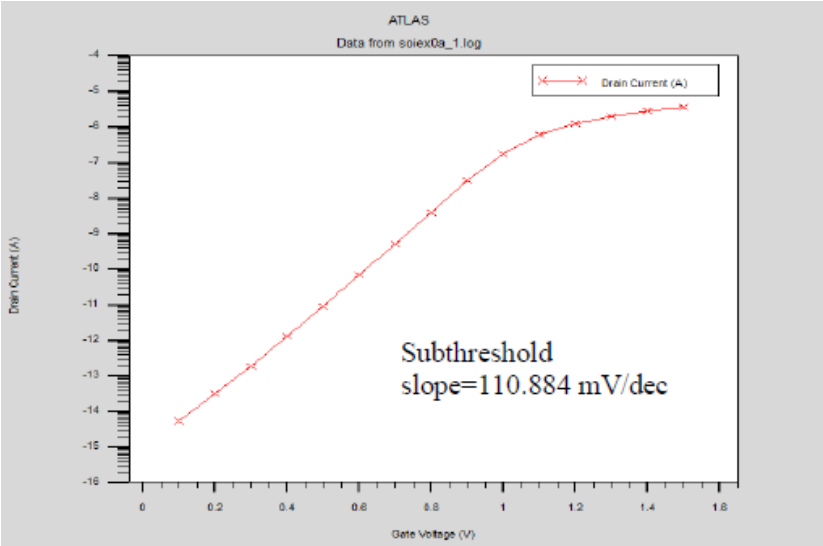


Fig.7(a) Subthreshold slope of PDSOI n-MOSFET of Tox=25 nm

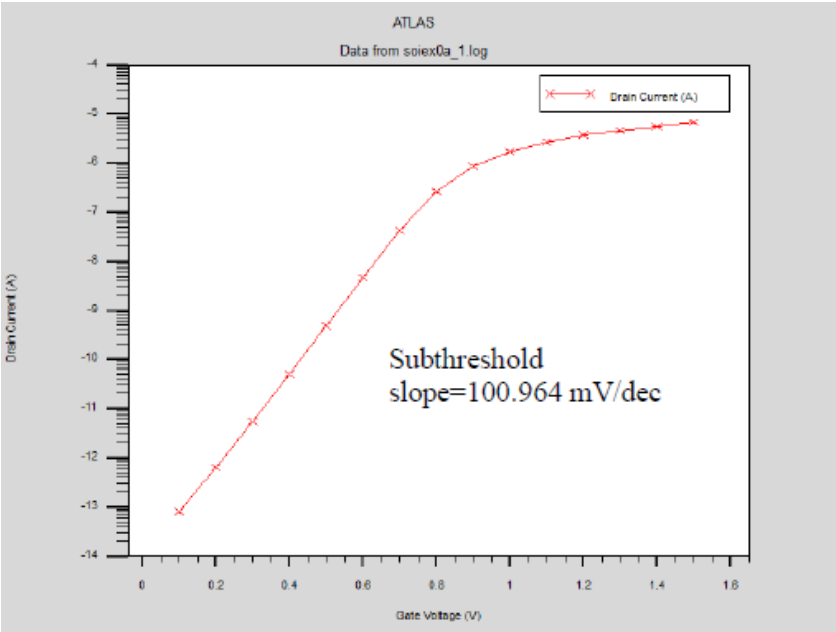


Fig.7(b) Subthreshold slope of PDSOI n-MOSFET of Tox=20 nm

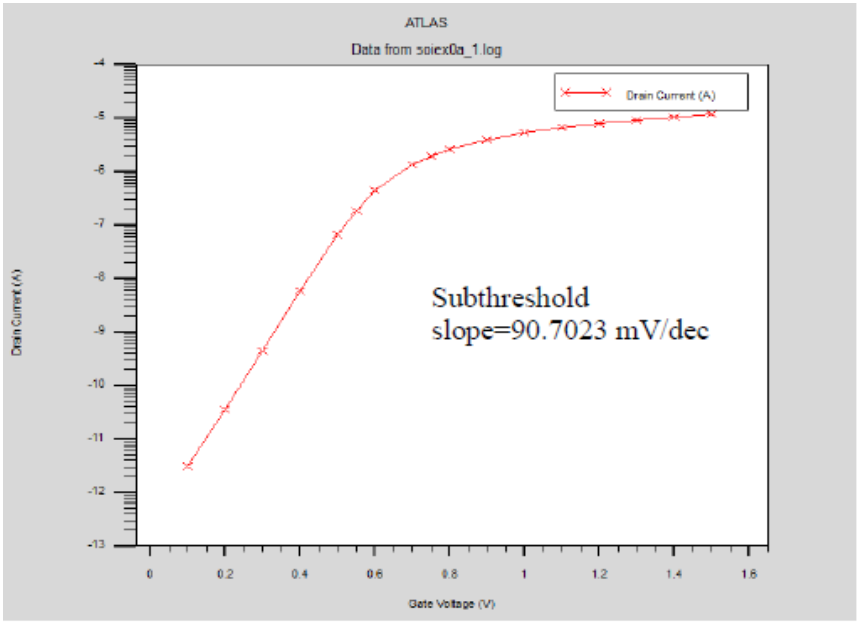


Fig.7(c) Subthreshold slope of PDSOI n-MOSFET of Tox=15 nm

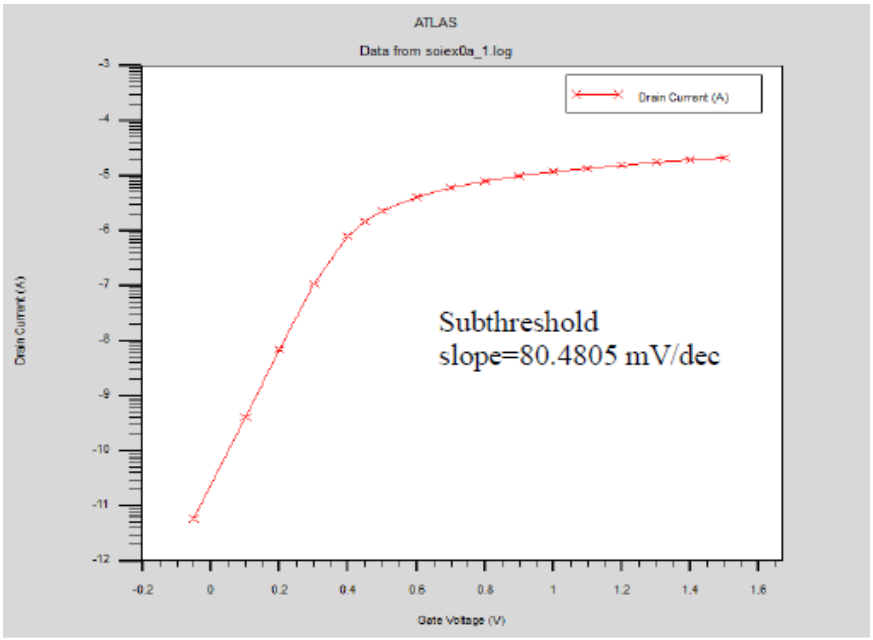


Fig.7(d) Subthreshold slope of PDSOI n-MOSFET of Tox=10 nm

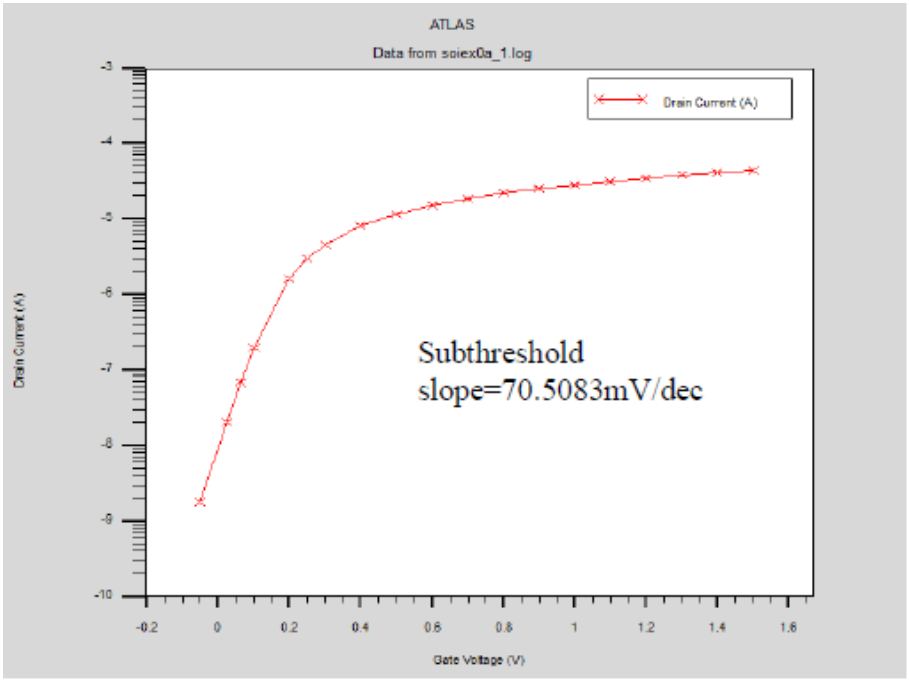


Fig.7(e) Subthreshold slope of PDSOI n-MOSFET of Tox=5 nm

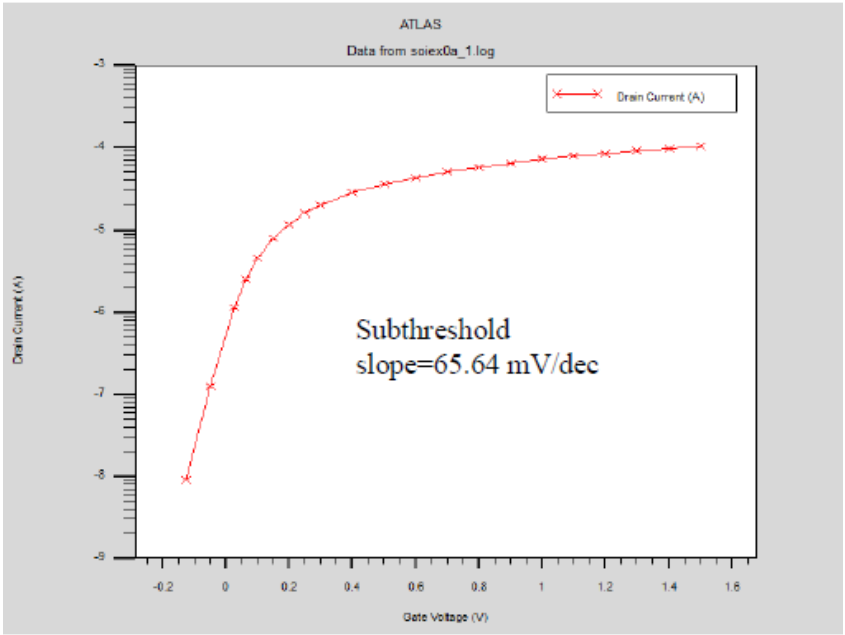


Fig.7(f) Subthreshold slope of PDSOI n-MOSFET of Tox=2 nm

A high on-state current(I_{on}) helps to increase the operating speed of the device. The graph Ion versus gate oxide thickness is shown in Fig.8. From Fig. 8, it can be said that the thinner the gate oxide thickness, the higher the on-state current.

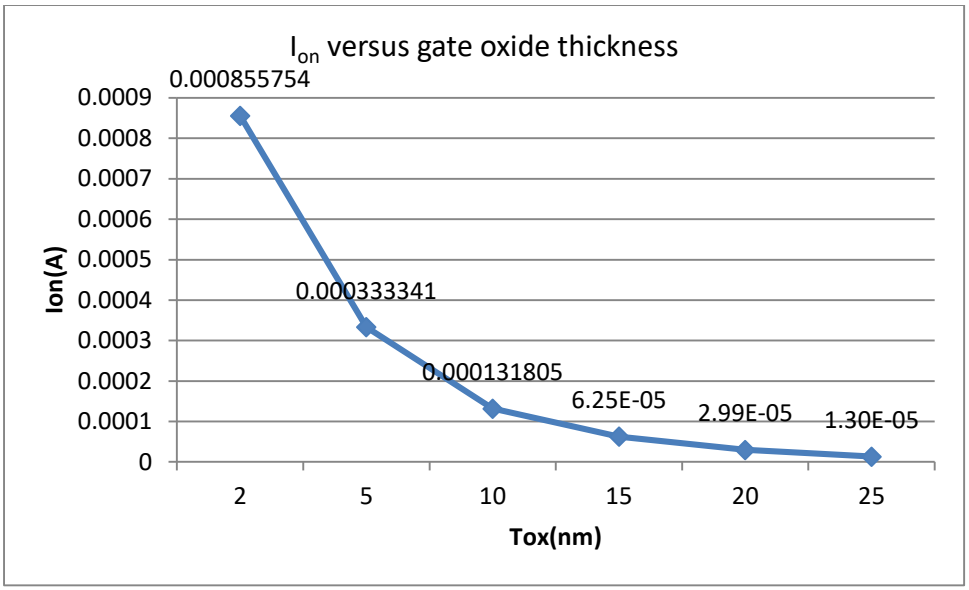


Fig.8 Graph of Ion versus gate oxide thickness of PD SOI

The result of leakage current(I_{off}) is inversely proportional to the threshold voltage [12]. This means that value of leakage current becomes smaller with the increasing of threshold voltage. The higher the threshold voltage, the smaller the leakage current. MOSFET device will fail when excessive leakage current occurs. Large leakage current of conventional semiconductor is caused by the electron-hole pair generation due to ionizing radiations.The graph of leakage current versus gate oxide thickness is shown in Fig.9. Leakage current contributes to static power dissipation and leakage power dissipation is caused by current flow when input transition is absent and transistor achieved steady state. Leakage power dissipation is caused by current flow when input transition is absent and transistor achieved steady state [13]. Thus, by having a smaller leakage current, static power dissipation will be less. Thus, from the result the PDSOI with larger gate oxide thickness will have a lower static power dissipation .

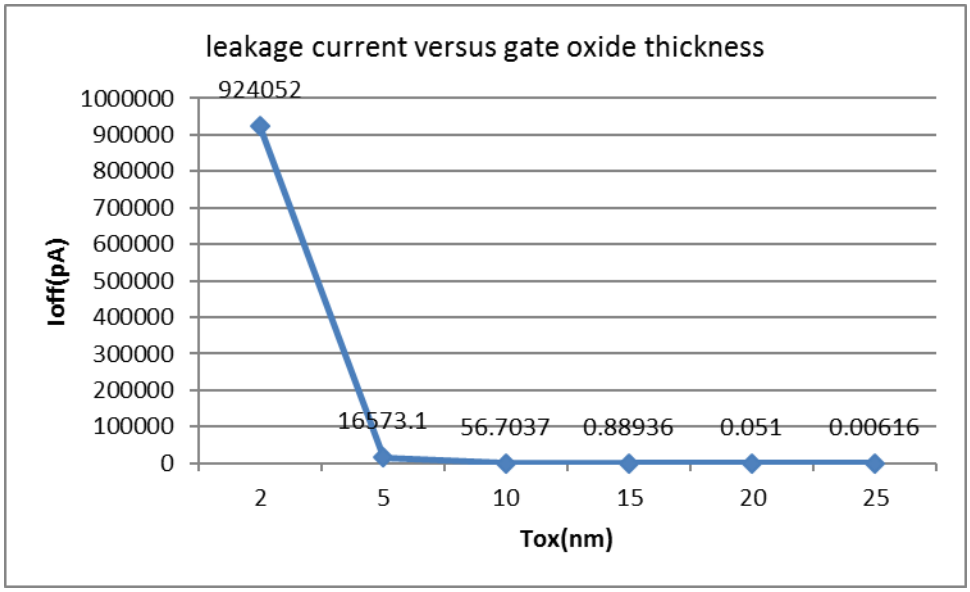


Fig.9 Graph of leakage current versus gate oxide thickness of PD SOI

IV. Conclusion

PD SOI has been compared in terms of electrical characteristics using Silvaco T-CAD Simulator by varying gate oxide thickness. It is found that the threshold voltage decreased with decrease in gate oxide thickness. So the device can be used for low power application. The subthreshold slope improved and on-state current increased with decrease in gate oxide thickness which increases the device speed. The leakage current increases with decrease in gate oxide thickness which result in increase in static power dissipation.

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