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Design Process, Simulation,and Analysis of a Common Source MOS Amplifier Circuit in Cadence at 45 nm CMOS Technology Node

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Abstract:
This work describes a design process, simulation, and analysis of a CMOS-based common source amplifier circuit in the Cadence Virtuoso environment at the 45nm technology node. The suggested CMOS circuit may be useful in the op-amplifier or other circuits.The circuit is designed to work with a 1.8V DC power source. The circuit is constructed from two complementary NMOS and PMOS transistors having a 45 nm gate length. The gate widths are chosen as 1 and 2 μm, respectively. Transistors are selected from the gpdk045 library of the Cadence. For the simulation purpose, we have used two sources from the AnalogLib library- one is a DC bias source and the other is a pulse source for the input signals. After designing the circuit, the circuit was simulated to test and assess various performance factors, including gain, phase margin, gain bandwidth, power dissipation, etc. Simulation results confirm that the designed circuit works well at this node. This type of design and simulation experience can give confidence to fabrication engineers regarding its functionality and reliability.

Keywords*:CMOS; Common Source Amplifier; Cadence; Bandwidth; Gain; Technology Node; VLSI.*

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I. Introduction

In the VLSI circuits,MOSFET is the basic functional unit [1]. The size of this device is being reduced gradually to accommodate more transistors in the same area of an integrated circuit following Moor's law [1, 2]. However, the reduced transistors have several detrimental effects, such as short channel effects [3, 4], noise problem [5, 6], subthreshold drain current effect [7, 8], mobility degradation [9], surface potential barrier lowering issue [10, 11], impact of temperature [12, 13], etc. Therefore, before using the MOS transistors at the reduced scale, we must observe the behavior of the circuits in an actual case.

A common-source amplifier circuit is one of the three fundamental single-stageComplementary Metal-Oxide-Semiconductor Field-Effect Transistor (CMOS)-based amplifier topologies in electronics [14]. It is frequently employed as a voltage or transconductance amplifier. However, due to the downsizing of the transistor, its supply voltage has been cut down, too. As a result, dynamic voltage range and voltage gain are also reduced [15].In this work, we aim to examinethe design of a common source CMOS amplifier topology at the 45 nm CMOS technology node. We worked using the Cadence Virtuoso simulation tool's gpdk045.Currently, the available working technology nodes in Cadence are 180, 90 nm, 65 nm,and 45 nm [16]. In thisarticle, we designed a common source CMOS amplifier circuit at a 45 nm technology node, then simulated the amplifier circuit to get various outputs and parameters, and evaluated their performances.

II. Literature Review and Problem Statement

In the literature, it was found that a method based on transconductance versus normalized drain current was developed to design a transconductance by drain current with active load. They used this method to model the device dimension and keep the assumed design specifications, such as gain, bandwidth, the product of gain and bandwidth, supply voltage (1.8 V), intake power, etc. within the desired ranges. To design their circuit, they used the Cadence Virtuoso tool at various technology nodes of 180nm, 90nm, 45 nm, etc. [14].

Another research paper examined the transconductance-boosted common source amplifier circuit with source degeneration. They investigated a thorough small signal analysis of the mid-band characteristics of this circuit having high input impedance. They also discussed the structural transformation of their circuit and they compared their results with other circuits through simulations [17].

In another research paper, the memristor device was modeled for a common source amplifier circuit in theCadence Virtuoso simulation environment at 180 nm technology. This device establishes a relationship between the flux and charge [18].

In a recently published research paper, the authors have presented a method for designing a common source amplifier circuit for an operational amplifier that usesa differentialamplifier also in the Cadence Virtuoso design environment based on a 180nm CMOS technology node [19].

In another paper, the behavior of a multiple-stage amplifier for anop-amp circuit was observed using Cadence based on CMOS technology. They designed the op-amp-based differential amplifier and gain amplifier. Theprimary stage is a differential amplifier to eliminate the noise signal and amplify the input signal. To meet the requirements, the gain amplifier, which is a common source amplifier,boosts the signal level further [20].

III. Common Source Amplifier Design

The goal of an amplifier is to produce an output signal that is an exact reproduction of the input signal but with a higher magnitude. Without altering the input signal or information, an amplifier amplifies or strengthens the weak signal. Amplifiers employ negative feedback to produce a stable output signal.

A block diagram of the Common Source (CS) amplifier circuit drawn in Cadence is portrayed in Fig. 1. In this illustration, we applied four sources to four different input terminals, such as input and bias signals for the different MOS terminals. Two sources at the drain and source terminals used are DC voltage sources from the analog library of the Cadence tool, and the applied voltages for these two sources are +2.5 V and -2.5 V, respectively. The applied input voltage at the input terminal is an AC voltage source with 4 mV at 1 kHz frequency. The third bias voltage at the bias voltage terminal is -900 mV, DC.

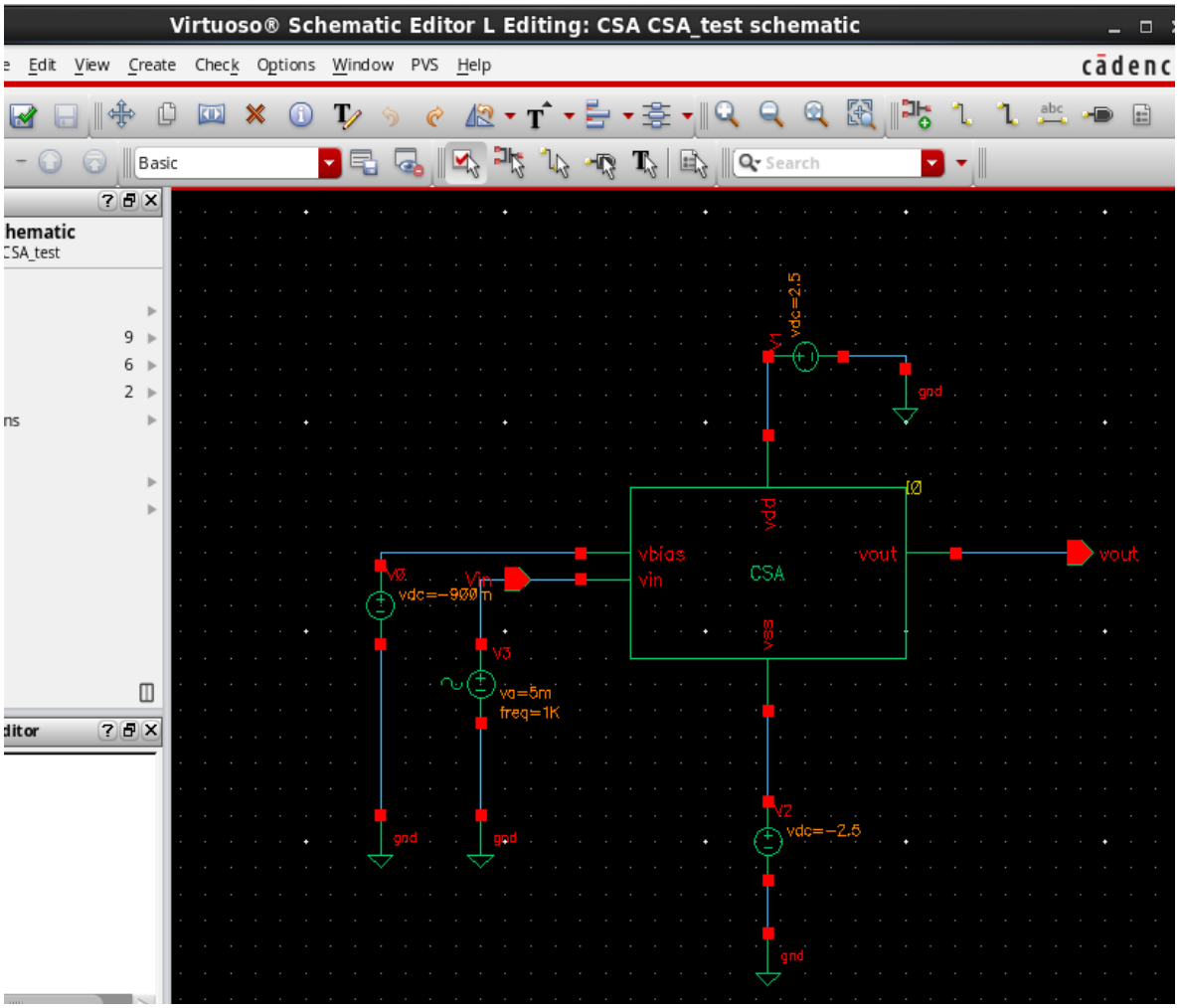

Figure 1. Block diagram representation of a common source amplifier circuit

We used NMOS and PMOS transistors in the CMOS circuit from the gpdk045 library of the Cadence design tool. The Table 1 presents the design parameters including the library and cell view names used for the common source amplifier circuit.

Table 1. Design and simulation parameters used in the Cadence environment

Library Name	Cell View Name	Properties
gpdk045	pmos1v	Total Width = 2u, Length = 45n
gpdk045	nmos1v	Total Width = 1u, Length = 45n
analogLib	vpulse (as input signal)	voltage1=0, voltage2=1.8, period =20n, pulse width= 10n
analogLib	vac	Start Frequency = 100 Hz, End Frequency = 1 GHz
analogLib	vdc	DC voltage =1.8
analogLib	vdd	
analogLib	vss	
analogLib	gnd	

The completeschematiccircuit diagram of the CS amplifier circuit is shown in Fig. 2. The drain of the PMOS transistor is connected to the Vdd source, the source of the NMOS transistor is connected to the Vss source, the gate of the PMOS transistor is connected to the Vbiassource, the gate of the NMOS transistor is connected to the Vin source. Besides, the source of the PMOS and the drain of the NMOS transistors are connected to the output terminals of the amplifier circuit. The biasing of the amplifier circuit helps to keep away the transistor from going into the saturation regime and to permit thesignals to obtain a larger gain.

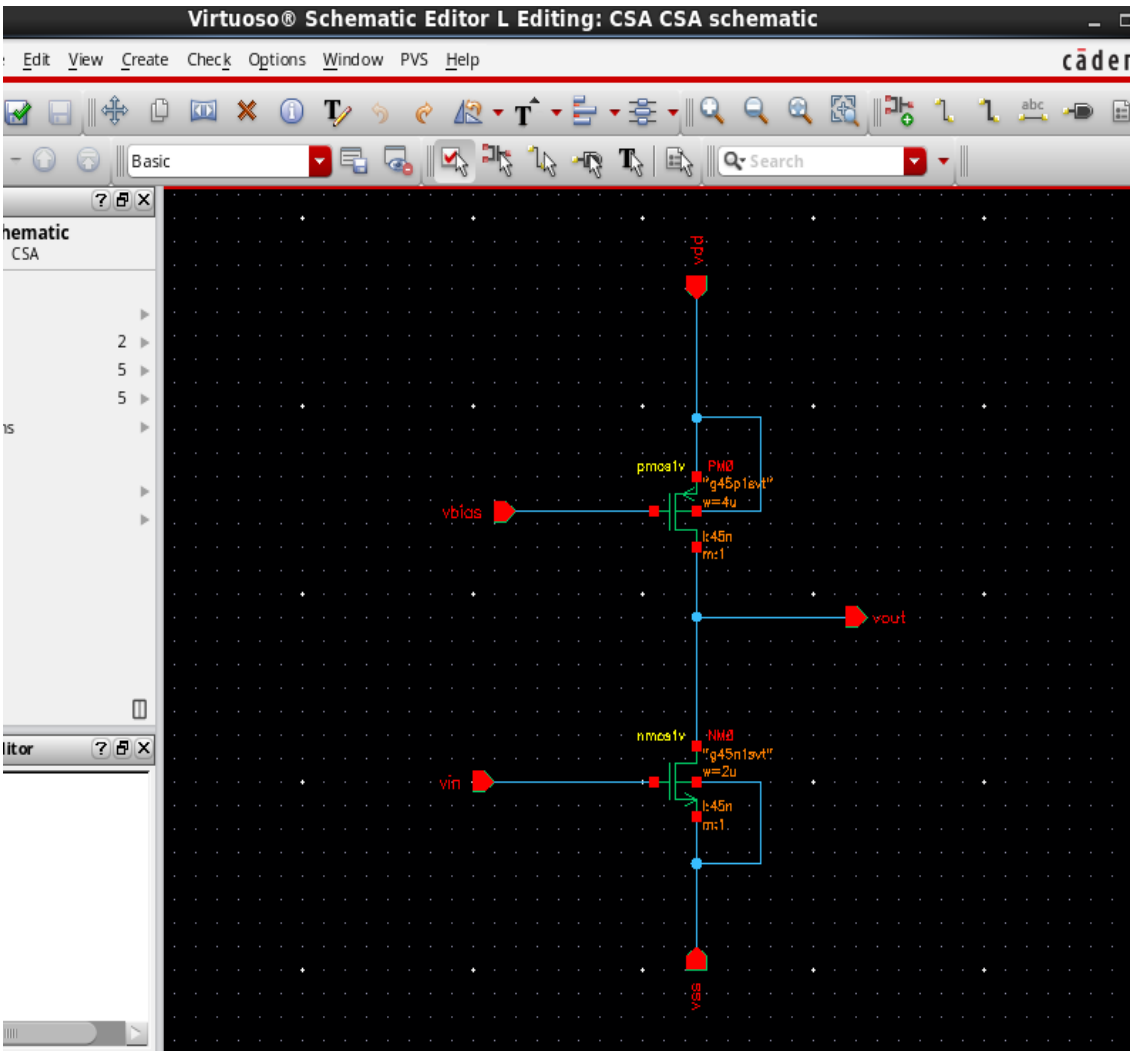

Figure 2. The detailed schematic circuit diagram of theCS amplifier circuit

To design the amplifier circuit with MOS transistors' length of 45 nm, we used the gpdk045 library and attached its technology file to our design library. After that, we opened the schematic window and inserted various components like transistors by creating various instances from various component libraries, pins, sources, ground, etc. from various libraries. We changed the parameter values and properties of them based on our design requirements shown in Table 1. Then we connected those using wires.

IV. Results and Discussions

To simulate the designed amplifier circuit, we used Analog Design Environment (ADE). We executed our analysis for a duration of 5 ms time to obtain the simulation results of the transient analysis for the input voltage of 5 mV peak at a frequency of 1 kHz. We obtain the output voltage of 1.8255 V peak after running the simulation. Therefore, the voltage gain (well-defined as the quotient of the output voltage to the input voltage on the same measurement scale) that we obtain through this simulation is approximately 365. It indicates how the amplifier circuit boosts the strength of an analog input signal.The transient analysis result is shown in Fig. 3.

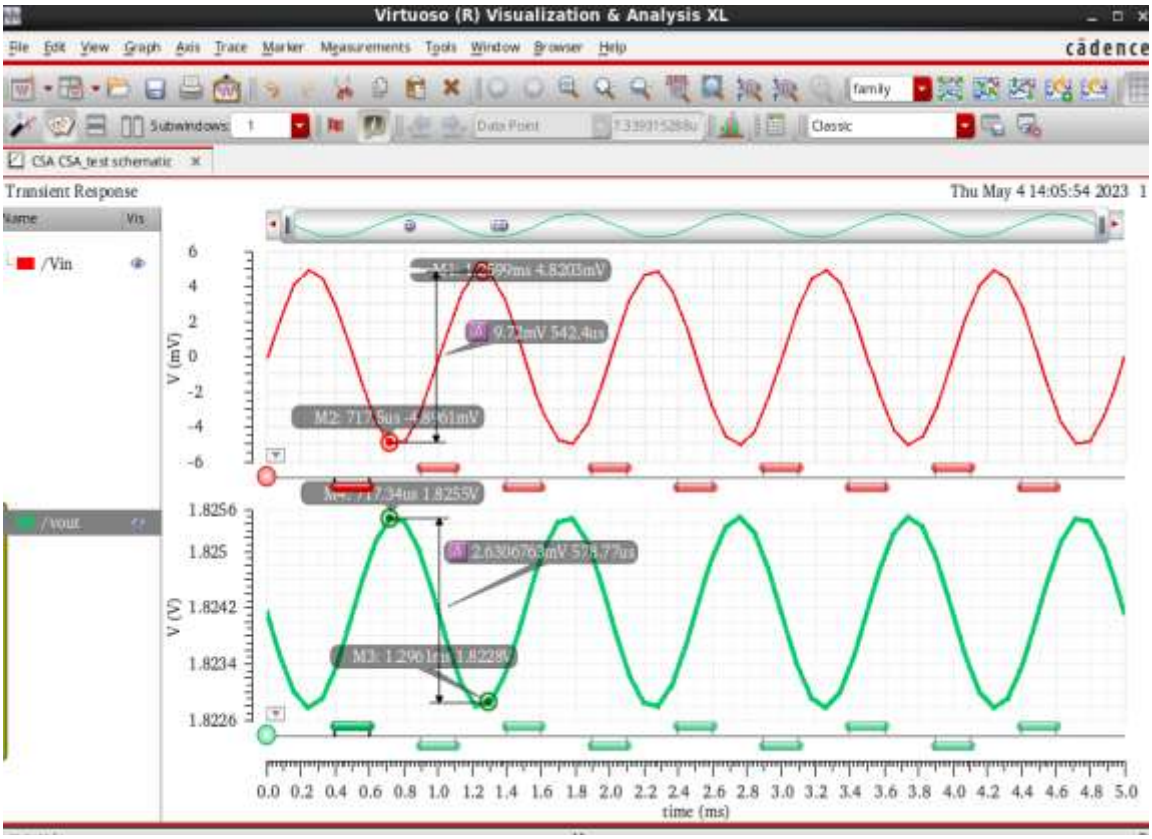

Figure 3. Simulated output voltage for an applied input voltage obtained by the transient response analysis

We also performed the DC analysis from -2.5 V V to +2.5 V, that is, to determine the output of the circuit when the input of the circuit goes from the OFF state to the ON state.The DC analysis result is shown in Fig. 4. Since the input voltage is connected to the input of the NMOS transistor, the output voltage decreases from 2.5 V to 1.5 V. The voltage is not exactly zero voltage when the input is completely turned ON, this is because of the body effect of the transistor.

We then performed the AC analysis. It gives the quantitative analysis of the output spectrum of a circuit or device in response to an input signal. It gives a measure of the magnitude (for example, the amplitude/gain in decibels) and the phase angle response concerning the frequency variation of the input signal.We chose the logarithmic scale on the frequency axis and the linear scale on the magnitude axis to display the results. For every decade, 10 points were taken. The result of AC analysis is shown in Fig. 5. We observe that for a constant input signal, the output voltage remains constant for a wide range of frequencies.

Similarly, the phase response of a circuit shows how the phase of the output signal changes as the input signal passes through the amplifier circuit with a varying frequency. In the phase response graph, the phase difference between input and output is 180^0 due to the storage elements present in the MOS transistors.

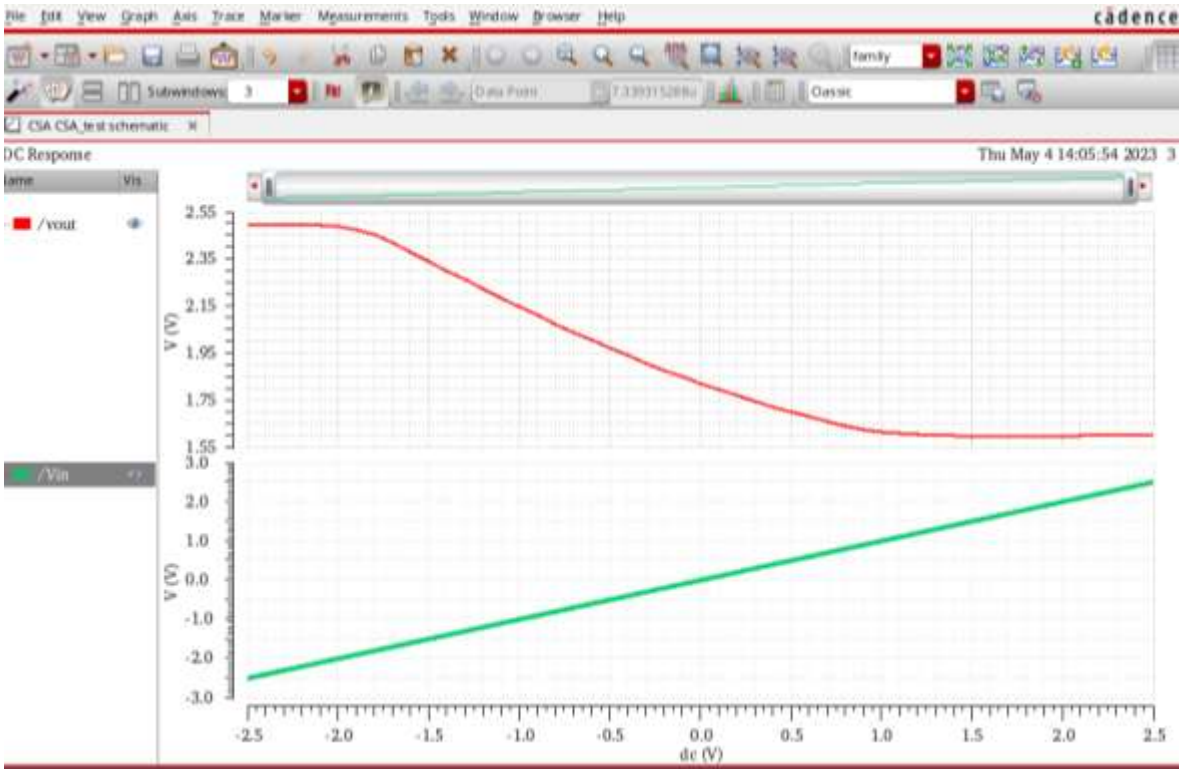

Figure 4. Simulated output voltage for an applied input voltage from 0 to 2.5 V obtained by the DC analysis

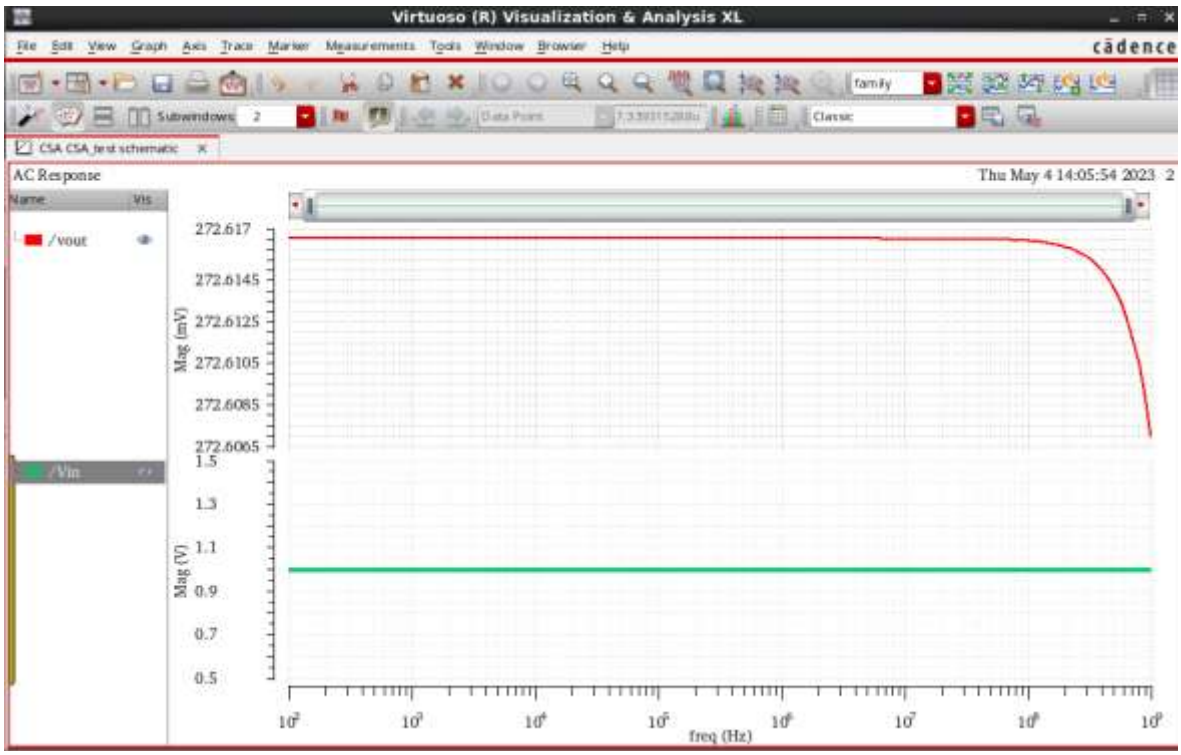

Figure 5. Simulation result of AC response analysis from 100 Hz to 1 GHz

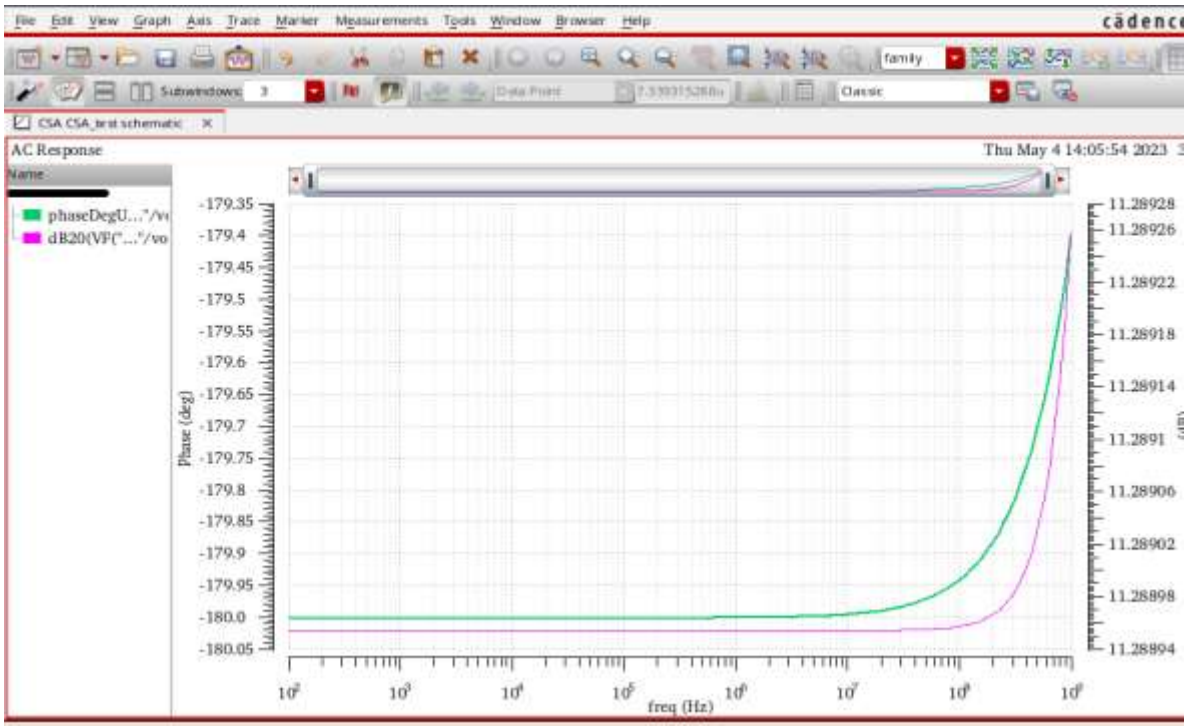

Figure 6. Simulation result of phase response analysis

V. Conclusions and Future Directions

In this design and investigative research paper, we designed, simulated, and analyzeda CMOS-based common source amplifier circuit using a 45 nm technology node in Cadence Virtuoso design and simulation tool. It provides high performance with a gain of 51.25dB, bandwidth of 400 MHz, and output phaseangle of -180^0. A common source amplifier circuit is crucial for electronic circuits and systems. It can be made inexpensively.However, before using a common source amplifier circuit, it is vital to take into account the limitations of the circuit-making parameters and the particular requirements of the application.

In the future, further analysis will be executedfor the same circuit with the latest technology node as well as for multiple stages at the same node. Besides, a comparison of the same circuit may be made for different technology nodes. Suchtypes of design and simulation tasksmay be helpful in teaching and learning the VLSI Circuit Design laboratorycourse works.

References

[1]. M.H.Bhuyan, "History and Evolution of CMOS Technology and its Application in Semiconductor Industry," Southeast University Journal of Science and Engineering (SEUJSE), ISSN: 1999-1630, vol. 11, no. 1, June 2017, pp. 28-42.

[2]. M. H. Bhuyan, "RF Semiconductor Devices Technology: History and Evolution, Prospects and Opportunities, Current and the Future," Southeast University Journal of Science and Engineering (SEUJSE), ISSN: 1999-1630, vol. 12, no. 2, December 2018, pp. 28-39.

[3]. M. H. Bhuyan, "Analytical Modeling of the Pocket Implanted Nano Scale n-MOSFETs," PhD Thesis, EEE Department, BUET, Dhaka, Bangladesh, 2011.

[4]. M. H. Bhuyan, F. Ferdous, and Q. D. M. Khosru, "A Threshold Voltage Model for sub-100 nm Pocket Implanted NMOSFET," Proceedings of the IEEEsponsoredInternational Conference on Electrical and Computer Engineering, Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh, 19-21 December 2006, pp. 522-525.

[5]. M. H. Bhuyan and Q. D. M. Khosru, "Low Frequency Drain Current Flicker Noise Model for Pocket Implanted Nano Scale n-MOSFET," Proceedings of the IEEE and EDS sponsored Nano Materials and Device Conference (NMDC), 12-15 October 2010, Monterey, CA, USA, pp. 295-299.

[6]. M. H. Bhuyan and Q. D. M. Khosru, "Linear Asymmetric Pocket Profile Based Low Frequency Drain Current Flicker Noise Model for Pocket Implanted Nano Scale n-MOSFET," Proceedings of the IEEE and EDS sponsored International Conference on Electrical Information and Communication Technology (EICT), Khulna University of Engineering and Technology (KUET), Khulna, Bangladesh, 13-15 February 2014, pp. 284-288.

[7]. M. H. Bhuyanand Q. D. M. Khosru, "An Analytical Subthreshold Drain Current Model for Pocket Implanted Nano Scale n-MOSFET," Journal of Electron Devices, France, 1682-3427, vol. 8, October 2010, pp. 263-267.

[8]. M. H. Bhuyan, F. Ferdous, and Q. D. M. Khosru, "Temperature Effects on Subthreshold Drain Current of Nano Scale Pocket Implanted n-MOSFET," Proceedings of the IEEE sponsoredInternational Conference on Electrical and Computer Engineering (ICECE), Bangladesh University of Engineering and Technology (BUET), Dhaka, 20-22 December 2012, pp. 599-602.

[9]. M. H. Bhuyan and Q. D. M. Khosru, "Inversion Layer Effective Mobility Model for Pocket Implanted Nano Scale n-MOSFET," International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering, ISSN: p:2010-376X, e:2010-3778, vol. 5, no. 1, 2011, pp. 1-8.

[10]. M. H. Bhuyan and Q. D. M. Khosru, "Linear Profile Based Analytical Surface Potential Model for Pocket Implanted Sub-100 nm n-MOSFET," Journal of Electron Devices, France, ISSN: 1682-3427, vol. 7, April 2010, pp 235-240.

[11]. M. H. Bhuyan and Q. D. M. Khosru, "An Analytical Surface Potential Model for Pocket Implanted Sub-100 nm n-MOSFET," Proceedings of the IEEE-sponsored International Conference on Electrical and Computer Engineering, Bangladesh University of Engineering and Technology (BUET), Dhaka, 20-22 December 2008, pp 442-446.

[12]. M. H. Bhuyan and Q. D. M. Khosru, "Effects of Temperature on Reverse Short Channel Effect in Pocket Implanted Sub-100 nm n-MOSFET," Journal of Materials Science and Engineering, USA, 1934-8959, vol. 4, no, 7, July 2010, pp. 18-23, DOI:10.17265/2161-6213/2010.07.004.

[13]. M. H. Bhuyan and Q. D. M. Khosru, "Temperature Effects on Threshold Voltage of the Pocket Implanted Fully Depleted Thin Film SOI n-MOSFET," Proceedings of the International Conference on Engineering Research, Innovation and Education (ICERIE) Shahjalal University of Science and Technology, Sylhet, Bangladesh, 11-13 January 2013, pp. 502-507.

[14]. S. L. Pinjare, G. Nithya, V. S. Nagaraja, and A. Sthuthi, "A Gm/Id Based Methodology for Designing Common Source Amplifier,"2nd IEEE sponsored International Conference on Micro-Electronics and Telecommunication Engineering (ICMETE), Ghaziabad, India, 20-21 September 2018, pp. 304-307, doi: 10.1109/ICMETE.2018.00073.

[15]. A. J. Rao,"Analog Front-End Design Using the gm/ID Method for a Pulse-Based Plasma Impedance Probe System,"Utah State University, USA, All graduate theses and dissertation, June 2010.

[16]. Cadence Tool: https://www.cadence.com/en_US/home.html, retrieved on 23 May 2023.

[17]. Y.Zhang, S. M.R. Hasan, "On the gm-boosted common source with source degeneration and its configuration as a transimpedance amplifier," International Journal of Circuit Theory and Applications, vol. 49, issue 5, May 2021,pp. 1390-1398, doi: https://doi.org/10.1002/cta.2972

[18]. H. A.Ayubi, N. Z. Rizvi, and P. K. Mishra "Memristor Modelling for Common Source Amplifier using 180 nm Technology," Journal of VLSI Design Tools and Technology, vol. 5, no. 3, 2015, pp. 45–54.

[19]. M. Rakshitha, U. S. Rakshitha, and R. Shreyas, "Two Stage CMOS Operational Amplifier Using Cadence 180 nm Technology," International Journal of Innovative Research in Science, Engineering, and Technology, Vol. 9, Issue 1, e-ISSN: 2319-8753, p-ISSN: 2347-6710, January 2020, pp. 12701-12706, DOI: 10.15680/IJIRSET.2020.0901002.

[20]. S. M. Aderao, Sushmakejgir, "Design of CMOS Multistage High Gain Differential Amplifier using Cadence," International Journal of Electrical, Electronics and Data Communication, vol. 6, issue 6, June 2018, p-ISSN: 2320-2084, e-ISSN: 2321-2950, pp. 50-53.