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Design And Analysis Of A 1.2V, 0.387 Mw High-Speed 4-Bit Current-Mode Flash ADC

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Abstract:
One of the main disadvantages of voltage-mode flash ADCs is their limited speed in real-time applications. Due to the charging and discharging of parasitic capacitances with the full voltage swing, the speed of the ADC is adversely affected. In current-mode flash ADCs, there is no need to charge and discharge parasitic capacitances because currents flow in closed loops. Therefore, current-mode flash ADCs are more suitable for high-speed real-time operation. Current-mode TIQ (Threshold Inverter Quantization) based comparators are gaining attention in flash analogue-to-digital converter (ADC) designs due to their high-speed operation and low power consumption. A current-mode TIQ comparator generates an internal quantization reference value, thereby eliminating the need for a resistive ladder. Since the quantization level depends on the inverter switching threshold voltage, which is highly sensitive to the transistor aspect ratio, the comparator is susceptible to process variations. To mitigate the effects of process variations, a Wilson current mirror is used instead of a simple current mirror in the TIQ comparator design. The Wilson current mirror employs negative feedback to generate more accurate reference current levels for quantization. The proposed 4-bit ADC consumes 0.38 mW of power and achieves a conversion time of 2.06 ns. The design operates with a 1.2 V power supply and is implemented using a 130 nm BSIM3 model. Simulations are carried out in LTspice, and Monte Carlo analysis is performed to evaluate the impact of process variations on the conversion speed of the current comparator.

Key Words: *Current-mode, Current-mode TIQ comparator with Wilson current mirror, Flash ADC, Low power design*

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I. Introduction

The data generated by the analogue front end must be converted into digital form for further processing. Due to this fact, the ADCs are the key part of recent data processing chips. The performance of applications like wearable electronics, biomedical and healthcare devices, and smartphones depends on the performance of ADC. As a result, there is a great demand for energy-efficient high conversion speed ADCs. Nowadays, current mode TIQ-based comparators (Threshold Inverter Quantization) are popularly used in analogue-to-digital converters (ADCs), especially in energy-efficient and high-speed applications [1-2]. As a separate resistive ladder is not required, the design becomes more energy efficient. When these comparators are implemented using current-mode design, they offer some advantages, such as high speed and better scalability in deep submicrometric technologies. However, there are several disadvantages or limitations associated with such as sensitivity to threshold voltage (V_{th}), device mismatch, etc. Since the comparator relies on the matching or predictable behaviour of MOS devices, PVT (Process, Voltage, and Temperature) variations can significantly affect the threshold levels and decision boundaries. This leads to non-uniform quantization levels. A detailed description of the proposed current comparator circuit is provided in Section 3. The current comparator is a vital part of the current-mode Flash ADC as it makes a comparison between the input current and the reference current. Based on the polarity of comparison, the output voltage is produced either at VDD or 0V. The output voltage of each comparator is a thermometer code, which is input to the encoder.

In this paper, a 15x4 encoder is designed using a mux-based configuration. The encoder's output is a binary code corresponding to the input. The fundamental block structure of the 4-bit Current-mode Flash ADC is shown in Fig. 1. It comprises 15 Wilson Current mirror-based TIQ Current-Mode comparators and a 15x4 thermometer to binary encoder.

This study is structured into several key sections. It begins with an introductory part laying the context and significance. The implemented design is simulated for conversion speed and power dissipation. The parametric variation is also performed on the design to see the effects on conversion speed and power

dissipation. The details of simulations and results are discussed in Section 4 of this paper. Section 5 concludes this paper.

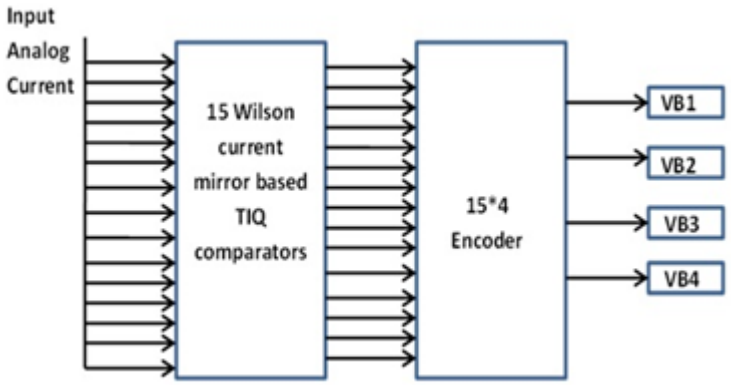

Fig. 1 Block diagram representation of 4-bit current-mode Flash ADC

II. Literature Review

The Current comparator is a fundamental building block for designing Flash ADC [3]. Their role involves comparing an input signal to a reference signal, producing a digital output indicating whether the input is higher or lower than the reference [3]. The demand for low-power and high-speed operation, particularly in portable and mobile devices, has driven significant research into optimizing CMOS current comparator design [3].

The authors in [4] presented a novel CMOS comparator that is inverter-based and contains low-power and high precision. A current-limiting circuit regulates the CMOS inverter's inherent high-power consumption. To optimize the comparator's gain before reaching a judgment, a current-modulation approach is suggested.

The authors in [5] introduced a flash ADC with a resolution of 12 bits and a sampling rate of 1.1 GS/s. This is a low-power and efficient architecture. The design employs a segmented structure comprising three sub-flash ADCs—SADC1, SADC2, and SADC3 are responsible for detecting the most significant, intermediate, and least significant bits, respectively. Specifically, SADC1 offers 1-bit, SADC2 provides 6-bit, and SADC3 provides 5-bit resolution, and their combined outputs, along with an encoder, generate the full 12-bit digital output.

In article [6], authors presented a dynamic current comparator that uses a parasitic charge recycling approach to attain an ultra-low energy per comparison of 175 FJ. Additionally, the comparative energy is further decreased to 55 FJ, which is more than three times lower, by adding a switched capacitor supply to the circuit's static section.

Sun et al. [7] investigated the impact of Negative Bias Temperature Instability (NBTI) ageing on a high-precision current comparator implemented in 16 nm FinFET technology. Their study shows how ageing effects lead to threshold voltage shifts and increased propagation delay, ultimately degrading comparator performance over time. The authors also proposed effective detection and mitigation techniques to reduce the impact of NBTI and improve long-term reliability. However, the work primarily focuses on reliability aspects without emphasizing power optimization and design efficiency in comparator circuits. Therefore, there is a need to develop comparator architectures that not only address ageing effects but also achieve low-power and high-speed performance, which is the focus of this work.

In article [8], the study presents an ultra-low power current comparator designed for low to medium frequency applications with a strict power budget. The circuit significantly lowers power dissipation through the use of diode-connected transistors and feedback. The suggested current comparator's overall power-delay product, or Figure of Merit (FoM), is therefore superior to that of the existing current comparators.

In [9], the authors presented the design of a low-power, high-speed current comparator-based analogue-to-digital converter (ADC). The proposed circuit incorporates a current conveyor as a key component of the comparator and demonstrates efficient performance. It achieves a low power consumption of 158 μW at an input current of 0.1 mA and an extremely small propagation delay of 0.4 ns. The analysis also reveals that the ADC exhibits low power dissipation and high accuracy.

In [10], the authors used a power-gating technique to implement a low-power, high-speed, high-resolution flash ADC.

The project presented in [11] implemented a 4-bit thermometer-coded ADC. This architecture uses a resistive ladder network to generate a reference voltage for comparison. The design uses a fully parallel architecture.

Although prior works have significantly improved comparator performance, limitations in power consumption and scalability remain, motivating the proposed approach in this study.

III. Wilson Current Mirror-Based TIQ Comparator

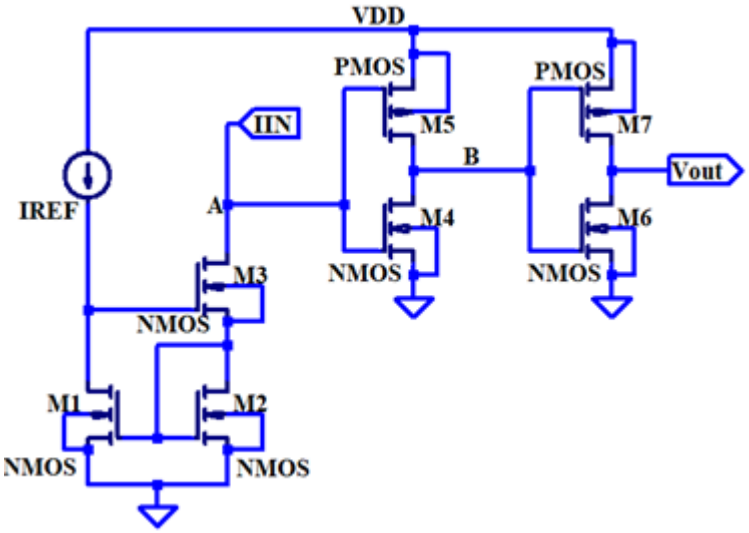

Fig. 2 Circuit diagram of CMOS TIQ Current Comparator Based on Wilson Current Mirror Configuration

The Wilson current mirror in the TIQ current comparator plays a crucial role in maintaining a stable voltage at node A (VA), despite variations in supply voltage or temperature. When VA tends to increase, it causes the drain current of transistor M3 to rise, which in turn increases the current through M2. Since M1 and M2 share the same gate-source voltage, the current in M1 also increases. However, because the reference current (I_{ref}) is fixed, this imbalance triggers a feedback mechanism that reduces the gate voltage of M3, thereby decreasing its current. This negative feedback action brings VA back to its original level, effectively stabilising it. As a result, the Wilson current mirror ensures that VA remains approximately constant, typically around half of the supply voltage (VDD/2) when input current equals reference current.

The comparator operation is based on detecting deviations between the input current (I_{in}) and the reference current (I_{ref}) at node A. According to Kirchhoff's Current Law, any difference between these currents causes a corresponding change in VA. This voltage is then fed into an inverter formed by transistors M4 (NMOS) and M5 (PMOS), which amplifies the variation. If I_{in} exceeds I_{ref}, VA rises above VDD/2, causing the inverter output (VB) to go low. Conversely, if I_{in} is less than I_{ref}, VA drops below VDD/2, and the inverter output goes high. In this way, the circuit effectively converts a small current difference into a clear digital output, with all transistors operating in the saturation region for improved accuracy and performance.

A. Design of Encoder

The second block of Figure 1 is the encoder. In this paper, the output of comparators is thermometer code, and thermometer code is used as input in encoders. In this work, the thermometer code is first translated to gray code, which is subsequently converted to binary code. The reason behind that, in regular binary systems, multiple bits might change simultaneously, which can lead to errors during the transition between values (for example, from 011 to 100).

In Gray code, only one-bit flips at a time, ensuring a smoother and more error-resistant transition between consecutive values. Figure 3 shows a functional block diagram of a 15*4 thermometer to gray code encoder. The output of current comparators is thermometer code (T1 to T15). Only gray-colored multiplexers are operational in this case when logic zero is present in the LSB bits T1–T7 [12]. T8–T15 function as inputs when the T8 signal becomes logic one [12]. This is a unique feature of this design. Its Boolean equations are given as follows [12].

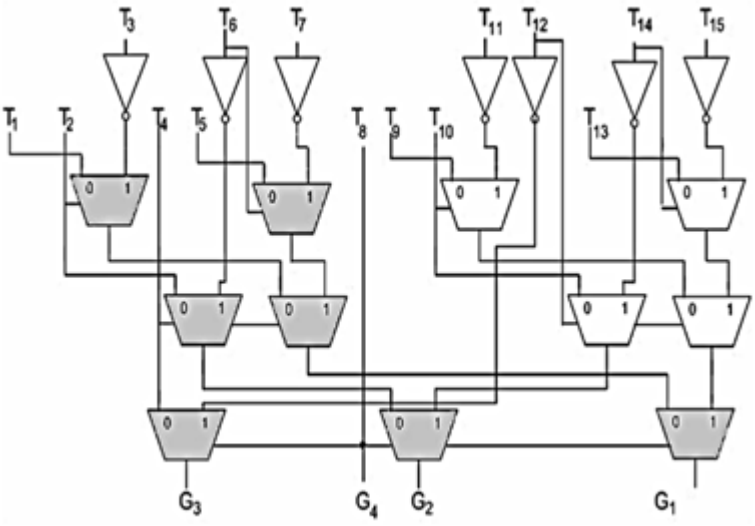

Fig. 3 15*4 thermometer to gray code encoder [12]

$G_4 = T_8$ (1)

$G_3 = T_8 \text{'} T_4 + T_8 T_{12}\text{'}$ (2)

$G_2 = T_8 \text{'} (T_4 \text{'} T_2 + T_4 T_6 \text{'}) + T_8 (T_{12} \text{'} T_{10} + T_{12} T_{14} \text{'})$ (3)

$G_1 = T_8 \text{'} [T_4 \text{'} (T_2 \text{'} T_1 + T_2 T_3 \text{'}) + T_4 (T_6 \text{'} T_5 + T_6 T_7 \text{'})] + T_8 [T_{12} \text{'} (T_{10} \text{'} T_9 + T_{10} T_{11} \text{'}) + T_{12} (T_{14} \text{'} T_{13} + T_{14} T_{15} \text{'})]$ (4)

IV. Results And Discussion

Simulations are carried out using the Predictive Technology Model (PTM) 130nm BSIM3 technology at a supply voltage of 1.2V, leveraging the LTspice simulation environment. The sizing of the transistors of Figure 2 is given in Table 1. Here, I_{ref} is chosen to be 15µA.

Table no 1. Sizing of Wilson's current mirror-based TIQ current comparator

Transistor	Width(µm)	Length(µm)
M1(NMOS)	2.72	0.13
M2(NMOS)	3.69	0.13
M3(NMOS)	1.95	0.13
M4(NMOS)	3.36	0.26
M5(PMOS)	3.58	0.26
M6(NMOS)	3.23	0.26
M7(PMOS)	3.71	0.26

To obtain the graph of Figure 4, a 16µA peak-to-peak square input is applied to the proposed comparator, producing a 1.2 V peak-to-peak square output voltage. The graph plots time (or propagation delay) on the X-axis and input/output on the Y-axis. The propagation delay is measured as the time difference between corresponding input and output edges. It represents the time taken by the comparator to respond due to internal switching and capacitance effects. The propagation delay achieved is 1.89ns. The graph of Figure 5 shows power dissipation in µW versus time in ns for a proposed comparator. It exhibits a periodic waveform with a steady baseline around -20 to -40µW, showing static power dissipation due to bias current and leakage. In addition, sharp negative spikes up to -98µW appear due to dynamic power dissipation caused by switching activity in the circuit. After each negative spike, the power quickly returns to a steady level, showing fast circuit recovery.

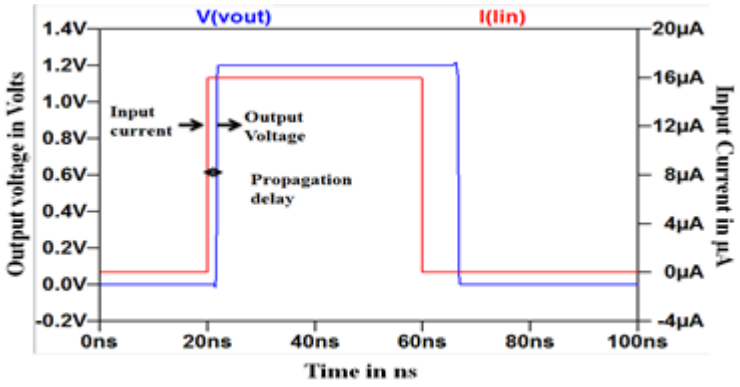

Fig. 4: Simulation output of the propagation delay between i/p current and o/p voltage of the Wilson current mirror-based TIQ-based current-mode comparator when I_{in}=16µA and I_{ref}=15µA

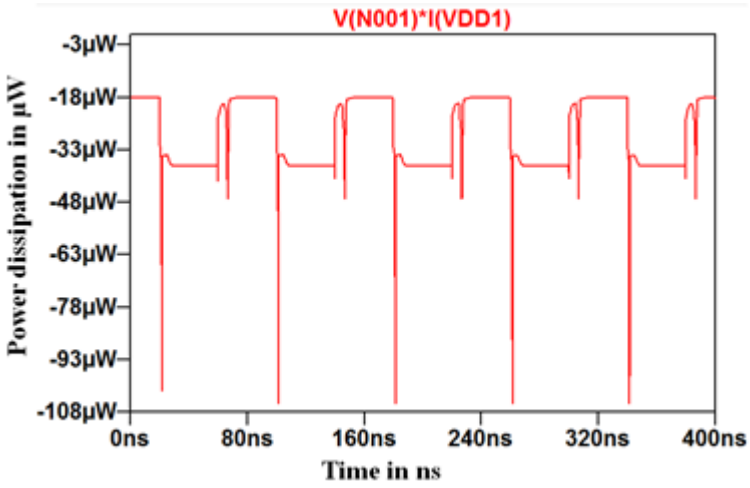

Fig. 5: Total power dissipation of the Wilson current mirror-based TIQ current comparator

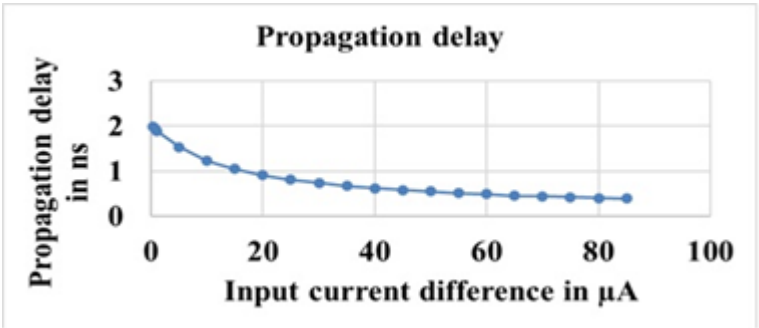

Fig. 6: Variation of propagation delay concerning input current difference

The sensitivity of a current comparator is the minimum change in input current required to switch the output and is given by ΔI_{min}. It is determined by the smallest difference between the input and reference current that the comparator can detect. Here, the input signal current is 15.3 µA, and the input reference current is 15 µA, giving ΔI_{min} 0.3 µA. Therefore, the sensitivity/resolution of the proposed comparator is 0.3 µA.

The impact of changes in current difference on both delay and power dissipation has been analyzed, and the corresponding simulation results are presented in Figures 6 and 7. The charts of Figs. 6 and 7 confirm that the increase in input current differences results in a decrease in propagation delay and an increase in power dissipation.

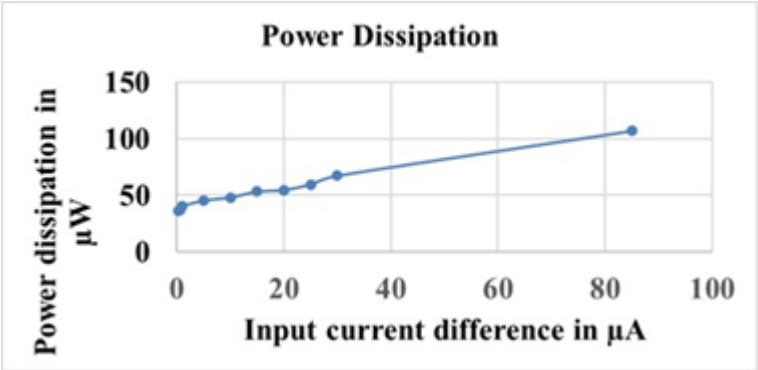

Fig. 7: Variation in power dissipation regarding the input current difference

Various performance metrics of Wilson's current mirror-based TIQ Current Mode comparator are assessed and presented in Table 2.

Table no. 2: Specifications of Wilson's current mirror-based TIQ current comparator

Parameters	Simulated Values
Technology	130nm
Supply Voltage	1.2V
Architecture	Wilson Current mirror-based TIQ CC
Biasing current	15µA
Input current	16µA
Propagation Delay	1.89ns
Power consumption	37.33µW

The robustness of the proposed Wilson current mirror-based TIQ comparator was evaluated using Monte Carlo simulations for 909 runs by incorporating process, voltage, and temperature (PVT) variations. A ±10% variation was introduced in key parameters, including supply voltage (VDD), threshold voltage (V_{th}), and transistor width (W), to account for process uncertainties and mismatch effects. Furthermore, the temperature was swept from −30°C to 150°C to analyze thermal sensitivity. The simulation results demonstrate that the proposed design exhibits reliable and stable performance across all considered variations.

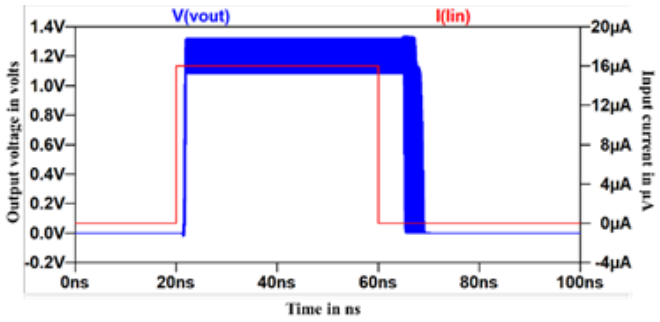

Fig. 8: Monte-Carlo simulation for 909 runs for the proposed comparator

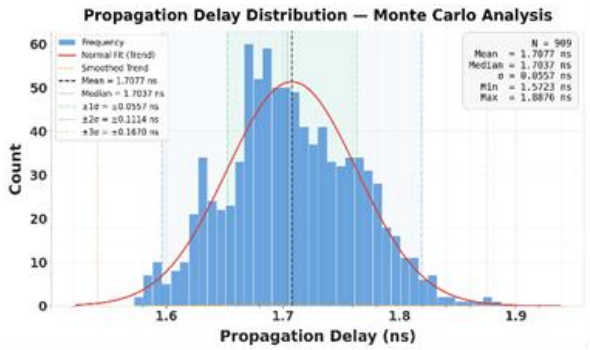

Fig.9: Histogram of the propagation delay of the proposed comparator

Table 3 shows the results of the histogram.

Table No.3 Result of Monte Carlo Analysis

Parameters	Value
Input Current Difference	16μA-15μA=1μA
Mean Value	1.7077ns
Median Value	1.7037ns
σ (Standard deviation)	0.0557ns
Min value	1.5723ns
Max value	1.8876ns

The Monte Carlo simulation results of the proposed comparator are illustrated through the histogram of propagation delay. The distribution shows a mean delay of 1.7077 ns and a median value of 1.7037 ns, indicating a nearly symmetric distribution with minimal skew. The standard deviation (σ) of 0.0557 ns reflects a small spread in delay values, demonstrating low sensitivity to process variations.

The delay varies from a minimum of 1.5723 ns to a maximum of 1.8876 ns, confirming that the performance remains within a tight range under ±10% variations in VDD, Vth, transistor width, and temperature conditions from −30°C to 150°C. The narrow distribution and close agreement between mean and median indicate that the proposed comparator exhibits strong robustness and reliability against process, voltage, and temperature (PVT) variations.

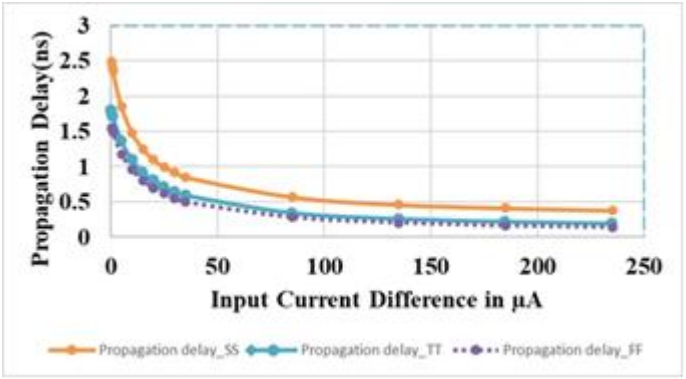

Fig. 10: PVT Variation effect on propagation delay of comparator

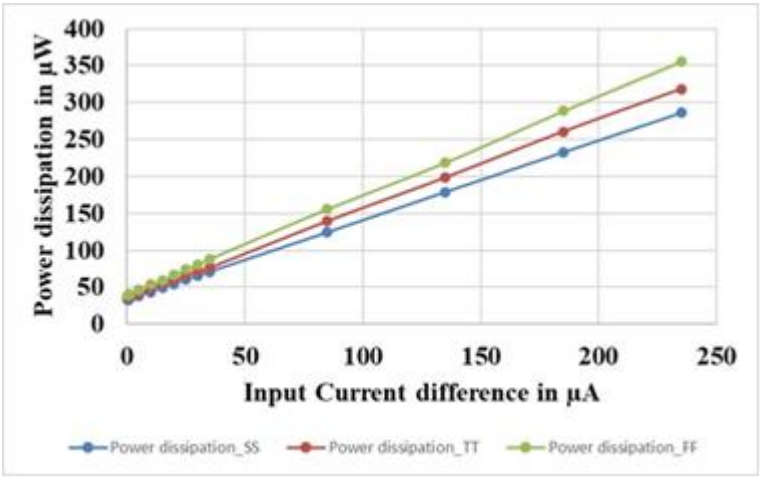

Fig. 11: PVT Variation effect on Power Dissipation of the comparator

The performance metrics, including propagation delay and power dissipation, are evaluated across a range of PVT (Process, Voltage, Temperature) corners. The simulations consider three process conditions (FF, SS, and TT), three supply voltage levels (1.32 V, 1.08 V, and 1.2 V), and three temperature settings (−30°C, 27°C, and 150°C). Figures 10 and 11 illustrate the simulation results corresponding to temperatures of −30°C, 27°C, and 150°C, respectively.

From figures 10 and 11, it is observed that the FF corner exhibits the highest power dissipation due to faster charging and discharging of parasitic capacitances, along with lower propagation delay compared to TT and SS corners. Conversely, the SS corner has maximum propagation delay and lowest power dissipation.

A. 4-bit Flash ADC using proposed comparator:

A four-bit Current-Mode Flash ADC has been designed utilising a Wilson current mirror-based TIQ current comparator along with a 15x4 encoder. The design incorporates a total of 15 Wilson current mirror-based TIQ current comparators, each assigned a reference current ranging from 1µA to 15µA as per below given formula. The reference current of the i^{th} comparator is,

$$I_{ref}i = (\text{Input Current Range}) * i /(2^n-1) \quad (5)$$

Where i is the no of comparator, the input current range is 15 µA, n is the total no of bits. In our case, the value of n is 4. The input current applied to the system is a ramp signal ranging from 0 to 16µA. This configuration allows for efficient comparison and encoding of the input current, converting it into a digital output corresponding to the closest reference value. The simulation results for this design, including the performance and output of the ADC, are presented in Figure 12, demonstrating its functionality and efficiency.

Here, the total conversion time T_{conv} of one sample of this ADC is 2.0625ns. Therefore, the sampling rate of this ADC is 0.484GSPS.

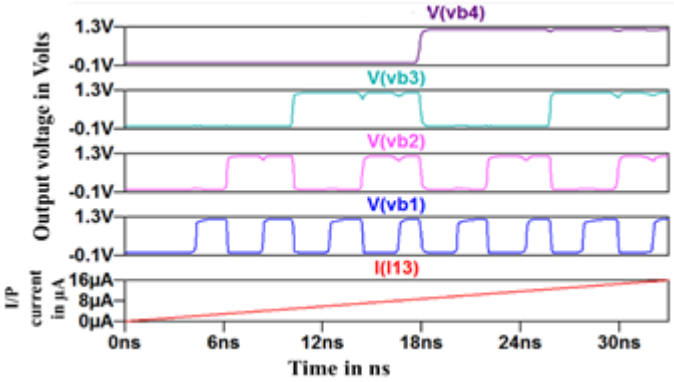

Fig. 12: Simulation output of 4-bit current-mode flash ADC

The variation between the actual width of the code and the ideal width of the code is quantified by Differential Nonlinearity (DNL), which indicates how much the code width deviates from its ideal value. On the other hand, Integral Nonlinearity (INL) is defined as the variation between the actual height of the code and the ideal height of the code, reflecting the cumulative error over the entire conversion range. To evaluate the linearity of the designed 4-bit Current-Mode Flash ADC, both DNL and INL are plotted using MATLAB. The results are shown in Figure 13, where the DNL and INL are calculated using two different methods: the Best Fit method and the Endpoint method.

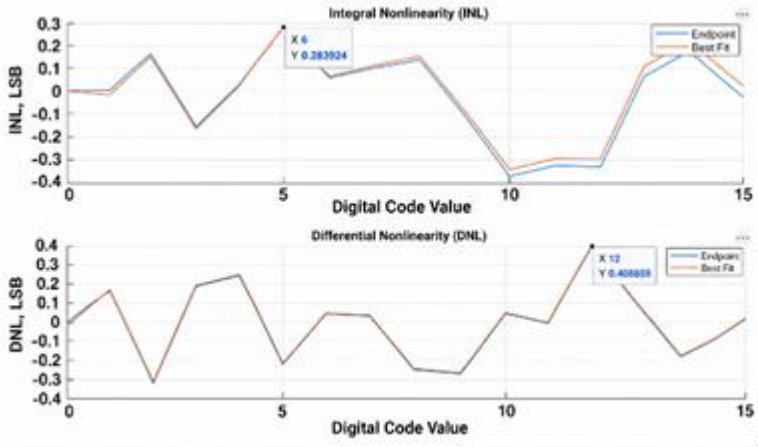

Fig. 13: INL and DNL characteristics of the proposed current-mode flash ADC

The value of Integral Nonlinearity (INL) is calculated to be 0.2839 LSB, while the value of Differential Nonlinearity (DNL) is found to be 0.4088 LSB by the Endpoint method, as shown in Figure 13.

To further evaluate the ADC's performance, a sine wave input with an amplitude of ±16uA and a frequency of 50MHz is applied. The resulting waveform, which demonstrates the system's response to this input, is presented in Figure 14. This helps illustrate the ADC's accuracy and behaviour under dynamic conditions.

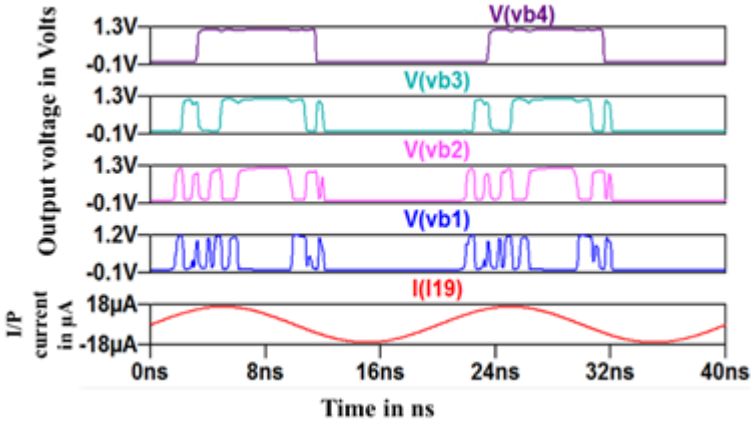

Fig.14: Simulation result of a 4-bit current-mode flash ADC using a sine wave input at 50MHz input frequency

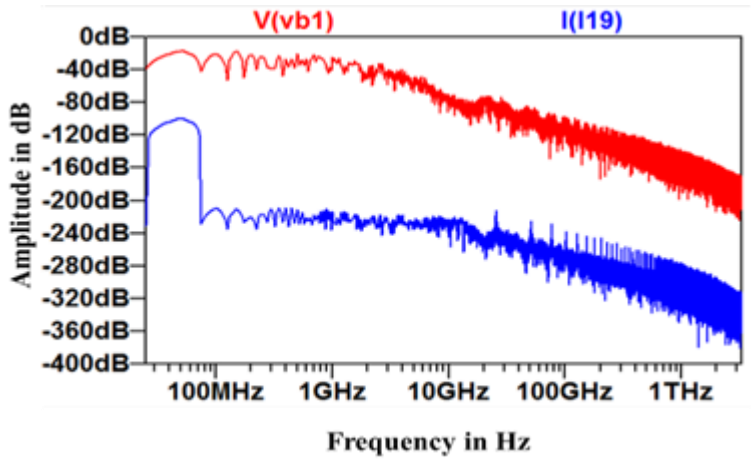

Fig. 15 FFT response at 50MHz input frequency

Figure 15 displays the Fast Fourier Transform (FFT) response of the ADC when a 50MHz input frequency is applied. This analysis helps visualize the frequency domain characteristics and performance of the ADC, highlighting any distortion or noise present in the output signal. From the FFT response shown in Figure 15, it is observed that the Signal-to-Noise Ratio (SNR) of the ADC is 23.67 dB. The Effective Number of Bits (ENOB) is an important parameter that quantifies the resolution of the ADC, and it can be calculated using the formula:

$$ENOB = (SNR - 1.76)/6.02 \quad (6)$$

Using this formula, the ENOB at a 50MHz input frequency is determined to be 3.64 bits. This value indicates the effective resolution of the ADC, accounting for both the quantization error and the noise present in the system. Finally, the power consumption of the entire system is the sum of the power consumed by the comparator array and the encoder. Total power consumed by the comparator array is 387 µW, and total power consumed by the encoder is 2.043nW. Therefore, the addition of both power consumptions is calculated to be 0.387mW, demonstrating the design's energy efficiency.

Table 4 provides a comprehensive summary of all relevant design parameters, including the SNR, ENOB, power consumption, and other key performance metrics, offering a complete overview of the ADC's performance and suitability for its intended applications.

Table 4. Performance parameters of 4-bit TIQ-based Current-Mode Flash ADC

Parameters	Simulated Value
Technology	130nm
Supply Voltage	1.2V
Resolution	4 bit
Sampling Rate	0.484 GSPS
Input current Range	1-15µA
Power Consumption	387µW
INL	0.2839 LSB
DNL	0.4088 LSB
SNR	23.67dB
ENOB	3.64bits@0.484GS/s (fin=50MHz)

The performance of the proposed flash ADC is verified under process, voltage, and temperature (PVT) variations. The supply voltage is varied by ±10% from its nominal value (1.2V), and the temperature is swept across −30°C, 27°C, and 150°C. In addition, extreme process corners FF and SS are considered to evaluate the robustness of the design. The simulation results show that the ADC produces correct and stable output waveforms under all PVT conditions, demonstrating reliable operation across a wide range of variations.

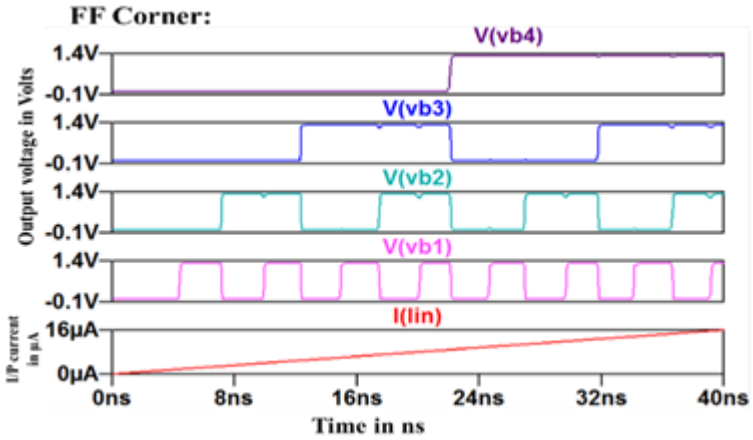

Fig. 16 FF Corner Response of proposed flash ADC

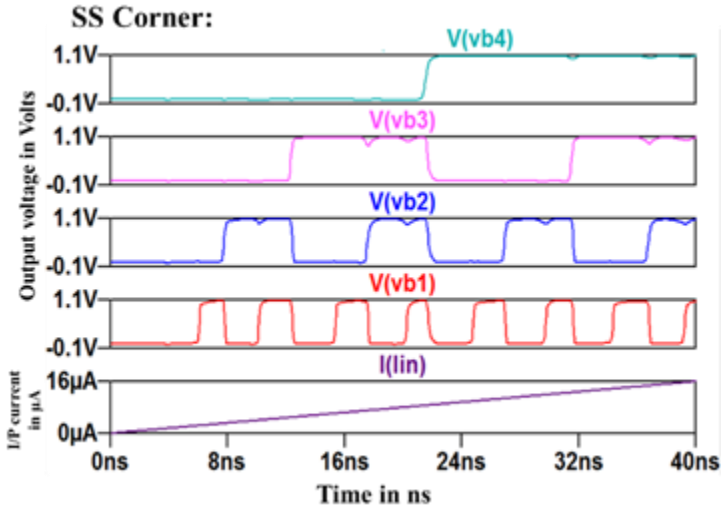

Fig. 17: SS Corner Response of proposed flash ADC

Table 5. Comparison table of different current-mode flash ADC

	[13]	[14]	[15]	Our work
Published Year	2016	2020	2025	
Technology	0.18 µm	0.18 µm	0.18 µm	0.13 µm
Supply Voltage	1 V	1.8V	0.8V	1.2V
Resolution	4 bits	4 bits	4 bits	4 bits
Sampling Rate	up to 3.33 GHz	--------	Up to 100MHz	Up to 0.484GSPS
Input Range	---	---------	1.2Vp-p	0-15 µA
Power consumption	1.3mW	2.14mW	0.059mW	387µW
DNL	-0.2LSB-O.1LSB (@3.3GS/s)	< 0.4 LSB	------	0.4088 LSB
INL	-0.2LSB - 0.12LSB (@3.3GS/s)	< 0.5 LSB	-------	0.2839 LSB
ENOB	------	3.6	------	3.64 bits @0.484GS/s

V. Conclusion

In this paper, the design of a 4-bit current-mode Flash ADC is presented using a novel design of Wilson Current Mirror-based TIQ comparator. The proposed design offers 0.387mW power with a conversion speed of 2.0625ns. Here, the sensitivity against process variation of the TIQ comparator is improved by maintaining a constant drain voltage of the M3 transistor using the negative current feedback. The power dissipation is reduced by taking a smaller quantization value of the order of 1 µA range. To improve the non-linearity error, the quantization level can be reduced further, or quantization level can be varied dynamically from LSB to MSB from 1µA to 0.25µA. For a 50MHz input frequency signal, ENOB is achieved at 3.64 bits. As we increased input frequency, the ENOB value decreased. Proposed comparator functionality is verified at extreme processing corners. This architecture is compared with other architectures from the literature to provide benchmarking.

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