

Design and FPGA Performance Evaluation of an 8-Bit Ordinary Truncated Multiplier for Approximate Computing

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Abstract—Approximate multiplication can reduce logic and switching activity in error-tolerant signal-processing and machine-learning hardware. This work presents a FPGA comparison of an 8-bit unsigned exact multiplier and an ordinary column-truncated multiplier in which partial products with $i+j < \text{CUT}$ are omitted, with $\text{CUT}=6$. Both architectures are evaluated on an Avnet ZedBoard (XC7Z020-CLG484-1) using Xilinx Vivado 2019.2 with common timing constraints, and synthesis with DSP inference disabled. Post-route measurements are reported over target clock frequencies from 100 to 190 MHz for both architectures, with an additional 200-MHz point for the truncated design. At the highest common 190-MHz target, truncation reduces critical delay from 5.19 to 5.08 ns, increases estimated F_{max} from 192.86 to 196.93 MHz, reduces dynamic power from 0.027 to 0.020 W, reduces LUT utilization from 82 to 65, lowers dynamic-power PDP from 0.1401 to 0.1016 nJ, and reduces LUT-based ADP from 425.58 to 330.20 LUT-ns. These correspond to improvements of 2.12% in delay, 2.11% in F_{max} , 25.93% in dynamic power, 20.73% in LUT count, 27.48% in PDP, and 22.41% in ADP. The observed results show a reliable FPGA hardware-efficiency reference point for successive improved truncated-multiplier designs.

Index Terms—approximate computing, FPGA, truncated multiplier, partial-product truncation, dynamic power, power-delay product, area-delay product.

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I. INTRODUCTION

The arithmetic operations are a supreme requirements in digital signal processing (DSP), image processing, computer vision, and machine-learning accelerators. The multiplication performed by conventional exact multipliers maintain the every partial product term and therefore it gives promise for arithmetic reliability, but the correspondingly the use of the reduction tree, carry propagation, and switching activity become significant contributors to overheads for logic cost and energy. The approximate computing make use of the error tolerance of selected applications in the design and modeling that further relaxing arithmetic computing exactness and enhance the hardware efficiency [1]. Therefore, a practical approximate multiplier may be evaluated for both the numerical-error measures and hardware realization standards for frequency, delay, power and area, delay, and area.

Truncation is one of the shortest approximation mechanisms due to its ability to eliminate partial products which are not so crucial instead of replacing the entire multiplication algorithm. The unsigned array representation has the contribution of a partial product $A_i B_j$ which is weighted by 2^{i+j} . The elimination of terms below a selected column boundary minimizes a region of logic that take part in accumulation and has the ability to minimize switching activity. The trade-off sounds sure underestimation because all rejected terms are nonnegative. Prior work has therefore, explored constant and variable correction, partial-product perforation, operand rounding, and scalable truncation-and-rounding structures to improve accuracy in the process of retaining hardware optimizations [3]–[8].

FPGA evaluation of approximate multipliers requires particular care. The approximate multipliers require close attention during the process of FPGA evaluation. A dedicated DSP48 block may be utilized for an exact multiplication operator, whereas LUTs and carry chains may be specially utilized for a custom truncated structure. So a formal direct comparison may become false unless a proper controlled mapping is not being done. The constraints also controls timing results: the change for lower the value of the target period leads to change in

placement and routing, so maximum operating frequency cannot be characterized by merely a single unconstrained delay estimation. The main contributing factors like clock rate, switching activity, device, implementation, and analysis assumptions controls power estimations and comparisons.

This paper deals with the mentioned issues through a controlled comparison of an 8-bit exact multiplier with an ordinary column-truncated multiplier on the XC7Z020-CLG484-1 device. The same registered input/output wrapper, synthesis and implementation strategies, and timing methodology are utilized in both designs, where DSP inference is disabled to provide a fabric-oriented comparison. The demonstrated results measured post-route WNS, critical delay, estimated Fmax, static, dynamic and total power, LUT utilization, flip-flops, I/Os, power-delay product (PDP), and LUT-based area-delay product (ADP). The contribution in this work is a reproducible hardware-performance baseline rather assert to the improvement in truncation process itself.

II. RELATED WORK

The research on approximate multiplier enhancement techniques covers the algorithm-, architecture- and circuit- level evaluation and executions. Momeni et al. by introducing bounded arithmetic error have recommended approximate 4:2 compressors and gave the explanation for how a simplifying reduction-tree cells can optimize the hardware cost [2]. This simplified compressor-based mechanism improve the internal accumulation network instead of eliminating a contiguous part of low-significance.

A truncated multipliers have an established rating over others. Petra et al. succeeded to devise a truncated binary multiplier has variable correction to minimize mean-square error [3]. Garofalo et al. in due course obtained analytical maximum-error results in case of a same category multiplier [4]. The investigative studies express that truncation method should be described by an explicit description how a system separate valuable data from a data; that is no longer needed and, whenever compensation technique is used in the mathematically proved correction rule. It is also expressed that the error data depend on the truncation boundary and operand distribution.

Other approximate-multiplication strategies reduce operand or partial-product complexity in different ways. DRUM retains a limited dynamic range around the leading one to obtain an approximately unbiased result [5]. Partial-product perforation selectively suppresses product terms and provides analytical error bounds [6]. RoBA simplifies multiplication by rounding operands to powers of two [7], whereas TOSAM combines truncation and rounding in a scalable architecture [8]. EvoApprox8b provides a library and common error metrics for reproducible comparison of approximate arithmetic circuits [9]. Application-oriented studies have further shown that circuit-level error measures should be complemented by task-level metrics when approximate multipliers are used in image or video processing [10], [11].

The present work focuses on ordinary column truncation as a transparent baseline. Unlike compensated structures, no correction term is introduced; consequently, the hardware effect of removing the low-weight region can be observed directly. The emphasis is on a fair FPGA methodology and on dimensionally consistent composite metrics. The threshold baseline is important because afterwards compensation logic may be compared against both the exact multiplier and the simplest uncorrected truncated implementation using a standard set-up.

III. ARCHITECTURE

A. Exact Unsigned Multiplication

For unsigned N-bit operands A and B, the exact 2N-bit product is the weighted sum of N^2 one-bit partial products:

$$P = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} A_i B_j 2^{(i+j)}. \quad (1)$$

There are 64 terms in the complete partial-product matrix in the experimentally evaluated 8x8 multiplier. The exact reference result has contribution from all terms.

B. Ordinary Column-Truncated Multiplier

The first retained product column is denoted by CUT.

In the case of an ordinary truncated multiplier, it scarp every partial product term satisfying the condition $i+j < \text{CUT}$ and pass and utilized further all terms satisfying $i+j \geq \text{CUT}$. In this work $N=8$ and $\text{CUT}=6$. The retained and discarded components are:

$$Q_{\text{CUT}}(A,B) = \sum_{i+j \geq \text{CUT}} A_i B_j 2^{(i+j)} \quad (2)$$

$$D_{\text{CUT}}(A,B) = \sum_{i+j < \text{CUT}} A_i B_j 2^{(i+j)} \quad (3)$$

The approximate output and signed approximation error are therefore

$$\hat{P}_{\text{OT}} = Q_{\text{CUT}}, \quad e_{\text{OT}} = \hat{P}_{\text{OT}} - P = -D_{\text{CUT}} \quad (4)$$

Due to nonnegative value of D_CUT , the ordinary truncation is negatively biased and/or it is exact for every unsigned input pair. For a special case, $N=8$ and $CUT=6$, 21 partial-product terms out of the 64 has been discarded, it is a nominal removal of 32.8% of the one-bit partial-product terms before synthesis. The expected reduction of final LUT count is not equal to this percentage exactly as FPGA synthesis process itself restructures Boolean logic and carry chains again.

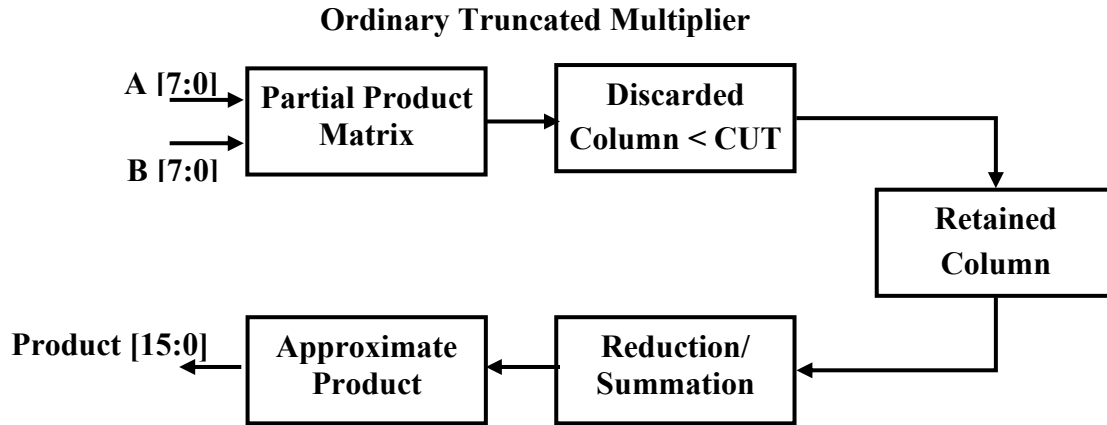


Fig. 1. Functional organization of the ordinary column-truncated multiplier.

C. Common Registered Wrapper and Mapping Control

Both multiplier cores are placed inside the same registered wrapper: input flip-flops capture A and B, the selected multiplier core forms the combinational stage, and output flip-flops capture the product. This structure creates a common register-to-register timing path and prevents interface differences from dominating the comparison. The exact and truncated cores are therefore evaluated under the same sequential boundary conditions.

To avoid an asymmetric comparison in which the exact $A \times B$ operator is mapped to dedicated DSP48E1 resources while the truncated architecture remains in programmable logic, DSP inference is disabled for the benchmark.

IV. EVALUATION METHODOLOGY

A. FPGA Platform and Timing Procedure

The designs were synthesized and implemented in Xilinx Vivado 2019.2 for the Avnet ZedBoard device XC7Z020-CLG484-1. The physical programmable-logic oscillator is 100 MHz; higher clock constraints in this study are used as timing-closure targets to characterize the implemented logic rather than as a claim that the fixed board oscillator itself operates at those frequencies. The exact design was evaluated at target frequencies of 100, 133, 166, 181, and 190 MHz. The ordinary truncated design was evaluated at the same five common targets and additionally at 200 MHz.

For each implemented design point, WNS is obtained from the post-route timing summary. For the common registered single-clock path used here, an engineering estimate of the critical delay is

$$T_{\text{critical}} \approx T_{\text{target}} - \text{WNS} \quad (5)$$

and the corresponding frequency estimate is

$$F_{\text{max}} \approx 1000 / T_{\text{critical}} \text{ MHz} \quad (6)$$

when T_{critical} is expressed in nanoseconds. Positive WNS indicates that the implemented design satisfies the target setup constraint. Because implementation is timing driven, the value derived from one timing target should not be interpreted as a constraint-independent physical constant; the most informative operating point is obtained by progressively tightening the target until WNS approaches zero from the positive side.

B. Power and Composite Metrics

Post-route power is separated into static and dynamic components. Dynamic power is used for the primary architecture-level PDP because it is more sensitive to clocking and switching differences between these small logic cores, whereas the measured static component is essentially unchanged across the reported experiments. The dynamic-power PDP is

$$\text{PDP} = P_{\text{dynamic}} \times T_{\text{critical}} \quad (7)$$

which is expressed directly in nJ when power is in watts and delay is in nanoseconds. The FPGA area used is measured by the total implemented LUT count in the design. The LUT-based area-delay product is expressed as:

$$ADP = N_LUT \times T_critical \quad (8)$$

with units of LUT·ns, the LUT-based ADP is a technology-specific hardware-cost indicator and it may not be counted as physical silicon area.

V. RESULTS AND DISCUSSION

A. Direct and Measured FPGA Results

Table I summarizes the post-placement and route results obtained during FPGA realization. All reported values of WNS are positive, it is a indication of successful setup timing closure at all the listed targets. The obtained results also reveal that LUT count can vary with timing constraint because the synthesis and implementation using CAD tool may restructure and replicate logic to achieve timing goals.

TABLE I. POST-ROUTE FPGA RESULTS FOR THE 8-BIT EXACT AND ORDINARY TRUNCATED MULTIPLIERS

Arch.	Target (MHz)	TtargetPeriod (ns)	WNS (ns)	T_critical (ns)	Fmax (MHz)	P_dynamic (W)	P_Tot (W)	N_LUT	PDP (nJ)	ADP (LUT·ns)
Exact	100	10.00	3.50	6.50	153.87	0.014	0.119	71	0.0910	461.50
Exact	133	7.50	0.98	6.52	153.28	0.019	0.124	71	0.1239	462.92
Exact	166	6.00	0.14	5.86	170.53	0.024	0.129	82	0.1406	480.52
Exact	181	5.50	0.12	5.38	185.87	0.026	0.131	75	0.1399	403.50
Exact	190	5.25	0.07	5.19	192.86	0.027	0.132	82	0.1401	425.58
Ord. Trunc.	100	10.00	3.09	6.91	144.76	0.010	0.115	54	0.0691	373.14
Ord. Trunc.	133	7.50	1.12	6.38	156.69	0.014	0.118	54	0.0893	344.52
Ord. Trunc.	166	6.00	0.13	5.87	170.30	0.017	0.122	57	0.0998	334.59
Ord. Trunc.	181	5.50	0.27	5.23	191.24	0.019	0.123	63	0.0994	329.49
Ord. Trunc.	190	5.25	0.17	5.08	196.93	0.020	0.124	65	0.1016	330.20
Ord. Trunc.	200	5.00	0.04	4.96	201.45	0.020	0.125	67	0.0992	332.32

B. Timing Behavior: WNS, Critical Delay, and Fmax

At the 100-MHz target, the Exact multiplier shows WNS=+3.50 ns, T_critical=6.50 ns, and an estimated Fmax of 153.87 MHz, whereas the Ordinary Truncated multiplier gives WNS=+3.09 ns, T_critical=6.91 ns, and Fmax=144.76 MHz. It has highest margin for further optimization. It is also shown that truncation mechanism does not produce a timing advantage at every constraint always.

The reported results show that as the target period is tightened, both the designs converge, but the truncated architecture becomes faster. In further simulations, at 166 MHz, the critical delays in both the cases are essentially identical (5.86 ns Exact and 5.87 ns truncated). At 181 MHz, the truncated model reaches down to 5.23 ns versus 5.38 ns for Exact, yielding estimated Fmax values of 191.24 and 185.87 MHz, respectively. At the highest common 190-MHz target, WNS values improves from +0.07 ns to +0.17 ns for Exact to Ordinary Truncated respectfully. The critical delay also shown a fall in its value from 5.19 to 5.08 ns, a 2.12% reduction, while estimated Fmax increases from 192.86 to 196.93 MHz, a 2.11% which is an improvement in the performance.

The Ordinary Truncated designed model was simulated at the additional 200-MHz target; the timing values at this target are WNS=+0.04 ns, T_critical=4.96 ns, and estimated Fmax=201.45 MHz. at 200-MHz target Exact implementation does not meet timing closure so, it is not included in the measured dataset, but The Ordinary Truncated model meets the timing closure properly.

C. Dynamic Power and PDP

The estimation behavior of The Ordinary Truncated multiplier shows a consistent dynamic-power advantage over The Exact model at all five common target frequencies. In comparison to Exact, the reported values in The Ordinary Truncated multiplier for dynamic power shows reduction from 0.014 to 0.010 W at 100 MHz (28.57%), from 0.019 to 0.014 W at 133 MHz (26.32%), from 0.024 to 0.017 W at 166 MHz (29.17%), from 0.026 to 0.019 W at 181 MHz (26.92%), and from 0.027 to 0.020 W at 190 MHz (25.93%). The static component of power remains 0.105 W in all the reported runs.

PDP is the combined product of dynamic power and critical delay. At 190 MHz target, Exact and Ordinary Truncated give $0.027 \times 5.19 = 0.1401$ nJ and $0.020 \times 5.08 = 0.1016$ nJ respectively. The resulting 27.48% reduction is larger than the delay improvement alone because truncation reduces both switching power and delay. In all common targets, the truncated design shows a lower PDP than the Exact model.

D. LUT Utilization and ADP

The programmable-logic cost has been reduced in truncated architecture effectively. The reported results at 190-MHz target show that the LUT utilization decreases from 82 to 65 in the implementation, it results in a 20.73% reduction. The calculated ADP also decreases from 425.58 to 330.20 LUT·ns in case of truncated model, it is a 22.41% improvement in performance. At 100 MHz, the corresponding values are 461.50 and 373.14 LUT·ns. The absolute LUT count varies with target constraint because implementation optimization is allowed to trade logic structure for timing, but the truncated design remains more area-efficient at every common operating point in the measured dataset.

TABLE II. EXACT VERSUS ORDINARY TRUNCATED MULTIPLIER AT THE 190-MHz TARGET

Metric	Exact	Ordinary Truncated	Change
WNS (ns)	+0.07	+0.17	+0.10 ns margin
Critical delay (ns)	5.19	5.08	2.12% lower
Estimated Fmax (MHz)	192.86	196.93	2.11% higher
Dynamic power (W)	0.027	0.020	25.93% lower
PDP (nJ)	0.1401	0.1016	27.48% lower
LUTs	82	65	20.73% lower
ADP (LUT·ns)	425.58	330.20	22.41% lower

In Table II, the identified highest common timing target for direct comparison. It is shown that ordinary truncation have dominant gains in dynamic power, PDP, LUT utilization, and ADP; but the WNS value change is measurable but comparatively modest.

VI. CONCLUSION

The presented in this paper is a controlled FPGA evaluation of an 8-bit unsigned Ordinary Truncated multiplier and an Exact multiplier on the Avnet ZedBoard XC7Z020-CLG484-1. The truncated architecture removes effectively all partial products below reference column CUT=6 and is investigated under the same for synthesis and implementation strategy with disabling DSP block utilization. Across all the timing targets, the truncated design parameters consistently reduces for LUT utilization, dynamic power, PDP, and ADP in values. At the highest common 190-MHz target, the performance of critical delay decreases from 5.19 to 5.08 ns (2.12%), calculated Fmax increases from 192.86 to 196.93 MHz (2.11%), dynamic power decreases from 0.027 to 0.020 W (25.93%), LUT utilization decreases from 82 to 65 (20.73%), calculated PDP decreases from 0.1401 to 0.1016 nJ (27.48%), and measured ADP decreases from 425.58 to 330.20 LUT·ns (22.41%). Also, the truncated design run to achieves timing closure at the 200-MHz target, where WNS reported is +0.04 ns. The results show that ordinary partial-product truncation provides a clear FPGA hardware-efficiency benefit.

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