

On-Chip Techniques for Electromagnetic Interference (EMI) reduction

Monirul Islam¹, Rajib Imran², Bushra Mahjabeen³
(ASIC Design Engineer, Fastrack Anontex Limited, Dhaka, Bangladesh)

Abstract: In modern days, integrated circuits are facing different challenges with its high speed features. One of the big challenges is EMI emission from electronic devices. Different regulatory bodies like US (FCC), EN etc have strict regulations aim at limiting the amount of EMI radiations. On the designer's point of view, these effects can range from a simple degradation of a specific signal to a total loss of data. To increase chip performance the clock speed is needed to be increased which gives rise to EMI immensely, however different approaches in the design cycle can successfully limit the emission at an expected level. This paper analyses different approaches for significant low cost reduction mechanisms. For higher data rates like 8 GT/s or 16 GT/s- Clock scrambling, Clock dithering, spread spectrum clocking, differential clocking and using clock buffers etc are the most beneficial methods especially for the faster System on Chip (SoC).

Keywords- EMI, Clock scrambling, spread spectrum, EMI emissions, EMI reduction, Dithering Ckt etc.

I. INTRODUCTION

Electromagnetic interference (EMI) is a disturbance that affects an electrical circuit due to either electromagnetic induction or electromagnetic radiation emitted from a source [1]. EMI is an electromagnetic wave, which consists of both electric (E-field) and magnetic (H-field) waves running perpendicular to each other [2]. As microprocessor speeds increase, reducing Electromagnetic Interference becomes an essential part of design considerations. This radiation, mainly produced by fundamental and low-order harmonics, unfortunately coincides and interferes with other signals.

The energy concentrated at the discrete frequencies of high frequency periodic signals radiated off-chip cause serious problem in consumer electronics. The radiated signals should be below an acceptable level to ensure the functionality and the performance of the system. Several different methods have been used to help deal with EMI directly on-chip, among them frequency modulation of the system clock, also called clock dithering, and control of pad output rise and fall times over process, voltage, and temperature (PVT) variations, clock scrambling, spread spectrum clock generation are the most effective techniques. Most of the widely available methods are off-chip and to have a better result in the EMI reduction we need to have modern design within the architecture of the chip design. Therefore, here we are going to introduce different efficient approaches a designer should think of to make his architectural solution of EMI reduction more developed. Besides, our design considerations can be applicable for EMI reduction on FPGA, ASIC, CPLD etc devices.

II. EMI BRIEF THEORY

As we mentioned earlier, Electromagnetic Interference (EMI) is unwanted radiation caused by internal source (conductors) or external source (wiring) that disrupts the natural function of an electronic device or a chip. The generation of EMI inside chips is rising day by day due to the increment in their speed-which is a result of using higher frequency signals like clock, inputs, outputs etc. EMI is also increasing due to making chips smaller in size. Moreover clock is no longer fed to just one point; rather it is being distributed in various nodes throughout the chip. This load increment on clock gives rise to EMI [4]. For making the chip work faster, the chip is needed to be smaller in size-which is also considered as an important factor for increasing EMI. As the chip size gets compact, the conductors get closer and this close proximity causes interference in the signals carried by the conductors.

EMI can be generated in two possible ways. One is due to physical contact of semiconductors which is termed as conducted emission and it is measured below 30MHz. The other is known as radiated emission that is caused as a result of electromagnetic induction which is found to be above 30MHz. The appraisalment of EMI is given by the following formula:

$$EMI = kIAf^2 \dots\dots\dots (1)$$

Where k is proportionality constant that depend on chip material and other factors, A is loop area, I is amount of current flowing and f is frequency of the signal by which EMI is created [3].

Internal EMI disrupts the normal functionality of any electronic device. For example, EMI causes skin effect, proximity effect, hysteresis losses, transients, voltage drops, electromagnetic disturbances, eddy current losses, harmonic distortion, and reduction in the permeability of the material. It is also the reason for injection of high frequency noise in power lines and wires acting as antennas that directly emit radiation. When these problems are created inside a chip it hampers the normal functionality of the chip. For example, EMI creates clock obstacle which results setup and hold time violation. In addition it causes disruption in the clock tree network operation and also in synchronization of I/O signal with clock. Sometimes power or ground pins can be burnt as a result of excessive EMI. It also gives rise to excessive twist noise which is very harmful for proper signal flow. So, EMI is expected to be eliminated completely from a chip. As this is not possible practically, it is required to be eliminated as much as possible for better functionality and longevity of any electronic device or chip. The permissible amount of EMI emission from an electronic device for the soundness of human health around that device is decided by United States Federal Communication Commission's (FCC) Part 15 and International Electro technical Commission's International Special Committee on Radio Interference (CISPR) Publication 22 class B limits [3]. So reducing EMI from any device or chip is a must. However, there are a number of ways to reduce EMI from a chip like clock scrambling method, spread spectrum CLK generation, differential clocking, typical clock dithering circuit, using CLK buffer, multi segment clocking etc. Now, for example an approximation of EMI reduction using spread spectrum technique is presented for better understanding of (a general) method and its purpose.

TABLE 1: Approximate peak reduction by Spread Spectrum

Clock Frequency	Radiation dB (*)	Pick EMI Reduction (PR)	Measurement Frequency
66~76 MHz	40.0	<8dB	600~700 MHz (9 th harmonic)
90~100 MHz	43.5		650~700 MHz (7 th harmonic)

*FCC Part 15 Class B Limits.

Like spread spectrum technique other methods can also be used for the purpose of reduction of EMI. Here by contemplating a few of them, we are going to deliberate a befitting method to solve the EMI problem inside chips.

III. TYPICAL PROBLEM CAUSED BY EMI

Problems caused by EMI in chips are consequential and undesired. Before taking steps to remove these problems they must be expatiated. One of the problems caused by EMI is direct radiation from chip surface. The conductors inside the chip act as antennas as an effect of flowing high current through them. This occurs due to Large Scale Integration. However, the level of radiation is smaller due to this kind of problem and can be deprecated by customizing chip design.

Another problem is conducting noise to signaling ports which causes off chip wires acting as antennas as well. Effect of this kind of noise source is significant but can be removed without many obstructions. Moreover wire subsystem clocks require independent EMI spreading in such case, the data and the clock can lose synchronization if a modified design is not utilized. This issue can grossly misalign the clock information with the data integrity.

Now, the most significant effect of EMI on chip is power line conducting high frequency noise signal. Chip switching activity contributes immensely to power/ground current. As high frequency current is the main source of EMI, the increment in power/ground current gives a significant amount of increase of EMI inside chips. EMI produced by this method is the hardest to remove from a chip [8].

IV. TECHNIQUES TO REDUCE EMI ON SYSTEM ON CHIP

In this section, we will propose various techniques to reduce EMI specially system on chip, which is the main attraction of our discussions. We declared earlier that electromagnetic radiation can't be removed entirely but it can be kept within a limit and by following novel techniques we can make our design more standard at preventing interference between electronic devices and should yield expected reduction in the electromagnetic interference. The strict regulations of regulatory bodies and the cost sensitivity of their impact have led to the development of alternative and less expensive solutions. In the following discussion we will introduces some of those effective techniques, their circuitry and issues how they impact on EMI reduction in brief.

In modern integrated circuits, almost any electrical transitions with sharp edges, such as clock, data, address etc produces electromagnetic radiation. Due to high performance modern devices we need to increase their

clock speed. To meet the timing requirement (such as set up and hold time) the transition edge or the slew rate became faster too. Besides, as stated earlier, clocks are not only fed one or two blocks inside the chip rather they are distributed among the whole architecture depending on their requirement. Moreover, increased memory requirements and excessive loads on the clock lines have a large contribution producing electromagnetic radiation. The periodic nature with the highest frequency clock signal derived from the digital clock and other signals derived from the clock are the sources for the electromagnetic radiation especially on chip. Therefore, we are more attentive manipulating the clock circuitry in such a fashion that will help us to make a modern design with preventing the radiation.

4.1 CLOCK SCRAMBLING MECHANISM

In this mechanism, the spectral profile of the digital clock is altering to reduce EMI reduction. The clock signal is mixing with a modulated signal of lower frequency. The mixing is accomplished with an XOR gate to get a suppressed carrier clock in order to spread the spectrum/energy of the higher frequency digital clock. In theory, this clocking doesn't introduce jitter. However, there is a drawback that the transition of the suppressed clock is lost during the transition of the modulating signal. This may lose the communication time of the digital system. This drawback can be obviated by using demodulated circuit at various ends of the clock distribution network.

By doing this, the signal in the clock distribution network can suppress EMI. Though, the other signals in the rest of the chip emit radiation at the clock frequencies. Besides, even clock harmonics into the spectrum can't be suppressed via scrambling [4,9].

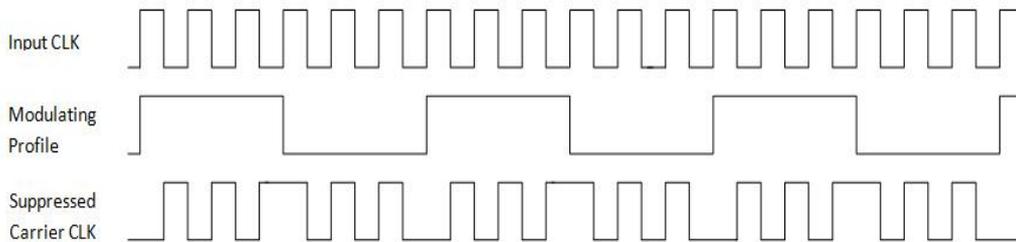


Figure 1: Time domain representation of scrambling method.

4.2 SPREAD SPECTRUM CLOCK GENERATOR

In spread spectrum method, the same technique is applied like clock scrambling method which modulates the signal and spreads the energy over a wider frequency range but in a different approach. This is a widely used method for EMI reduction in the industry. Therefore, we will discuss the method a bit detail.

The spread spectrum clock generator (SSCG) reduces the radiated emission by spreading the emissions over a wider frequency band. This band can be broadened by slowly frequency modulating the higher frequency clock over a few hundred kHz with the adequate reductions in the measured radiation level. Thus, SSC modulated the clock frequency along a predetermined path with a specific determined modulation profile. By deviating the period with a small amount, the energy of the clock is widely spread and the peak emission is attenuated significantly. The greater the deviation, and slower the frequency of the modulated signal, the attenuation will be greater. Here, the frequency is generally selected to be larger than 30 kHz and small enough not to upset the PC system timing [3,4].

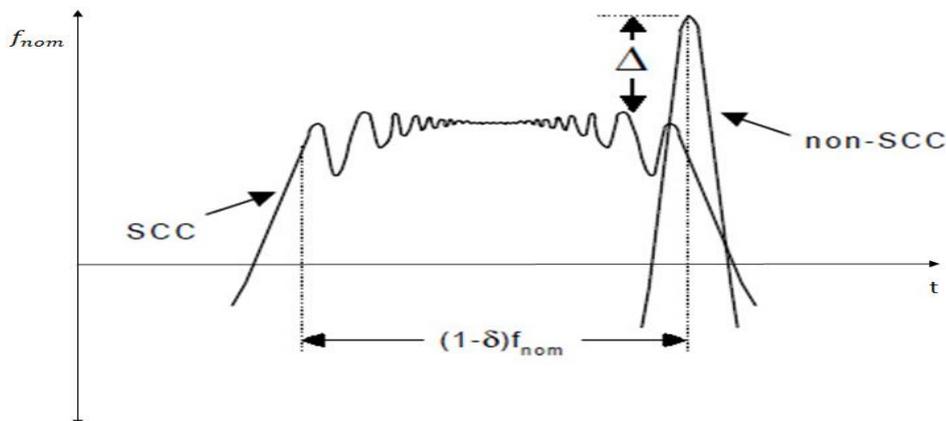


Figure 2: Spread spectrum clocking.

Radiated emissions are typically confined in a sharp band concentrated around clock frequency harmonics. By uniformly distributing the radiation in a wide band, regulatory measurement levels can be reduced. Thus the modulation amount increases, so does the amount of EMI reduction. Let's talk about how we can implement this on design.

We can implement this in two ways: a) PLL based SSGC and b) Delay cell approach.

4.2.1 PLL BASED SSGC

In this fashion, the clock frequency is directly modulated with a predetermined signal. Specially, this is done by a voltage control oscillator (VCO) has its input voltage controlled by a modulation waveform. We can make it more simple using triangular modulation profile. These techniques introduce some more peripheral block such as phase frequency detector (PFD) with the charge pump output and a VCO. Conventional PLL based SSC has a significant drawback that it suffers due to jitter. This also can reduce the expected amount to want to achieve from the circuitry. Digital PLL can be a smart choice to make it more efficient [5,9].

4.2.2 DELAY CELL APPROACH

We can control the clock frequency by controlling the temporal spacing of the clock edges. In this approach, single or multiple based on the requirement delay elements are used to control the speed of the clk. This approach is a very simple solution reducing jitter that we may face using PLL based SSGC. Delay elements are used in series that create a delay chain. When the clock signal approaches through the chain, each edge encounter a small amount of delay which form a good shape of the clock signal into a spread spectrum clock signal. This method showed a significant result in variance of random jitter which helps to achieve greater reduction in EMI using spread spectrum techniques. It must be cautious that the digital delay cell array must be implemented with simple and low jitter implementation. To get it, we can use differential current starved inverter based delay circuit. We have to use a counter to create triangular modulation waveform to control the current passing through this inverter.

On a whole, SSC can be effectively used to reduce peak radiation by approximately 8 dB [9].

4.3 DIFFERENTIAL CLOCKING

In differential clocking, the clock generator supplies both the clock and the clock bar traces. The designers have to route the two traces together in parallel. The clock bar has the equal and opposite current with the fundamental clock which is 180 degree out of phase. In differential clocking, by cancelling the H-field, EMI emissions can be reduce by a significant amount. As H-fields travel with the current flow according to the right hand rule, two current of opposite direction and 180 degree out of phase will have their H-field cancelled. This results in lower emission. It also reduces the amount of noise coupled to I/O traces, which generates EMI.

According to the Intel Corporation they suggested for best results [2, 3] -

- a) The trace lengths and the 180 degree phase difference between the two clocks needs to be closely matched.
- b) The real and parasitic terminations of each differential line should be the same.

The spaces between two traces must be as small as possible. We can place the ground traces on the outside of the differential pair to reduce more emission.

4.4 CLOCK DITHERING CIRCUIT

Clock Dithering is another on-chip solution for EMI reduction. This is a special frequency modulation technique. In this technique the frequency generated by the Voltage Control Oscillator (VCO) is controlled and dominated in such a way that the output frequency of the Phase locked Loop (PLL)/ PLL clock (clk) is the same as the input frequency. In fig. 3 shows a typical clock dithering circuit. The circuit depends on the control of the frequency of the voltage-controlled oscillator (VCO) of a phase-locked loop by appropriate division of the reference clock (RefClk) by the input divider (Q) and of the VCO clock (fvco) by the feedback divider (P). The dividers all consist of digital counters. The divided digital waveforms are compared by the phase-frequency detector, which puts out an up or down signal pulse depending on whether the P waveform lags or leads the Q waveform. The width of the up or down pulse is proportional to the amount of lag or lead. The up or down pulse is fed to the charge pump and low-pass filter block, which translates it to a change in the VCO control voltage (vcntl). The VCO control voltage is repeatedly adjusted by up or down pulses until the VCO frequency fvco is such that the P and Q waveforms align (i.e., the up and down pulses are of nearly zero width). At this point-

$$\frac{RefClk}{Q} = \frac{fvco}{P} \dots\dots\dots (2)$$

Since the VCO frequency is divided by the output divider D, the actual output signal-

$$PLLClk = \frac{fvco}{D} \dots\dots\dots(3)$$

Thus, the output frequency at stable operation is dictated by the values of the Q, P and D dividers and by appropriate substitution can be written as

$$PllClk = \frac{P(RefClk)}{QD} \dots\dots(4)$$

Thus, for example, if RefClk=16 MHz, P=50, Q=10 and D=5, the output frequency PllClk is the same as the input frequency, 16 MHz [1].

If the P counter endpoint is 49, the output frequency is 15.68MHz, 2% less than 16 MHz. Therefore, a simple way to achieve dithering is to change the P counter endpoint back and forth between 50 and 49 at some reasonable rate. Controlling this rate is the job of the M counter, that is, the P counter endpoint is changed each time the modulation counter (M) reaches its endpoint. A typical value for M might be 10, so that the modulation frequency is then 16 MHz/(QM)=160 kHz. In practice, either the Q counter, the P counter, or both can be changed to achieve different target frequencies. Furthermore, by using both the rising and falling edges of the VCO clock, P can effectively have values such as 50.5 and 49.5, thus allowing a symmetric deviation of 1% about a center value of 50 [1].

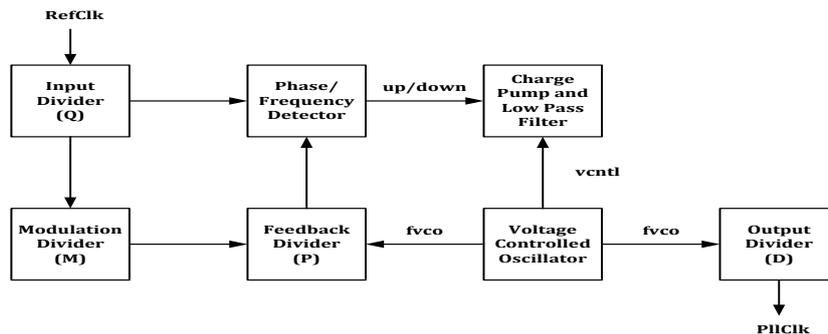


Figure 3: Block Diagram of a typical Dithering Phase Locked Loop.

The scheme described above can be thought of as square wave modulation because the phase-locked loop is asked to jump instantaneously from one frequency to another. Because real systems don't respond that way, and because of deliberate filtering to moderate this sudden transition, the actual frequency modulation waveform looks more like a ringing square wave. Square wave modulation as just described has been used successfully in a number of products to reduce EMI emission sufficiently to allow products to pass FCC testing. In some applications, the cycle-to-cycle jitter associated with this modulation method cannot be tolerated by the system. This drawback has been addressed by the development of triangle wave modulation [1,2].

Conducted EMI measurements of the frequency spectrum has lower peak values for the square-wave-modulated part than for the triangular-wave-modulated part, which appeared to be a result of greater spectrum spreading because of square wave overshoot. Radiated emissions from the boards using parts designed with triangular wave modulation exhibited less noise overall.

4.5 USING CLOCK BUFFERS

Faster data rates made a big challenge in the EMI reduction techniques. Spread Spectrum technique is effective where a single master clock acts as the source and other clock and data signals derive their timing from the source clk. While using this technique directly on different sub-system clocks, it encounters challenges synchronization problems for which we need special care to take on the design [3,5,6].

In certain design, where sub-system clocks require independent EMI spreading, the data and clock lose synchronization which referred as Cycle slip. This can mitigate by using timing safe clock buffer. This device can be directly inserted into the sub-system clock path as an active EMI filter. The Timing-safe clock buffer allows spread spectrum EMI reduction to be used in the SDRAM memory clock distribution lines. Besides, this solution is independent of the ASIC, and doesn't have any dependency on the other areas of the system [5].

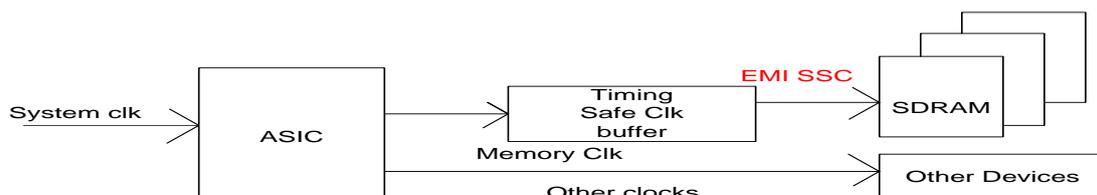


Figure 4: EMI reduction design using Timing-safe Clock Buffer.

Thus the solution effectively reduces the peak amplitude of clock signals ensuring the compliance with FCC standards maintaining synchronization in the whole architecture in order to protect data integrity.

4.6 OTHER EFFICIENT TECHNIQUES

To make a design combating the EMI emissions, the designers follow a series of guides and methods. In chip architecture, there are different sources of EMI emissions, so following one or two techniques will satisfy that particular reason. To have an overall efficient reduction we have to be concerned about some useful methods. They are experimentally proved and widely used in industry to achieve efficient outcomes. Here are some of those methods and due to space regulation we are discussing them in brief [5,6,7,8,9] -

- a) Solid grounds and power planes have to be used in the design.
- b) We should place the clock drivers near the center of the PCB rather than at the periphery. For the clock traces that are routed on the surface plane, it is better to route parallel ground traces on the other side of the clock trace. A smart choice here is to place the clock traces between the ground and Vcc plane.
- c) Impedance must be matched as closely as possible. Long clock traces should not run parallel as they introduce crosstalk which contributes to EMI.
- d) We should use Vdd decoupling capacitors for clock sources. All capacitors must be placed within 20 mils of the Vdd pins.
- e) RC filters at the clock sources are efficient to control rise and fall times.
- f) Power supply pins should be placed next to the ground pins. Besides power and ground leads should be kept in parallel.
- g) Should keep the high speed lines short and direct.
- h) Clock and digital lines must be placed as far away as analog input and voltage reference pins.
- i) Clock circuit must be placed away from I/O cables.

Faster data rates made a big challenge in the EMI reduction techniques. Spread Spectrum technique is effective where a single master clock acts as the source and other clock and data signals derive their timing from the source clk. While using this technique directly on different sub-system clocks, it encounters challenges synchronization problems for which we need special care to take on the design [3,5,6].

V. CONCLUSION

In this paper, we proposed portable, low power, and area-efficient EMI reduction techniques for SoC applications. Based on the proposed techniques, the spreading ratio can be specified flexibly by application demands while keeping the phase tracking capability. Every scheme we describe above can potentially reduce emissions in the order of approximately below 7 dB. A smart choice in an architectural design that can reduce the design cost at the early age of its cycle. So designers should consider the issue like EMI emission while designing his chip. In this paper, though we proposed the efficient theoretical methods of different approaches but they are highly used in industries. Besides, we have collected different industry papers to make a credible research which we gave in our reference section. In future, our plan is to make an experimental comparison between different methods to investigate how much of the radiated emission from a chip especially from the clock distribution network and their solution to mitigate them in the modern design.

REFERENCES

- [1] Cornelis D. Hoekstra, Frequency Modulation of System Clocks for EMI Reduction, *Hewlett-Packard Journal*, Article 13, August, 1997.
- [2] Dr. Sergiu Radu, An Overview of Chip Level EMC Problems, *Sun Microsystems, Inc.*
- [3] Design for EMI, *Intel*, Application note AP-589, February 1999.
- [4] Cameron Katrai, Chris Arcus., EMI Reduction Techniques, *Pericom Semiconductor Corporation*, Application Note 11, 1998, 59-64.
- [5] Timing-Safe™ Spread Spectrum EMI Reduction, *ON Semiconductor*, P3P623S05A/B and P3P623S09A/B, July, 2010.
- [6] Understanding Radiated EMI, *Applications Engineering Group, MCU Division, Silicon Labs.*
- [7] D.J.Prasad kumar, B.Chinna rao, P.M.Francis, A Novel Techniques to Reduce EMI Attenuation by Triangular Modulation, *International Journal of Engineering Research & Technology (IJERT)*, Vol. 1 Issue 6, August, 2012.
- [8] Sachio Hayashi, Masaaki Yamada, EMI Noise Analysis under ASIC design Environment, *DA Development Dept., Semiconductor DA & Test Engineering Centre, Toshiba Corporation.*
- [9] Subramaniam Venkatraman, Matthew Leslie, Novel spread spectrum clock generator.