A Novel Enhanced Noise-Immunity Design Technique for Dynamic Logic Gates

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Abstract : *This paper focuses on a new enhanced noise-tolerant dynamic circuit design technique. The effectiveness of this technique is demonstrated by means of HSPICE level 49 simulations for two and four input AND gate. Noise immunity improvement of proposed technique is compared with previous techniques [1]. Simulation results show that the proposed technique has a very good improvement in the noise tolerance and the ANTE-delay quotient over the conventional dynamic logic circuits and decrease in power consumption with less performance degradation than existing ones for AND gates.*

Keywords: *Keeper transistor; Noise immunity; Dynamic circuits; Domino Logic; CMOS ; ANTE; EANTE; PDN;*

I. INTRODUCTION

In digital integrated circuit noise has become one of the foremost issues in the design of very deep submicron VLSI chips. Noise in digital integrated circuits refers to any phenomenon that causes the voltage at a node to deviate from its nominal value. While these noises always existed, in the past they had little impact on the performance of integrated circuits and were often neglected. It is the unstopped aggressive technology scaling in an effort to continuously improve chip performance and integration level that makes noise play an increasingly important role in comparison with conventional design metrics like area, speed and power consumption [2].

Together with technology scaling, circuits designed using dynamic logic styles can be considerably faster and more compact than their static CMOS counterparts.
This is especially the case with wide fan-in dynamic logic gates where a single gate can realize the logic function that otherwise would require multiple levels of static CMOS logic gates. Therefore, wide fan-in dynamic gates are routinely employed in performance critical blocks of high-performance chips, such as in microprocessor, digital signal processor, and so on.

The switching threshold voltage of a dynamic CMOS logic gate, which is defined as the input voltage level at which the gate output changes its state. In comparison, the switching threshold voltage of static CMOS logic gate is typically around half the supply voltage [2] [3]. Therefore, dynamic logic gates inherently have less noise immunity than static CMOS logic gates and are the weak link in a high-performance VLSI chip designed using deep submicron process technology. In fact, using proposed method in this paper, noise tolerance of dynamic circuits can be improved beyond the level of static CMOS logic gates while still retain their advantage in performance.

A number of design techniques have been developed in the past two decades in an effort to reinforce this weak link. However, existing remedial techniques improve dynamic circuit noise tolerance at a significant cost in terms of one or more other important design metrics like circuit area, speed and power consumption [2][8].

In this paper, we propose new noise tolerance dynamic circuit which increases noise immunity. The noise immunity is the ability of a device to operate in the presence of noise disturbance.

In order to determine which technique has more noise-immunity, the performance measures the Average Noise Threshold Energy (ANTE) and Average Noise Threshold Energy Normalised Energy (EANTE) are calculated and compared. The ANTE metric is defined as the average input noise energy that the circuit can tolerate [1]. EANTE is a related parameter that quantitatively describes energy-efficiency which is the ANTE-normalized energy, given by the ratio of the average energy consumption of a circuit to its ANTE measure. The goal of noise-tolerance techniques is to increase ANTE, while reducing EANTE.

The rest of this paper is organized as follows. Section II briefly explains various types of noise sources in dynamic logic circuits designed using deep submicron process technology. Section III describes overview of existing noise tolerant techniques. In section IV proposed technique is introduced. In section V proposed technique with keeper is explained. Section VI presents simulation results that compare the performance of

different noise-tolerant techniques as well as conventional dynamic circuit. Conclusion is presented in section VII.

II.   Noises In Dynamic Logic Circuits

In this paper the discussion will be focused on one type of dynamic circuits known as domino CMOS logic circuits, which is probably the most widely used dynamic logic style [2] [3].
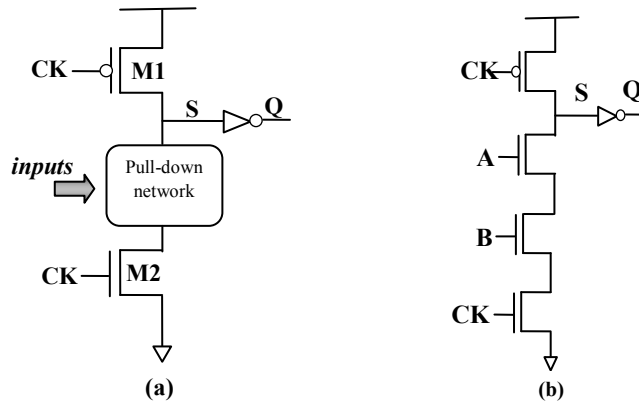

Fig.1 Domino logic gate. (a) Circuit schematic. (b) Two-input domino AND gate.

A typical n-type domino CMOS logic gate, as shown in Fig.1(a). Which consists of clock controlled transistors M1 and M2, a pull-down n-type transistor network (PDN), and an output driver. The operation of a domino CMOS logic gate can be divided into two phases, the *pre-charge* phase where the clock CK is low, the dynamic node S is charged to logic high through M1 and the output of the gate Q is low, and the *evaluation* phase starts when the clock goes high. In which M1 is OFF and M2 is ON. The dynamic node S discharges or retains its charge depending on the inputs to the pull-down network. A 2-input domino AND gate is illustrated in Fig.1(b).

Noise sources in dynamic logic circuits can be broadly classified into two basic types: i) gate internal noises of which charge sharing noise and leakage noise are of most importance. ii) External noises including input noise, power and ground noise, and substrate noise [2][9].

The charge sharing noise is caused by charge redistribution between the dynamic node and the internal nodes of the pull-down network. The Leakage noise refers to the possible charge loss in the evaluation phase due to sub threshold leakage current. The input noise refers to noise presented at the inputs of a logic gate, which are primarily caused by the coupling effect, also known as crosstalk, among adjacent signal wires. The power and ground noise is mainly caused due to the parasitic resistance and inductance at the power and ground networks and at the chip package. The substrate noise can affect the signal integrity of a logic gate through substrate coupling. In all, these noises, together with other sources of disturbance like process variation, alpha particle radiation and so on, can endanger the correct function of dynamic logic circuits designed using very deep submicron process technology and a desired noise-tolerant design technique should be able to improve the noise immunity of dynamic logic gates against all afore-mentioned noises.

III.   Overview Of Existing Noise Tolerant Techniques

To improve the noise-immunity of a dynamic CMOS logic gates, three techniques have been proposed in literature, they are.

3.1 **Feedback keeper technique**

To enhance the noise tolerance of dynamic CMOS logic gates use a weak transistor known as keeper (MK), at the dynamic node S, as shown in fig.2. MK transistor draws a small amount of current from the power supply to dynamic node S, so that the charge stored in the dynamic node is maintained [1]. On the falling edge of the clock signal (CLK) the circuit enters into the pre-charge phase, the M1 transistor is ON then the dynamic node is pre-charged to a high logic level and the output Q discharges to a low logic level. Whenever the output goes to low the MK transistor ON but, the amount of current flowing through keeper is minimum because the dynamic node S value is high. On the rising edge of the clock signal, the circuit enters into evaluation then the dynamic node S value depends on the PDN state. If the PDN is OFF the dynamic node S is same as high logic level and output Q remains low. If PDN is ON it forms a dc path to the dynamic node which discharges to low and output Q goes to high then the MK transistor turning OFF.

3.2 Twin transistor technique

To improve the dynamic gate noise immunity use twin transistor technique. In this circuit the additional transistor M4 called twin transistor is used. The M4 transistor drain node is connected to gate of M2 transistor [4], as shown in fig.3. On the falling edge of the clock the circuit enter into the pre-charge phase where the M1 transistor is ON and the dynamic node pre-charged to high then the output Q goes to low. When the dynamic node S pre-charged to high then the extra transistor M4 is ON during the start of evaluation phase. In evaluation phase clock signal is high the M1 transistor is OFF, If the input is also high then the node voltage X increases with input as transistor M4 is ON, which increases switching threshold of the circuit, in turn this increases noise immunity of the circuit. The main disadvantage is it increases input gate capacitance and this technique is not suitable for certain logic function, because it may short input nodes.
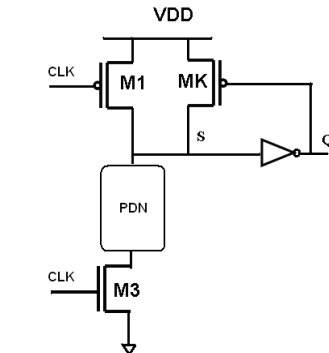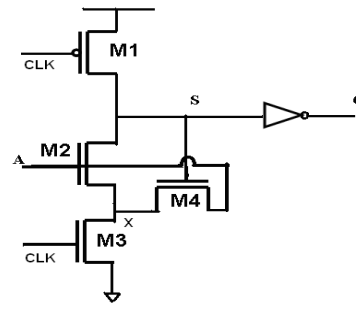
Fig.2 Feedback keeper technique

Fig.3 Twin transistor technique

3.3 Isolated noise tolerant technique(INT)

This is widely used technique to enhance the noise immunity. This technique uses both preventing dynamic node from high impedance and raising source voltage to improve noise immunity [5], as show in fig.4. The isolated noise tolerant technique can rise the source voltage of pull down network V_{SPDN}, to enhance the noise immunity of dynamic circuit from V_{th} to V_{thN} ($V_{thN=}V_{th}+V_{SPDN}$).

INT technique *operation*:

The INT technique operates in 3 cases: Pre-charge phase operation, Evaluation phase in normal operation and Evaluation phase with noise interference operation.

In pre-charge phase the clock signal CLK is low and the inverse clock signal CLKB is high. Then the node X is charged to high and Q goes to low the MNT2 transistor is ON by CLKB and MNT3 transistor is turned OFF by Q.

In evaluation phase the CLK is high and CLKB is low, the M1 is OFF then the dynamic node X is floating. As input A is at logic '0' the MNT2 transistor is turned OFF by CLKB and MNT3 transistor is turn OFF by input which is at logic '0'. Then the result of node X is isolated and latched in the logic high to maintain the conduction of MNT1 transistor. The clock feed through effect caused by CLKB can lower the voltage at node X. To charge the node X to V_{DD} the MNT4 transistor is used to provide a conduction path. So the clock feed effect can be eliminated and enhance noise tolerant ability. As input A is at logic '1' node X is pull down to low and output high.

When the noise interrupts the circuit the noise charged can be drained away immediately through MNT1 transistor to source node then the source voltage of MNT1 transistor will be raised by the disturbing signal so the noise ability can be enhanced. In this phase the conduction situation of MNT1 transistor can be hold because the node X is isolated. Therefore the noise tolerant mechanism can be protected and the noise
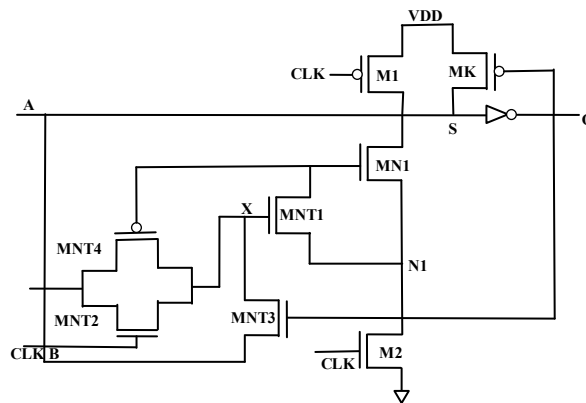
Fig.4 Isolated noise tolerant technique

tolerant ability will not degrade even under noise interferences. The main advantage is it increases the noise immunity. The main disadvantage is increased area, increased dynamic node capacitance and increased delay. The analysis shows, all noise types against by the keeper technique to improve the circuit robustness. Keeper presents low power consumption and it is suitable for all logic functions. In existing technique the isolated noise tolerant technique presents the best results in noise immunity, but delay increases when compared with feedback keeper technique and twin transistor technique.
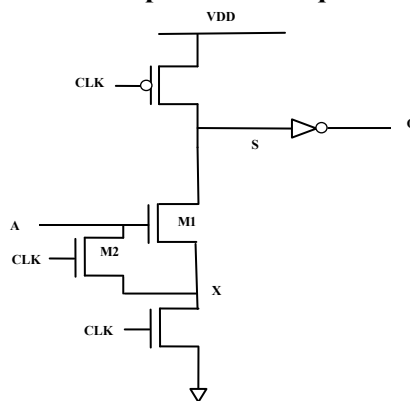
IV. Proposed Technique

Fig.5. a buffer circuit with proposed technique

The buffer circuit with proposed technique is shown in fig.5. This technique increases noise immunity by raising source voltage. The M2 transistor provides a path to transmit noise to raise the source voltage and enhance the noise immunity. The proposed technique operate in the following three phases.

4a. Operation in pre-charge phase

The operation of pre-charge phase is shown in fig.5(a). On the falling edge of the clock the circuit enters into pre-charge phase. In pre-charge phase clock is low and the dynamic node S is pre-charged to high then output Q goes to low.

4b. Operation in evaluation phase

In the evaluation phase the clock is high, pre-charge transistor OFF and extra transistor M2 is ON. This turns on the noise tolerant mechanism. As the input A is logic '0' the noise tolerant mechanism is achieved by M2 which is illustrated in fig.5(b). As input A is logic '1' the node S will pull down to logic low output Q is logic high, as shown in fig.5(c).

4c. Operation in evaluation phase with noise interference.

When the noise interrupts the circuit illustrated in fig.5(d). Then the noise can be drained away immediately through M2 transistor to node X and then source voltage of M1 will be raised by the disturbing signal. Hence the noise tolerant ability can be enhanced. In this evaluation phase M2 transistor is always ON. So that the proposed technique will provide more noise immunity under high noise environment also.
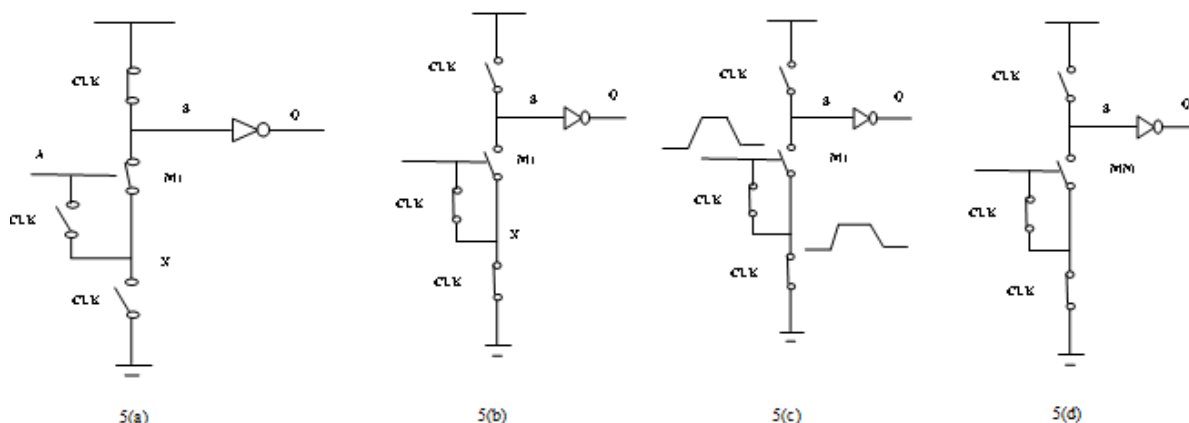
Fig. 5(a). Operate in Pre-charge phase 5(b). Normal operation in evaluation phase as input signal is '0' 5(c). Normal operation in evaluation phase as input signal is '1' 5(d). In evaluation phase with noise interference

V. Proposed Technique With Keeper Transistor

The proposed technique with keeper transistor circuit uses preventing dynamic node and raising source voltage is shown in fig.6. In pre-charge phase the operation is same as proposed technique. Hence the MK transistor is ON, during the start of evaluation phase. The keeper transistor supplies a small amount of current from the power supply network to the dynamic node of the gate. So that the charge stored in dynamic node is maintained. Therefore, this keeper transistor further increases more noise immunity of dynamic circuits.
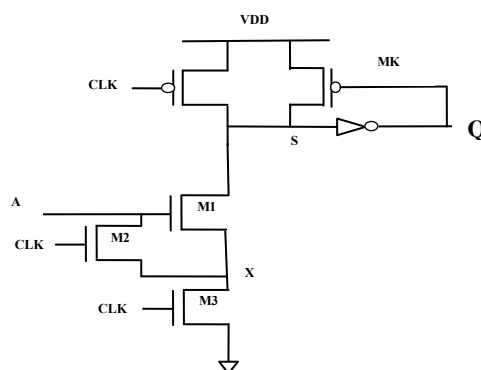

Fig.6 The buffer circuit using proposed technique with keeper transistor.

VI. Simulation Results

The feedback keeper technique provides more noise immunity with less area and speed in preventing dynamic node from high impedance. Twin transistor technique and isolated noise tolerant techniques provide more noise immunity in rising source voltage.

The noise immunity curves are plotted for a dynamic buffer circuit is shown in fig.7. These curves were obtained by applying noise pulse with different width and amplitude in one of the inputs of the gate [7]. These curves are plotted by keeping delay constant for all the techniques and frequency of operation at $500MH_Z$.
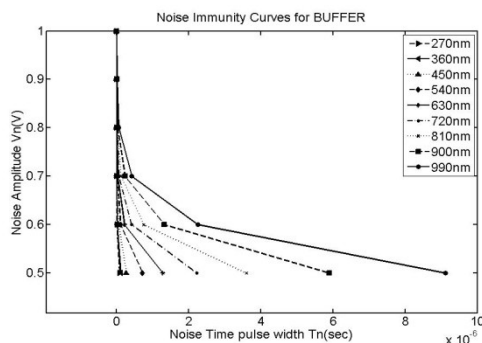

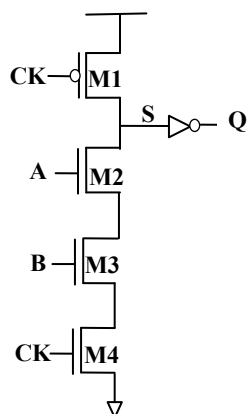Fig.7 Noise immunity curves for different widths

Fig.8 2-input AND gate using conventional dynamic circuit.

For the 2-input AND gate using conventional dynamic circuit as shown in fig. 8. Noise pulses are applied to the input A and the input B remains in a logic HIGH level during evaluation phase, because if two inputs are in logic HIGH level then only the dynamic node S is discharged.

The noise immunity curves for different techniques are shown in fig.9. From this simulation results the isolated noise tolerant technique provides more noise immunity compare to proposed technique. But it is less compared to proposed technique with keeper.
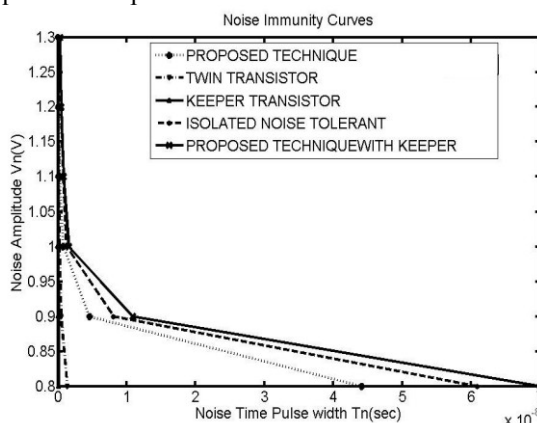
Fig.9. Noise immunity curves for 2-input AND gate for different techniques.

The Noise metrics for 2-input AND gate are shown in table I. For a circuit, to be more immune to noise ANTE [6] [7] must be as high as possible, and EANTE must be low. So the proposed technique with keeper provides more noise immunity with low energy consumption.

TABLE I
Noise metrics for 2-input AND gate

TECHNIQUE	ANTE(V^2pS)	EANTE*10^{-5}
Conventional	0026.449	110.000
Keeper transistor	0310.210	011.600
Twin transistor	1108.400	003.070
Isolated noise tolerant	8125.757	000.541
Proposed	5550.000	000.550
Proposed with keeper	9571.860	000.384

The table II, represents delay and power for 2-input AND gate the proposed technique has less delay as compared to existing techniques except twin transistor, the power consumption also reduced.

TABLE II
Delay and power for 2-input AND gate

TECHNIQUE	DELAY(pS)	POWER(μW)
Keeper transistor	099.38	18.09
Twin transistor	084.17	17.07
Isolated noise tolerant	242.50	22.00
Proposed	086.29	15.30
Proposed with keeper	206.50	18.40

In Table III, we observe that with increase in area then capacitance increase. So delay and power dissipation are more for other techniques, as compared to proposed with keeper transistor.

TABLE III
Performance metrics for 4-input AND gate

TECHNIQUE	DELAY(0.1ns)	POWER(μW)
Keeper transistor	1.737	1076.3
Twin transistor	1.660	912.672
Isolated noise tolerant	1.53	705.582
Proposed	1.579	484.056
Proposed with keeper	1.374	696.834

VII. CONCLUSION

We present a new noise-tolerant dynamic circuit technique. The noise immunity curves and ANTE – delay quotient show that this technique improves the noise immunity with less performance degradation than existing ones for AND gates. The power consumption also reduced.

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