

## **Design and realisation of Low leakage 1-bit CMOS based Full Adder Cells for Mobile Applications**

Padma sai .Y<sup>1</sup>, Rajesh.K<sup>2</sup>

<sup>1</sup>working as professor at vnrvjiet, Hyderabad

<sup>2</sup>Pursuing Mtech at vnrvjiet, Hyderabad

---

**Abstract:** For the most recent CMOS feature sizes (e.g., 180nm), leakage power dissipation has become an overriding concern for VLSI circuit designers. As technology scales into the nano meter regime leakage power and noise immunity are becoming important metric of comparable importance to active power, delay and area for the analysis and design of complex arithmetic and logic circuits. In this project, low leakage 1-bit full adder cells are proposed for mobile applications. Noise immunity has been carefully considered since the significant threshold current of the low threshold voltage transition becomes more susceptible to noise. Since, Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition. The vast use of this operation in arithmetic functions attracts a lot of researcher's attention to adder for mobile applications. In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells. Therefore a new transistor resizing approach for 1-bit full adder cells to determine the optimal sleep transistor size which reduce the leakage power has been proposed. The simulation results depicts that the proposed design also leads to efficient 1-bit full adder cells in terms of standby leakage power. In order to verify the leakage power, various designs of full adder circuits are simulated using DSCH, Micro wind and Virtuoso (Cadence).

**Keywords:** Low leakage power; Noise Margin; Ground bounce noise; Sleep transistor; Sleep method; Stack method; Dual stack method and Adder cell.

---

### **I. Introduction**

Adders are heart of computational circuits and many complex arithmetic circuits are based on the addition. The vast use of this operation in arithmetic functions attracts a lot of researcher's attention to adder for mobile applications. In recent years, several variants of different logic styles have been proposed to implement 1-bit adder cells. These adder cells commonly aimed to reduce power consumption and increase speed. These studies have also investigated different approaches realizing adders using CMOS technology. For mobile applications, designers have to work within a very tight leakage power specification in order to meet product battery life and package cost objectives. The designer's concern for the level of leakage current is not related to ensuring correct circuit operation, but is related to minimize power dissipation. For portable electronic devices this equates to maximizing battery life. For example, mobile phones need to be powered for extended periods (known as standby mode, during which the phone is able to receive an incoming call), but are fully active for much shorter periods (known as talk or active mode, while making a call).

When an electronic device such as a mobile phone is in standby mode, certain portions of the circuitry within the electronic device, which are active when the phone is in talk mode, are shut down. These circuits, however, still have leakage currents running through them, even though they have been de-activated. Even if the leakage current is much smaller than the normal operating current of the circuit. The leakage current depletes the battery charge over the relatively long standby time, whereas the operating current during talk time only depletes the battery charge over the relatively short talk time. As a result, the leakage current has a disproportional effect on total battery life. This is why building low leakage adder cells for mobile applications are of great interest.

Shortening the gate length of a transistor increases its power consumption due to the increased leakage current between the transistors source and drain when no signal voltage is applied at the gate. In addition to the sub threshold leakage current, gate tunneling current also increases due to the scaling of gate oxide thickness. Each new technology generations results nearly a 30x increase in gate leakage. The leakage power is expected to reach more than 50% of total power in sub 100nm technology generation. Hence, it has become extremely important to develop design techniques to reduce static power dissipation during periods of inactivity.

The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. On the other hand, there are several techniques to reduce leakage power. Power gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground (called virtual ground). This device is turned off in the sleep mode to cut-off the

leakage path. It has been shown that this technique provides a substantial reduction in leakage at a minimal impact on performance and further peak of ground bounce noise is possible with proposed novel technique with improved staggered phase damping technique.

In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this technology trend, transistor leakage power has increased exponentially. As the feature size becomes smaller, shorter channel lengths result in increased subthreshold leakage current through a transistor when it is off. Low threshold voltage also results in increased subthreshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power consumption for current and future silicon technologies.

There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique. We propose a new approach, thus providing a new choice to low-leakage power VLSI designers. Previous techniques are summarized and compared with our new approach presented in this project.

The advent of a mobile computing era has become a major motivation for low power design because the operation time of a mobile device is heavily restricted by its battery life. The growing complexity of mobile devices, such as a cell phone with a digital camera or a personal digital assistant (PDA) with global positioning system (GPS), makes the power problem more challenging. Dynamic power consumption was previously a major concern for chip designers since dynamic power accounted for 99% or more of the total chip power. However, as the feature size shrinks, static power, which consists mainly of subthreshold and gate-oxide leakage power, has become a great challenge for current and future technologies. The main reason is that leakage current increases exponentially as the feature size shrinks. Based on the International Technology Roadmap for Semiconductors (ITRS), Kim et al. report that subthreshold leakage power dissipation of a chip will exceed dynamic power dissipation at the 65nm feature size [1][2]. Techniques for leakage power reduction can be grouped in two categories: state-preserving techniques where circuit state (present value) is retained and state-destructive techniques where the current boolean output value of the circuit might be lost [1]. A state-preserving technique has an advantage over a state destructive technique in that with a state-preserving technique the circuitry can resume operation at a point much later in time without having to somehow regenerate state. Our new design technique, which we call the "sleepy stack" technique, retains data during sleep mode while providing reduced leakage power consumption at a cost of slightly increased delay. Furthermore, the sleepy stack approach can be applicable to single- and dual-threshold voltage technologies. The sleepy stack approach delivers a new choice to designers to implement low leakage- power circuits that retain state.

## **II. Proposed Full Adder Circuits**

Recently, power dissipation has become an important concern and considerable emphasis is placed on understanding the sources of power and approaches to dealing with power dissipation [3]. Static logic style gives robustness against noise effects, so automatically provides a reliable operation. Pseudo NMOS and Pass-transistor logic can reduce the number of transistors required to implement a given logic function. But those suffer from static power dissipation. Implementing Multiplexers and XOR based circuits are advantageous when we implement by the pass transistor logic [4]. On the other hand, dynamic logic implementation of complex function requires a small silicon area but charge leakage and charge refreshing are required which reduces the frequency of operation. In general, none of the mentioned styles can compete with CMOS style in robustness and stability [4], [13].

Fig. 1 shows the conventional CMOS 28 transistor adder [12]. This is considered as a Base case throughout this paper. All comparisons are done with Base case. The CMOS structure combines PMOS pull up and NMOS pull down networks to produce considered outputs.

Transistor sizes are specified as a ratio of Width/Length (W/L). The sizing of transistors plays a key role in static CMOS style. It is observed in the conventional adder circuit that the transistor ratio of PMOS to NMOS is 2 for an inverter and remaining blocks also followed the same ratios when we considered the remaining blocks as an equivalent inverters. This ratio does not give best results with respect to noise margin and standby leakage power when it is simulated in 90nm process. Modified adder circuits with sizing are proposed in Design1 and Design2 targeting the noise margin, and ground bounce noise.

Further, power gating technique is used to reduce the leakage power, where a sleep transistor is connected between actual ground rail and circuit ground. Ground bounce noise is being estimated when the circuits are connected with a sleep transistor. Further, the peak of ground bounce noise is achieved with a proposed novel technique.

Modified sizing are shown in Fig. 2 and Fig. 4 respectively. The smallest transistor considered for 90nm technology has a width of 120nm and a length of 100nm and gives W/L ratio of 1.2. The W/L ratio of



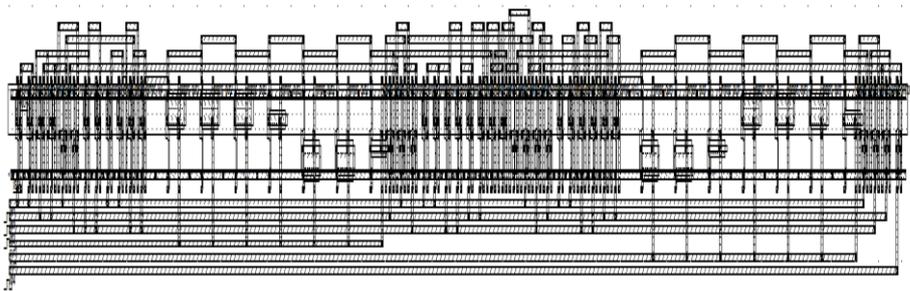


Figure 5. Layout for design-2 full adder circuit

### III. Sleep Method

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. Two components determine the power consumption in a CMOS circuit: Static power: Includes sub-threshold leakage, drain junction leakage and gate leakage due to tunneling. Among these, subthreshold leakage is the most prominent. Dynamic power: Includes charging and discharging power and short circuit power. When technology feature size scales down, supply voltage and threshold voltage also scale down.

Techniques for leakage power reduction can be grouped into two categories: state-preserving techniques; where circuit state is retained and state-destructive techniques; where the current Boolean output value of the circuit might be lost. A state-preserving technique has an advantage over a state destructive technique in that with a state-preserving technique the circuitry can resume operation at a point much later in time without having to somehow regenerate state.

The most well-known traditional approach is the sleep approach. In the sleep approach, a "sleep" PMOS transistor is placed between V<sub>dd</sub> and the pull-up network of a circuit and a "sleep" NMOS transistor is placed between the pull-down network and Gnd (Fig.6). These sleep transistors turn off the circuit by cutting off the power rails. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively.

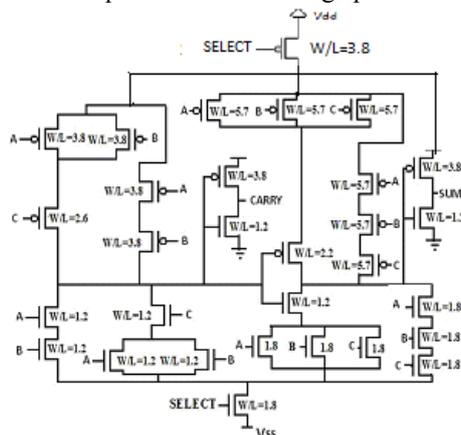


Figure 6. Full Adder circuit using sleep method

### IV. Dual Stack Approach

In dual stack approach (Fig.7), 2 PMOS in the pulldown network and 2 NMOS in the pull-up network are used. The advantage is that NMOS degrades the high logic level while PMOS degrades the low logic level. Sleep transistors in the sleep approach (Fig.6) are sized such that any sleep transistor between V<sub>dd</sub> and a pull-up network takes the size of the largest transistor in the pull-up network, and any sleep transistor between Gnd and a pull-down network takes the size of the largest transistor in the pull-down network. We compare the dual stack approach with Base Case, Design 1, Design 2, Sleep techniques. Thus, we compare five design approaches in terms of leakage power and area.

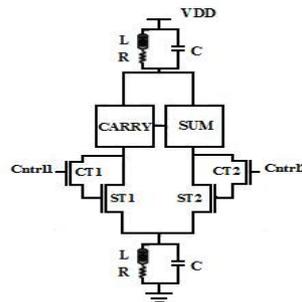


Full Adder circuit	Optimized Power	%Power reduction
Base case	0.594mw	-----
Design-1	0.200mw	66.33%
Design-2	93.377uw	82.21%
Sleep method	74.601uw	87.34%
Dual stack method	58.733uw	90.11%

**Table-1: Performance characteristics of simulated full adder circuits.**

In this thesis, we have presented different ways to reduce the leakage power of one-bit full adder circuits. The same full adder circuit designs i.e., sleep method and Dual stack designs with little modifications as discussed below can be used to reduce the ground bounce noise and further may also reduce the leakage power.

During last one decade various alternatives and improvements of conventional power gating has been proposed to reduce the ground bounce noise during mode transition. In staggered Phase Damping technique [15] during standby-to-active power mode transition, staggered-phase damping delays the activation time of one of the two sleep transistors relative to the activation time of the other one by a time that is equal to half the resonant oscillation period. As a result, noise cancellation occurs once the second sleep transistor turns on due to phase shift between the noise induced by the second sleep transistor hence reduction in settling time. But it is not very effective in reducing the peak noise due to the initial spike. And in another scheme [17], there will be a two stage procedure. In first stage sleep transistor working as diode by turn on the control transistor which is connected across the drain and gate of the sleep transistor. Due to this, drain to source current of the sleep transistor drops in a quadratic manner. This reduces the voltage fluctuation on the ground and power net and it also reduces the circuit wakeup time. In second stage control transistor is off so that sleep transistor works normally. This method is not effective to suppress the overall fluctuations in the ground bounce noise. Therefore, the technique must be adopted to reduce both peak of ground bounce noise and reducing the overall fluctuations in the ground bounce noise. The idea is to combine both the above techniques to further reduce the peak of ground bounce noise and overall power mode transition noise in the proposed technique.



**Figure 10. Proposed novel technique for ground bounce noise reduction.**

Figure10 shows the proposed scheme for peak of ground bounce noise reduction in mode transition. One bit full adders will be taken to apply the proposed technique. One-bit full adder circuit is considered as two cascaded blocks i.e. carry generation block and sum generation block. Separate sleep transistors are added at the bottom of the blocks.

To summarize, since full adder circuits are designed in five different methods, each with its own advantages and disadvantages of power, area, etc., can be used depending up on the requirement of the designer.

### References

- [1] Radu Zlatanovici, Sean Kao, Borivoje Nikolic, "Energy-Delay of Optimization 64-Bit Carry- Lookahead Adders With a 240ps 90nm CMOS Design Example," IEEE J. Solid State circuits, vol.44, no. 2, pp. 569-583, Feb. 2009.
- [2] K.Navi, O. Kavehei, M. Rouholamini, A. Sahafi, S. Mehrabi, N. Dadkhai, "Low-Power and High-Performance 1-bit CMOS Full Adder Cell," Journal of Computers, Academy Press, vol. 3, no. 2, Feb. 2008.
- [3] Rabaey J. M., A. Chandrakasan, B. Nikolic, Digital Integrated Circuits, A Design Perspective, 2nd Prentice Hall, Englewood Cliffs, NJ, 2002
- [4] Pren R. Zimmermann, W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid- State Circuits, vol. 32, pp. 1079-1090, July 1997.
- [5] S.G.Narendra and A. Chandrakasan, Leakage in Nanometer CMO Technologies. New York: Springer-verlag, 2006.
- [6] K.Bernstein et al., "Design and CAD challenges in sub-90nm CMOS technologies," in Proc. int. conf. comput. Aided Des., 2003, pp.129-136.
- [7] "International Technology Roadmap for Semiconductors," Semiconductor Industry Association, 2005. [Online]. Available:<http://public.itrs.net>
- [8] H.Felder and J.Ganger,"Full Chip Analysis of Leakage Power Under Process variations, Including Spatial Correlations," in proc. DAC, pp.523-528, June2005
- [9] Jun Cheol Park and Vincent J. Mooney" Sleepy Stack Leakage Reduction" IEEE transactions on very large scale integration (vlsi) systems, vol.14, no.1. november 2006.

- [10] Harmander Singh, Kanak Agarwal, Dennis Sylvester, Kevin J. Nowka, "Enhanced Leakage Reduction Techniques Using Intermediate Strength Power Gating," IEEE Transactions on VLSI Systems, Vol.15, No.11, November 2007.
- [11] Y.Chang, S.K.Gupta, and M.A.Breuer, "Analysis of ground bounce in deep sub-micron circuits", in proc.15th IEEE VLSI Test symp., 1997, pp.110-116.
- [12] N.West. K.Eshragian, Principles of CMOS VLSI Design: A systems Perspective, Addison-wesley, 1993.
- [13] Suhwan Kim, Chang Jun Choi, Deog-Kyoon Jeong, Stephen V. Kosonocky, Sung Bae Park, "Reducing Ground-Bounce Noise and Stabilizing the Data Retention Voltage of Power-Gating Structures," IEEE transactions on Electron Devices, Vol.55, No.1, January 2008.
- [14] S.Mutoh et al., "1-v power supply high-speed digital circuit technology with multithreshold-voltage CMOS," JSSC, vol.SC- 30, pp.847-854, Aug.1995.
- [15] Charbel J. Akl, Rafic A. Ayoubi, Magdy A. Bayoumi, "An effective staggered phase damping technique for suppressing power-gating resonance noise during mode transition," 10<sup>th</sup> International Symposium on Quality of Electronic Design, pp.116-119, 2009.
- [16] K. Kawasaki et al., "A sub-us wake-up time power gating technique with bypass power line for rush current support," IEEE J. Solid-State Circuits, vol.44, no. 4, pp.146-147, Apr. 2009.
- [17] Ku He, Rong Luo, Yu Wang, "A Power Gating Scheme for Ground Bounce Reduction During Mode Transition," in ICCD07, pp. 388-394, 2007.
- [18] M. V. D. L. Varaprasad, Rohit Bapna, Manisha Pattanaik, "Performance Analysis of Low leakage 1-bit Nano-CMOS Based Full Adder Cells for Mobile Applications," Proceedings of International Conference on VLSI Design & Communication Systems, pp.233-238, January 2010.