

“CMOS Form of Wallace Range Exploitation Domino Logic Full Adder”

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Abstract: *The main objective of this project is to provide new low power solution for very large scale integration (VLSI) designer. Especially, this work focuses on the reduction of power dissipation, which is showing an ever increasing growth with the scaling down of the technology. Various technologies at the different level of the design process have been implemented to reduce power dissipation at the circuit, architectural and system level. It permits for commencement of analysis during a procedure block before its analysis section begins, and quickly performs a final analysis as shortly because the inputs are valid. This dynamic logic family is best suited to arithmetic circuits as a result of the important path is created of a protracted chain of cascaded inverting gates. Because the major advantage of this logic that is higher speed is discovered upon cascading, it's most fitted for arithmetic circuits using submicron technology.*

Keyword: *Domino Logic, Wallace Multiplier, Power Dissipation, Full Adder, CMOS Logic*

I. Introduction

Digital electronic computations started with the introduction of vacuum tubes. During this era of electron tube primarily based laptop, machines like ENIAC and UNIVAC were developed. It was comprised of 18,000 vacuum tubes and was eighty feet long with many feet of height and dimension. This clearly tells concerning the low integration density drawback of vacuum tubes. Thus implementation of larger engines became economically and much impossible. The invention of the semiconductor unit, followed by the introduction of the bipolar semiconductor unit junction rectifier to the primary successful IC logic family, TTL (Transistor-Transistor Logic). TTL had the Advantage, of a better integration density and on this;

The primary computer circuit revolution was primarily based. Ultimately, the big power consumption per gate place a restriction on the quantity of devices which will be dependably integrated on one chip. Next was the flip of the MOS digital computer circuit approach. at the start MOS ICs were enforced in PMOS solely. As electrons have higher quality than holes, NMOS was most popular later. The second age of the digital computer circuit revolution began with the introduction of microprocessors by Intel (4004) and 1974 (8080). These processors used NMOS-only logic, with higher speed relative to the PMOS logic. But later, NMOS-only logic started plagued by a similar problem: power consumption. Finally the balance a tilt towards the CMOS technology, wherever we have tendencies to still are nowadays.

Power consumption considerations are once more turning into dominant in CMOS style in addition. Sadly, this point there doesn't appear to be a replacement technology developing any time shortly. thus what we will do is create slight modifications within the logic vogue thus on improve speed and scale back power consumption just in case of CMOS, addition of one input will increase the device count by a pair of and so will increase the propagation delay. New logic designs were developed to attenuate the propagation delay and chip space.

Thus kinds of CMOS circuits are searched to supplement the static CMOS logic that may be utilized in special applications. Then Dynamic logic came into image that works as per clock. Its higher speed in addition as lower power however suffers from cascading downside that diode to Domino and NORA logic designs. Wallace high-speed multipliers use full adders and 0.5 adders in their reduction part. 0.5 adders don't scale back the quantity of partial product bits. Therefore, minimizing the quantity of 0.5 adders utilized in a multiplier factor reduction can scale back the complexity. A modification to the Wallace reduction is given that ensures that the delay is that the same as for the traditional Wallace reduction. The changed reduction methodology greatly reduces the quantity of half adders; manufacturing implementations with 80% fewer half adders than normal Wallace multipliers, with a very slight increase within the variety of full adders.

II. Literature survey

Gaetano Palumbo, Melitia Pennisi, Massimo Alioto [1] proposes a simple approach to reduce delay variations in domino logic gates is proposed. In particular, a simple modified keeper is proposed to reduce the loop gain while keeping the same silicon area, noise margin, and nominal performance.

Rahul Singh, Gi-Moon hong, Sulwan Kim [2] present new footer voltage feedforward domino (FVFD) and static-switching pulse domino (SSPD) designs for dynamic multiplexers. Both improve noise tolerance, and both reduce the switching power by limiting the voltage swing on the large bitline capacitance through the introduction of dual dynamic nodes.

Skyler Weaver, Benjamin Hershberg, Nima Maghari [3] proposes A low-power synthesizable analog-to-digital converter (ADC). By cascading many digital-like domino-logic cells whose propagation delay is influenced by an analog input voltage, a digital value is obtained at the end of the allowed ripple period by determining the number of cells that the ripple passed through.

Ali Paravi, Mohammad Asyaei [4] proposes In this paper, a new domino circuit is proposed, which has a lower leakage and higher noise immunity without dramatic speed degradation for wide fan-in gates. The technique which is utilized in this paper is based on comparison of mirrored current of the pull-up network with its worst case leakage current. The proposed circuit technique decreases the parasitic capacitance on the dynamic node, yielding a smaller keeper for wide fan-in gates to implement fast and robust circuits.

Massimo Alioto, Gaetano Palumbo, Melita Pennisi[6] In this paper, the effect of process variations on delay is analyzed in depth for both static and dynamicCMOSlogic styles. Analysis allows for gaining an insight into the delay dependence on fan-in, fan-out, and sizing in sub-100-nm technologies.

Charbel J. Aki and Magdy A. Bayoumi [7] The high switching activity of wide fan-in dynamic domino gates introduces significant power overhead that poses a limitation on using these compact high-speed circuits. This paper presents a new limited-switching clock-delayed dynamic circuit technique, called SP-Domino, which achieves static-like switching behavior, while maintaining the low-area and high-performance characteristics of wide fan-in dynamic gates.

Themistoklis Haniotakis, Yiorgos Tsiatouhas, Dimitri Nikolos [8] Domino CMOS circuits are an option for speeding up critical units. An inherent problem of Domino logic is that under specific input conditions the charge redistribution between parasitic capacitances at internal nodes of a circuit can violate the noise margins and cause erroneous responses at the output. The dominant solution to this problem is the multiple precharging of the gate's internal nodes.

Amir Amirabadi, Ali Afzali Kusha, Yousof mortazari & Mehrdad Nourani [9] In this paper, efficient clock delayed domino logic with variable strength voltage keeper is proposed. The variable strength of the keeper is achieved through applying two different body biases to the keeper. The circuits used to generate the body biases are called capacitive body bias generator and cross-coupled capacitive body bias generator. Compared to a previous work, the body bias generator circuits presented in this paper are simpler and do not require double or triple power supply while consuming less area and power.

III. Related Work

In this section, we have a tendency to principally survey the various techniques wont to scale back escape power in 4*4 Wallace tree number. The 4*4 Wallace tree number with full adder methodology replaces the total adders within the place of half adders. Hence the overall escape power is reduced .The most of typical ways think about reducing static power and dynamic power dissipation. The dynamic power is reduced by victimization totally different domino logic style.

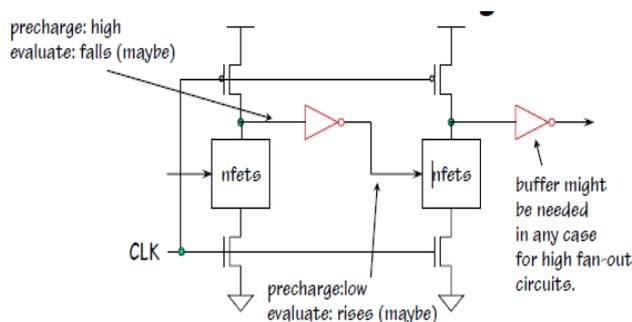


Fig (1): CMOS Domino logic.

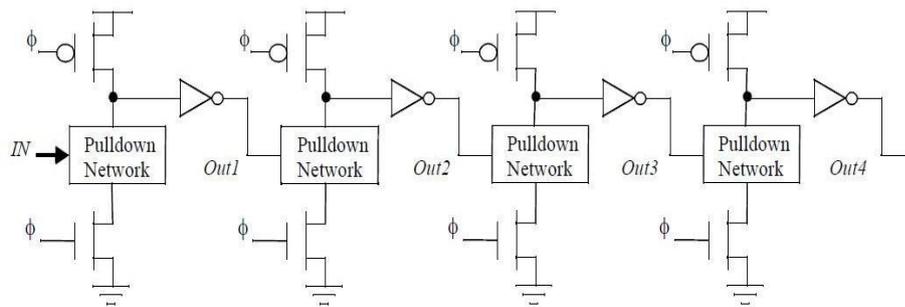
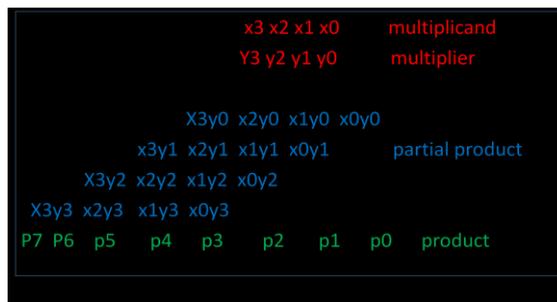


Fig (2): cascading of domino logic

Partial product



The above shows the partial product in this 4*4 bit multiplication $x_0 x_1 x_2 x_3$ is multiplicand and $y_0 y_1 y_2 y_3$ is multiplier. And get the partial product p_0 to p_7 .

IV. Schematic & Results

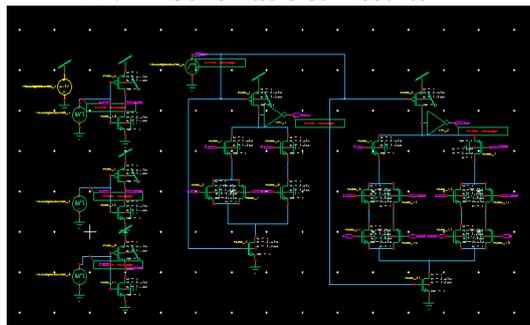


Fig (3): Schematic of AND gate

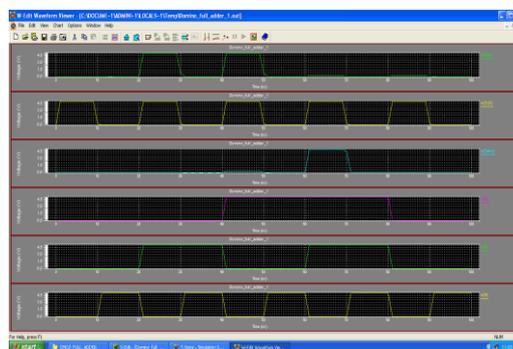


Fig (4): Waveform of AND gate

The above fig shows the schematic and simulation of AND gate. At every positive half cycle circuit gives correct operation of arithmetic gate.

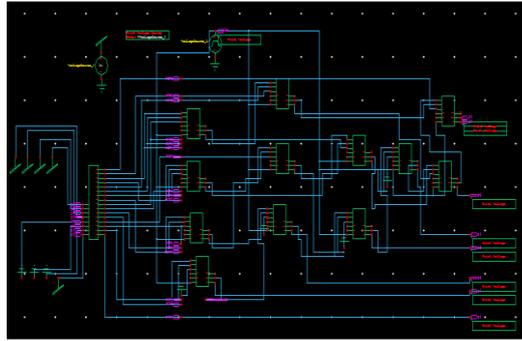


Fig (5): Schematic of Wallace tree multiplier



Fig (6): Waveform of Wallace multiplier

The above fig shows the schematic and simulation of Wallace multiplier. At every positive half cycle circuit gives correct operation of arithmetic gates.

Dynamic logic came to picture to reduce the area and gate complexity of CMOS. It reduced the device count and increased the speed. As there is no direct path, power consumption is very low. But there is cascading problem in dynamic logic which is removed in Domino and NORA logic styles.

V. Proposed Work

A 4*4 Wallace tree multiplier factor is intended mistreatment current comparison primarily based domino logic full adders. 4*4 Wallace multiplier factor has twelve full adders, wherever of these full adders are replaced by current comparison primarily based domino logic full adders. By these adders dynamic power dissipation within the multiplier factor is reduced specified 1/2 the entire outflow power within the 4*4 Wallace tree multiplier factor is reduced. The idea of current comparison primarily based domino logic is shown in figure. In this logic pull down network implements the logical perform and it's separated from the keeper semiconductor unit by current comparison stage. This stage compares the pull up network current with the worst case outflow current.

The Multipliers play a serious role in arithmetic operations within the digital signal process application. presently the necessity for low power multiplier factor has been redoubled owing to the increasing demand for transportable and mobile systems. C.S. Wallace advised a quick multiplier factor throughout 1964 with combination of [*fr1] adders and full adders. The outflow power is high during this style. Later several researches were created on these multipliers. Among them the multiplier factor with full adders style had showed fast development in reducing outflow power in 4*4 Wallace multipliers with full adders by domino logic.

VI. Result

In Dynamic logic, problem arises when cascading one gate to the next. The precharge "1" state of the first gate may cause the second gate to discharge prematurely, before the first gate has reached its correct state. This uses up the "precharge" of the second gate, which Cannot be restored until the next clock cycle, so there is no recovery from this error.

In order to cascade dynamic logic gates, one solution is Domino Logic, which inserts an ordinary static inverter between stages. While this might seem to defeat the point of dynamic logic, since the inverter has a pFET (one of the main goals of Dynamic Logic is to avoid pFETs where possible, due to speed), there are two reasons it works well. First, there is no fanout to multiple pFETs. The dynamic gate connects to exactly one inverter, so the gate is still very fast. And since the inverter connects to only nFETs in dynamic logic gates, it too is very fast. Second, the pFET in an inverter can be made smaller than in some types of logic gates.

In Domino logic cascade structure of several stages, the evaluation of each stage ripples the next stage evaluation, similar to a domino falling one after the other. Once fallen, the node states cannot return to "1" (until the next clock cycle) just as dominos, once fallen, cannot stand up, justifying the name Domino CMOS Logic. It contrasts with other solutions to the cascade problem in which cascading is interrupted by clocks or other means.

Table: Results of Full adder & Multiplier

No. of Transistor	Voltage	Current	Power
Domino full adder	3v	361 p	1.085 n
Wallace Multiplier	3v	14.4798 m	43.439 m

VII. Conclusion

Propagation delay and power consumption are comparable for small circuits (i.e. circuits with less no. of inputs) in CMOS, pseudo NMOS, Domino and FTL because the device count is low and structure is not cascaded. HS0 LP0 family is best suited to applications in circuits with long chain of cascaded inverting structures as the value attained by the output node is V_{th} after certain no. of stages which is neglected in initial stages.

Power delay product of HS0 is greater and of LP0 is lesser than that of domino. So, LP0 is the most optimized logic family out of three logic families compared here. Wallace tree multiplier result in fast multiplication and low power design.

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