

## Generation of Variable Duty Cycle PWM using FPGA

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**Abstract:** Field Programmable Gate Arrays (FPGA) provide very good hardware design flexibility. This paper specifies the generation of PWM signals for variable duty cycles using VHDL. Pulse Width Modulation found in large number of applications as a voltage controller. It is used in controlling output voltage of inverter in most of the applications. PWM has a fixed frequency and a variable voltage. Voltage value changes from 0V to 5 V. The advantage of this method is that it is used to generate High-frequency variable duty cycle PWM output. The VHDL code is written and synthesized using Xilinx ISE 10.1. Behavioral simulation was performed and the results are verified by downloading the code into SPARTAN 3 FPGA and observed in ISE simulator.

**Key Words:** FPGA, ISE, PWM, VHDL.

### I. Introduction

Pulse Width Modulation (PWM) is an integral part of almost all embedded systems. It is widely used as a control technique in most of the power electronic applications [1] like DC/DC, DC/AC, etc. PWM Inverters are one of those power converters which particularly use PWM concept for its operation. Recently PWM inverters have great popularity in industrial applications because of their superior performance. There are basically two PWM techniques –Analog and Digital Techniques. The disadvantages of these analog methods [2] and [3] are that, they are easily affected by noise and they change with respect to voltage and temperature. Digital methods are good for designing variable PWM signals. They are very flexible and less sensitive to environmental noise [2]. Easy to construct and can be implemented in very fast manner.

Reprogramming capability of FPGA makes it suitable to develop any design using FPGA [1]. FPGA reduces the design implementation time. FPGA based designs proves less costly and hence they are economically suitable for small designs [1]. The PWM signal is not constant, the main parameter is a duty cycle D that is a part of PWM period, the equation (1) describes the duty cycle as the following:

$$\text{Duty cycle (D)} = \frac{\text{Integer Value of N bit word}}{2^N} \quad (1)$$

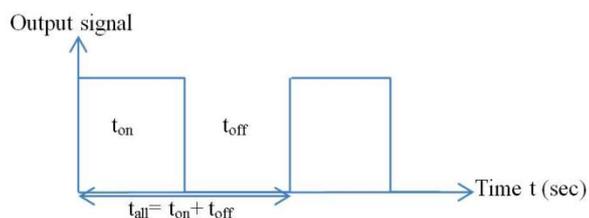
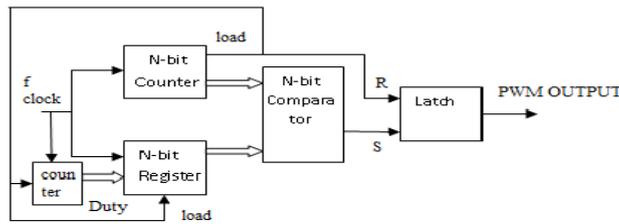


Fig.1 PWM with 50 % duty cycle

### II. Proposed Pwm Architecture

To produce the input data to generate the PWM using high speed N-bit free running counter, whose output is compared with register output and stores desired input duty cycle with the help of comparator. The comparator output is set equal to 1 when both these values are equal. This comparator output is used to set RS latch. The overflow signal from counter is used to reset RS latch. The output of RS latch gives the desired PWM output. This overflow signal is also used to load new N-bit duty cycle in Register. PWM has a fixed frequency and a variable voltage. This voltage value changes from 0V to 5 V. The basic PWM generates the signals, which gives the output of PWM, requires a comparator that compares between two values. The first value represents the square signal generated by N bit counter and the second value represents the square signal which contains the information about duty cycle. Counter generates the load signal whenever there is an overflow. Once load signal becomes active, the register loads the new duty cycle value. Load signal is used to reset the latch also. Latch output is a PWM signal. This is varying with change in duty cycle value.



**Fig.2** Block diagram of PWM with variable duty cycle

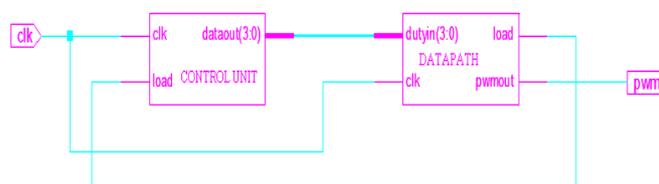
The block diagram of the proposed architecture is shown in Fig. 2. The system input is an N-bit data word, depending on the required PWM duty cycle value, which can be easily achieved through FPGA. The N-bit register output, containing the N-bit data input, is compared with the output value of an N-bit free-running synchronous counter, in terms of a comparator. When these two values become equal, the comparator output is used to reset the R/S latch output, which produces the PWM wave. The R/S latch output is set when the counter reaches an overflow condition at the end of a PWM period. Counter “Overflow” signal is used to load the new duty cycle value to the PWM generator input register. The reference frequency can be supplied from 5 to 10 MHz from FPGA board.

### III. FPGA Results

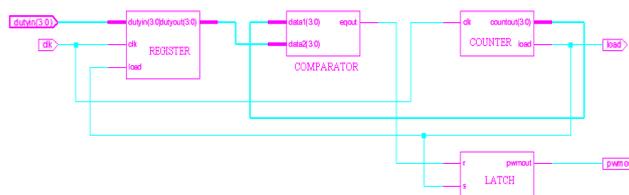
The PWM with variable duty cycle is designed and simulated using VHDL. To implement the proposed architecture, Spartan 3 FPGA is used. ISE 10.1 Simulator is used for synthesis, translation, mapping and place & route process. The FPGA resource utilization is listed in table 1. The RTL schematic generated by ISE simulator is shown in figure 3 and 4. This will clearly illustrate the integration of the work.

**Table 1:** Resource Utilization

Logic utilization	Used	Available	Utilization
Number of Slices	13	768	1%
Number of Slice Flip Flops	20	1536	1%
Number of 4 input LUTs	21	1536	1%
Number of IOs	2	-	
Number of bonded IOBs	2	124	1%
Number of GCLKs	1	8	12%



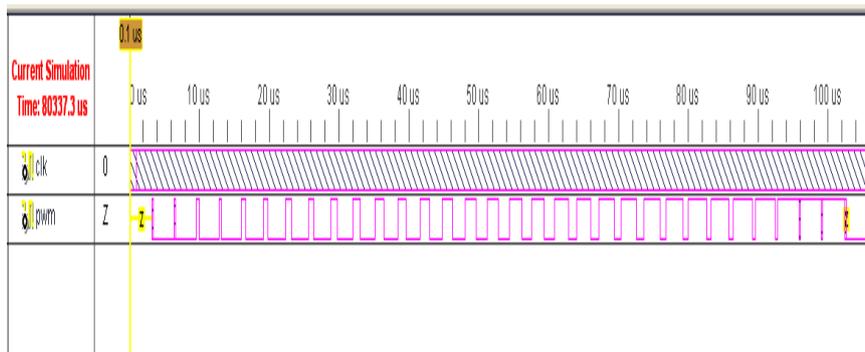
**Fig. 3** Top level RTL schematic



**Fig. 4** RTL Schematic of data path unit

#### IV. Simulation Results

A VHDL program has been written for the proposed architecture and synthesized and simulated using Xilinx ISE Simulator.



#### V. Conclusion

Here we discussed regarding generation of PWM signals with varying duty cycle using VHDL code and tested on FPGA. A FPGA SPARTAN3 board is used as hardware and ISE10.1 XILINX is used as software. The comparator is necessary to compare between the data available in register and counter to generate suitable PWM signals. The generated PWM signals have a fixed frequency (10 MHz) depended on the frequency of square wave, and a variable duty cycle that changes from 0% to 100%. But the frequency can be changed on FPGA board based on our requirement, without changing anything in program. These signals can be used to drive a BLDC motor.

#### References

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