

A new design 6T Full Adder Circuit using Novel 2T XNOR Gates

Krishna Chandra¹, Rajeev Kumar², Shashank Uniyal³, Vishal Ramola⁴

M.Tech. Student of VLSI Design Department, Faculty of Technology, University Campus, UTU Dehradun, UK India^{1&3}

Assist. Prof. Electronics Department, UCST Dehradun, UK India²

Assist. Prof. VLSI Design Department, Faculty of Technology, University Campus, UTU Dehradun, UK India⁴

Abstract: Exclusive-NOR (XNOR) gates are important in digital circuits. This paper proposes the novel design of 2T XNOR gate using pass transistor logic. The proposed circuit utilizes the least number of transistors and no complementary input signal is used. The design has been compared with earlier designed XNOR gates and a significant improvement in silicon area and power-delay product has been obtained against 3T XNOR gate. In this paper we designed a new 6 transistor full adder using the proposed two-transistor XNOR gate. The performance has been investigated using 0.18 μ m Technology and evaluated by the comparison of the simulation result obtain from TSPICE.

Keywords: XNOR gate, Full adder, Power, Delay, Power Delay Product.

I. INTRODUCTION

Since the battery technology available does not advance at the same rate as the microelectronics technology, IC designers have encountered more constraints: high speed, small silicon area, and at the same time, low power dissipation. Hence, the research of establishing high performance adder cells is becomes feverish. The design of 1 bit full adders which forms the basic building blocks of all digital VLSI circuits has been undergoing to minimizing the transistor, minimizing the power consumption and increasing the speed [6-12].

Circuit realization for low area has become an important issue with the growth of integrated circuit towards very high integration density and high operating frequencies. Due to the important role played by XNOR gate in various circuits especially in arithmetic circuits, optimized design XNOR circuit to achieve small size and delay is needed. The primary concern to design XNOR gate is to obtain low power consumption and delay in the critical path and full output voltage swing with low number of transistors to implement it. A survey of literature reveals a wide spectrum of different types of XNOR gates that have been realized over the years. The early designs of XNOR gates were based on either 4 transistors [3] or 3 transistors [4] that are conventionally used in most designs.

The paper is organized as follows: in Section II, previous work is reviewed. Subsequently, in section III, the proposed design of XNOR gate and full adder are presented. In section IV, the simulation results are given and discussed. The comparison and evaluation for proposed and existing designs are carried out. Finally a conclusion will be made in the last section.

II. PRELIMINARIES

(A) Logic Equations for the Proposed XNOR gate

The XNOR gate functions are shown in Table 1 and denoted by this \square . The logic expression for XNOR is

$$A \square B = A'B' + AB \quad (1)$$

Table I. XNOR Gate Function

B	A	XNOR
0	0	1
0	1	0
1	0	0
1	1	1

(B) Logic Equations for the Proposed Full Adders

The logical function of the 1 bit full adder operation equations presented below can be stated as follows: given the inputs A , B and C_{in} which calculate two 1-bit outputs Sum , for sum and C_{out} , for carry out.

$$SUM = A \oplus B \oplus C \quad (2)$$

$$C_{out} = A(A \oplus B) + C(\overline{A \oplus B}) \quad (3)$$

Jyh-Ming Wang et al. [2] to design 4 transistor XNOR gate as shown in fig.1. This design no longer need complementary signal inputs and only one poor signal level on output end. Author define the defect property of a 4-transistor type is that the output level will be higher or lower than the normal case by the voltage $|V_{th}|$, the threshold voltage of MOS. Under the condition of $|V_{th}|$ value, this poor level can still drive the inverter and make the inverter action correct.

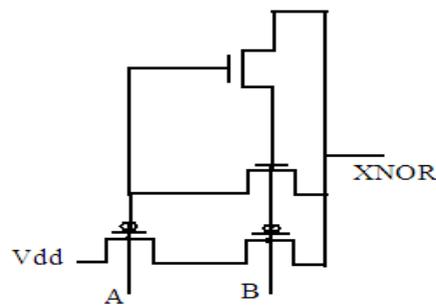


Figure.1-4T XNOR Gate [2]

Hung Tien Bui et al. [3] to design 4 transistor XNOR gate as shown in fig. 2 that is named Groundless, because there is no ground and show the better performance previous design XNOR gate.

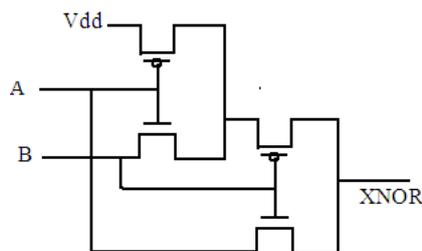


Figure.2-4T XNOR Gate [3]

J. Wang et al. [5] to design 4 transistors XNOR gate as shown in fig 3. It is inverter base XNOR gate.

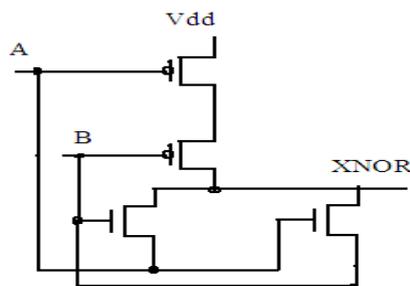


Fig.3 4T XNOR Gate [5]

Sreehari Veeramachaneni et al. [4] to design XNOR gates using 3 transistors (3-T) shown in fig 4. 3 transistors has a small delay of mere 1 transistor (1-T). However, for certain input combinations, they give bad

output logic levels. Author manipulates the (W/L) ratios of PMOS and NMOS transistors to solve this problem until an acceptable logic level is restored.

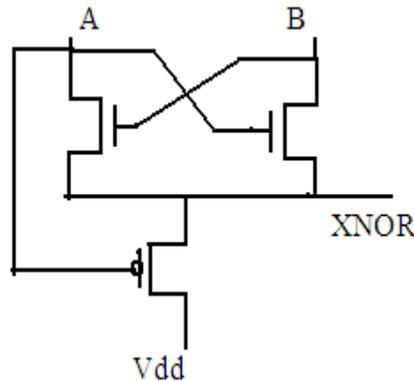


Figure.4 3T XNOR Gate [4]

III. Proposed Circuits

(A) 2T XNOR Gate

On the 2-transistor design, the new proposed structures require non-complementary inputs and their output will be nearly perfect. The configurations are shown in Fig. 4. For the XNOR function, the output signal in the case of $AB = 00, 01, 11$ will be complete. While $AB = 10$, NMOS will be on and pass the poor “HI” signal level to the output end.

The input combinations, they give bad output logic levels but we manipulate the (W/L) ratios of PMOS and NMOS transistors to solve this problem until an acceptable logic level is restored.

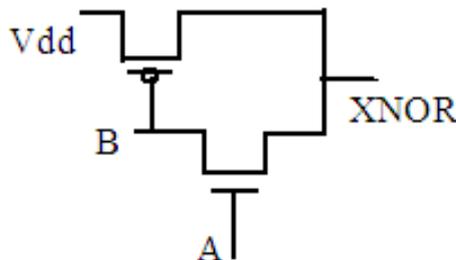


Figure.5-Proposed 2T XNOR Gate

(B) The Proposed 6T Full Adders using 2T XNOR gate

As shown in Fig. 6, the 6-T full adder contains three modules—two 2-T XNOR gates and a 2-transistor multiplexer (2-T MUX) as shown in Fig. 6. The Sum and Cout can be obtained using (2) and (3) respectively. Owing to the appealing traits of a small number of transistors and a mere 2-transistor (2-T) delay, it can work at high speed with low power dissipation. By using proposed 2T XNOR gates we became able to minimize the transistor count of the full adder and subsequent decrease in power and delay.

The sum output is basically obtained by a cascaded XNOR of the three inputs in accordance with above mentioned equation (2). The carry output is obtained in accordance with above mentioned equation (3). The final sum of the products is obtained using a wired XNOR logic. The W/L ratios of transistors M1-M3 are $70/18 \mu\text{m}$ as the corresponding in figure 6. The W/L ratios of transistors M2 and M4 are same taken as $2/90 \mu\text{m}$. The W/L ratios of transistors M5 is taken as $4/18 \mu\text{m}$ and M6 is taken as $0.1/0.18 \mu\text{m}$. It is quite evident from figure 6 that two stage delays are required to obtain the sum output and at most two stage delays are required to obtain. The calculated power and delay is shown in Table II. We can observe from this table that how much delay and power has been reduced by using proposed 2T XNOR gate. The simulation waveform of proposed 6T full adder is shown in figure 8.

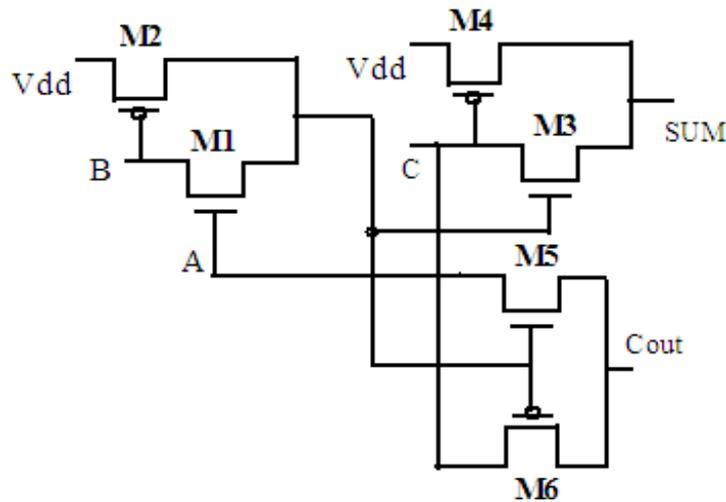


Figure 6. 6T full adder

IV. Simulation Environment

The proposed 2T XNOR gates, three previous 4T, 3T XNOR gate, three input XNOR gate and 1-bit full adders are simulated using Tspice in Tanner Tools. All the results are obtained in 180nm CMOS process technology with a 5V supply voltage. In order to establish an impartial simulation circumstance, authors prefer the input patterns in Fig. 8 and 9, which covers every possible inputs combination of *A*, *B* and *Cin*.

The delay has been measure between the time when the changing input reaches 50% of voltage level to the time it output reaches 50% of voltage level for both rising and fall transition for Sum and Cout. The power delay product (PDP) is measured as the product of the average delay and the average power. The output waveform of the proposed circuit is shown in fig 7 and 8.

The comparison of the different XNOR gates and Full adders are shown in table.II according to their transistor count, Propagation delay, power dissipation and power delay product.

Table.II: Comparison of existed XNOR gate with proposed one in terms of different.

Circuits	Tran-sistor	Propagation Delay (&)	Power Consumption (S)	PDP
Fig.1 (XNOR)	4	3.41	0.072	0.24
Fig.2(XNOR)	4	33.45	0.013	0.43
Fig.3 (XNOR)	4	6.26	0.009	0.056
Fig.4 (XNOR)	3	290	3.89	1128.10
Fig.5 (XNOR) (Proposed)	2	89	3.37	299.93
Fig.6 full adder (sum)	6	2×10^4	2.29	4.45×10^4
Fig.6 full adder (carry)	6	2.99×10^4	2.29	6.84×10^4
Units &=pico				

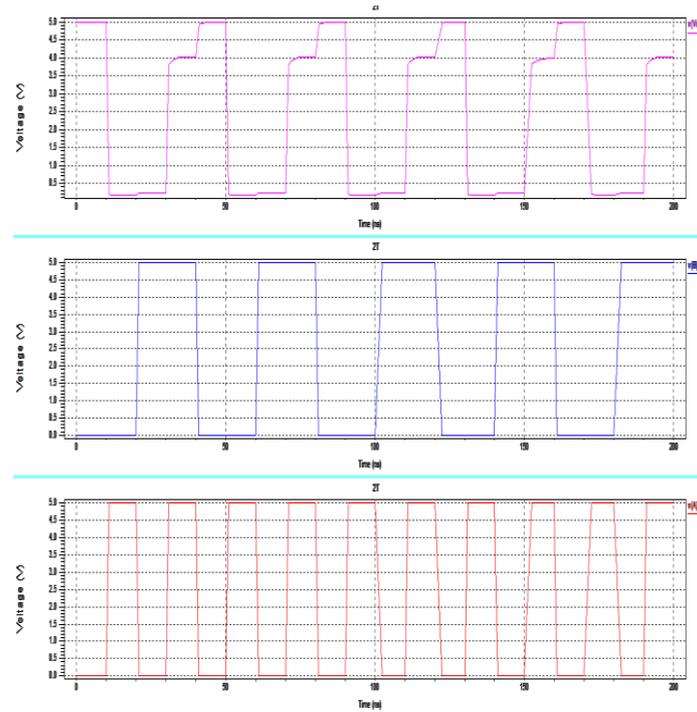


Figure 7. Simulation waveform of 2T XNOR gate in 0.18 μ m Technology

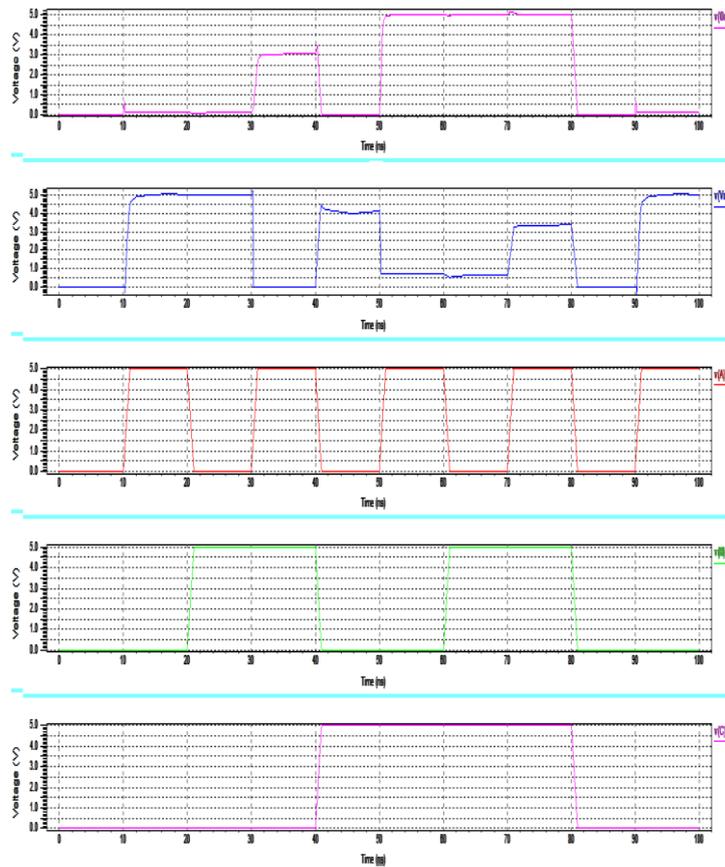


Figure 8. Simulation waveform of 6T Full adder in 0.18 μ m Technology

V. Conclusions

In this paper, we proposed the new design 2T XNOR gate circuit is based on the Pass Transistor Logic. The performances of this circuit have been compared to earlier designed XNOR gate delay, power dissipation and Power Delay Product (PDP). The current work proposes the design of a 6T full adder using a novel 2T XNOR gate. The newly designed full adder processes the merits of small delay, small Power-Delay product, and area saving due to lower transistor counts and special structures.

References

- [1] N. Weste and K. Eshraghian, Principles of CMOS VLSI Design, Reading, MA: Addison-Wesley, 1985
- [2] W. Jyh Ming, F. Sung-Chuan, and F. Wu-Shiung, "New efficient designs for XOR and XNOR functions on the transistor level," Solid-State Circuits, IEEE Journal of, vol. 29, pp. 780-786, 1994.
- [3] H. T. Bui, A. K. Al-Sheraidah, and Y. Wang, "New 4-transistor XOR and XNOR designs," Tech. Rep., Florida Atlantic Univ., Boca Raton, 1999.
- [4] Sreehari Veeramachaneni and Hyderabad, "New improved 1-bit adder cells", CCECE/CCGEI, Niagara Falls, Canada, May 5-7 2008, pp. 735-738.
- [5] J. Wang, S. Fang, and W. Feng, "New efficient designs for XOR and XNOR functions on the transistor level," IEEE J. Solid-State Circuits, vol. 29, pp. 780-786, July 1994
- [6] H.T. Bui, Y. Wang, Y. Jiang, "Design and analysis of 10-transistor full adders using novel XOR-XNOR gates," in Proc. 5th Int. Conf. Signal Process., vol. 1, Aug. 21-25, 2000, pp. 619-622.
- [7] H. T. Bui, Y. Wang, and Y. Jiang, "Design and analysis of low-power 10-transistor full adders using XOR-XNOR gates," IEEE Trans. Circuit Syst. II, Analog Digit. Signal Process., vol. 49, no. 1, Jan. 2002, pp. 25-30.
- [8] A. M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 10, no. 1, Feb. 2002, pp. 20-29.
- [9] K.-H. Cheng and C.-S. Huang, "The novel efficient design of XOR/XNOR function for adder applications," in Proc. IEEE Int. Conf. Elect., Circuits Syst., vol. 1, Sep. 5-8, 1999, pp. 29-32.
- [10] H. Lee and G. E. Sobelman, "New low-voltage circuits for XOR and XNOR," in Proc. IEEE Southeastcon, Apr. 12-14, 1997, pp. 225-229.
- [11] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltage swing nodes," in Proc. IEEE Worksh. Signal Process. Syst., Oct. 20-22, 1999, pp. 713-722.
- [12] G.A. Ruiz, M. Granda, "An area-efficient static CMOS carry-select adder based on a compact carry look-ahead unit", Microelectronics Journal, Vol. 35, No. 12, 2004, pp. 939-944.
- [13] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, July 1997, pp. 1079-90.
- [14] N. Zhuang and H. Wu, "A new design of the CMOS full adder," IEEE J. Solid-State Circuits, vol. 27, no. 5, May 1992, pp. 840-844.
- [15] E. Abu-Shama and M. Bayoumi, "A new cell for low power adders," in Proc. Int. Midwest Symp. Circuits Syst., 1995, pp. 1014-1017.
- [16] A. M. Shams and M. Bayoumi, "A novel high performance CMOS 1-bit full adder cell," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 47, no. 5, May 2000, pp. 478-481.
- [17] R. Shalem, E. John, and L. K. John, "A novel low-power Energy recovery full adder cell," in Proc. Great Lakes Symp. VLSI, Feb. 1999, pp. 380-383.
- [18] S. Goel, M.A. Elgamel, M.A. Bayoumi, Y. Hanafy, "Design Methodologies for high performance noise tolerant XOR- XNOR circuits", IEEE Transactions on Circuits and Systems - I: Regular Papers, Vol. 53, No. 4, 2006, pp. 867-878.
- [19] A. Fayed and M. Bayoumi, "A low-power 10-transistor full adder cell for embedded architectures," in Proc. IEEE Symp. Circuits Syst., Sydney, Australia, May 2001, pp. 226-229
- [20] M. Vesterbacka, "A 14-transistor CMOS full adder with full voltage swing nodes," in Proc. IEEE Worksh. Signal Process. Syst., Oct. 20-22, 1999, pp. 713-722.

AUTHOR'S PROFILE:



Krishna Chandra was born in February, 2, 1992, at Lakhminia, Begusarai in India. He received his B.Tech. Degree in Electronic and Communication Engineering from Uttarakhand Technical University, Dehradun (India) in 2013. He is currently pursuing M. Tech. (VLSI design) degree from Faculty of Technology, University Campus at the same university. His area of interests includes Electronics circuit design, VLSI design, Advance digital signal processing, electronics and communication, Digital image processing, and Nano scale device & circuit design.



Vishal Ramola working as an Assistant Professor and Head of Department in M.Tech. Department of VLSI design Faculty of Technology, University campus, Uttarakhand Technical University, Dehradun. He is a vigorous professor of VLSI Design in Uttarakhand. He has more than fifteen years of teaching experience and has published many research papers in various International Journals. His area of interest includes VLSI design, Advance VLSI Technology, and Nano scale circuit design. He is presently guiding a large number of M. Tech. students in the same area