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Performance and Analysis of 28T Full Adder using SVL Technique for Reducing Leakage Current at 45 nm Technology

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Abstract: *A conventional Full Adder using 28 transistors is presented here. In digital signal processors and microprocessors, the Full Adder is not only important for addition based digital circuit like multiplier and divider but is also used for accessing the address in memory. For low power requirement, there is a need to reduce leakage current in Full Adder. In this paper SVL (self controllable voltage level) technique is introduced for leakage current reduction and then standby leakage power reduction. Using SVL technique we can provide DC voltage supply as per requirement for load circuit in active mode and decrease DC voltage supply for load circuit in standby mode. This paper represents that leakage current of Full Adder using SVL technique is reduced by 61.8% as conventional Full Adder at .7volt DC supply. Simulation result is performed with 45nm CMOS technology, 20ns access time and 0.05GHZ frequency using cadence virtuoso tool.*

Keywords: *CMOS, Full Adder, leakage current, SVL technique.*

I. Introduction

Full Adder used in different logic circuits like multiplier [3], divider, parity checker, comparator and compressor and also used to generate address in case of memory access or cache is shown in fig.1. There are three types of basic structure on which Full Adder is based static, dynamic and hybrid. Static Full Adder are less power consuming than dynamic and then more reliable. Dynamic Full Adder have faster switching speed, full swing voltage level and less number of transistors but suffer from charge sharing, clock load, high power dissipation due to high switching activity and complexity [1], [2]. Hybrid Full Adder is basically the combination of static and dynamic Full Adder [5], [2].

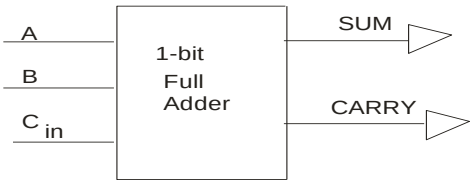

Fig.1 Symbol Diagram of Full Adder

There are number of research papers focus on different type of structures of Full Adder based on different logic structure design and also based on the way of expression of logic function. Full Adder performs the addition bit by bit with carry input and provides output with carry output. The carry output becomes the carry input for next input combination. We can see this in truth table in tab. 1. On the basis of truth table, the sum and carry function can be expressed as

$$SUM = \mathbf{A}.B.C + \overline{A}.\overline{B}.C + A.\overline{B}.\overline{C} + \overline{A}.B.\overline{C}$$
$$SUM = A \oplus B \oplus C$$
$$CARRY = A.B.C + \overline{A}.B.C + A.\overline{B}.C + A.B.\overline{C}$$
$$CARRY = A.B + B.C + CA$$

The gate level schematic of Full Adder is shown in fig.2 using above equation. Here we use the carry signal to produce sum signal instead of realize separate function for sum and carry signal [6]. For the transistor level implementation of Full Adder only14 NMOS and 14 PMOS transistors used see in fig.3. In this way we can reduce circuit complexity and save chip area.

II. Problems in Full Adder

With advancement in Technology from micrometer to nanometer transistor density is doubled, propagation delay and transistor threshold voltage are reduced by 30% and 15% respectively [1]. In VLSI for

transistor level implementation of any device there is the problem of tradeoff mainly between three parameters power dissipation, chip area and operating speed [5]. Chip area depends on the number of transistors, size of transistors and number of wires for connecting them.

Table.1 Truth Table of Full Adder

A	*B*	*C*	*SUM*	*CARRY*
0	*0*	*0*	*0*	*0*
0	*0*	*1*	*1*	*0*
0	*1*	*0*	*1*	*0*
0	*1*	*1*	*0*	*1*
1	*0*	*0*	*1*	*0*
1	*0*	*1*	*0*	*1*
1	*1*	*0*	*0*	*1*
1	*1*	*1*	*1*	*1*

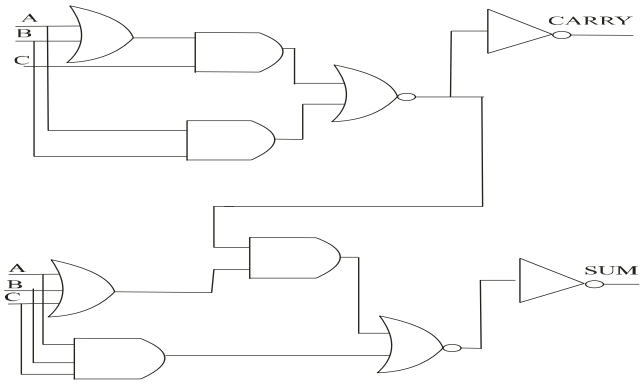

Fig.2 Gate Level Schematic of Full Adder

Operating speed mainly depends on propagation delay of transistors, number of inversion and intra-cell wiring capacitance [2]. Power dissipation in CMOS circuits is mainly due to node capacitance, transistor size and switching activity of transistors. In VLSI design, sources of power consumption are: 1) switching power due to charging and discharging of capacitances, 2) short circuit power due to current flow between power supply and ground when pull up and pull down network act simultaneously, 3) static power due to static current and leakage current [4]. Power dissipation for small size and battery operated equipments like mobile phone, palmtops, laptops and other biomedical equipments are mainly due to leakage current power dissipation. There is reduction in supply voltage and increase in magnitude of leakage current due to decrease in gate length up to 45nm [7]. In CMOS devices leakage current are of many types. 1) Sub threshold leakage current is the current which sink from drain to source of transistors when gate source voltage VGS is less than VTH (i.e. transistors are in cut off regions) [12]. When MOS device operating in weak inversion (sub threshold) region then sub threshold leakage current is the diffusion current of the minority carriers. The equation for sub threshold leakage current is

$$I_{DS} = K\left(1 - e^{\frac{V_{DS}}{V_T}}\right).e^{(V_{GS} - V_T + \eta.V_{DS}/nV_T)}$$

Where k and n are technology functions, η is drain induced barrier lowering coefficient. Sub threshold leakage current depends on temperature supply voltage, device size, and threshold voltage etc [10]. We can reduce sub threshold leakage current using higher threshold VTH in some part of design. 2) Another type of leakage current is called gate leakage current in which main current sinks from gate to substrate of transistor within the sio2 layer beneath the gate [11]. We can use multiple thickness of oxide layer to decrease the gate leakage. 3) Junction tunneling leakage current is the current which varies as an exponential function of reverse bias voltage and junction doping. It produces in reverse bias region due to generation of electron hole pair in the depletion region and due to diffusion of minority carriers near depletion region [12].

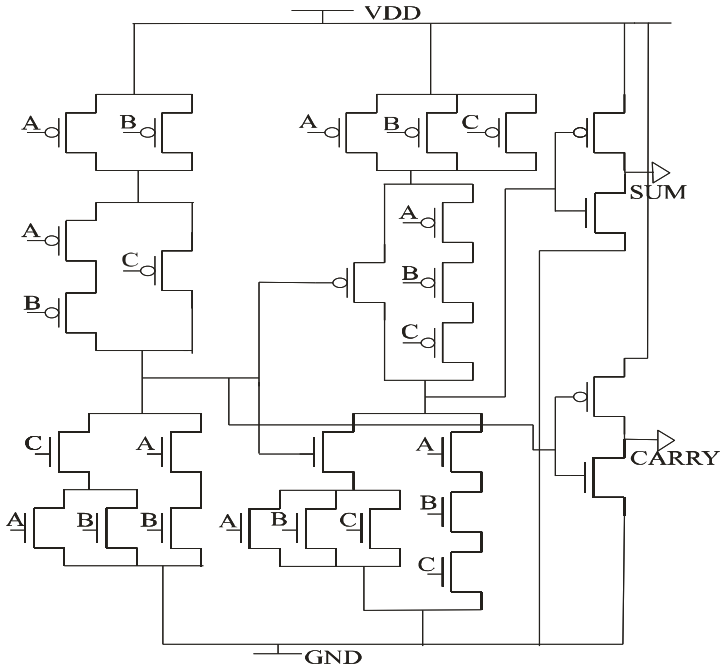

Fig.3 Transistor level schematic of Full Adder

III. Proposed work

To avoid leakage current length of gate should be large but with advancement in technology up to 45nm gate length becomes small and then leakage current increases. So it is a need to introduce leakage reduction techniques. Different techniques like MTCMOS technique, VTCMOS technique, stacking technique are used for reduce leakage current. But these techniques have some drawbacks like need for additional fabrication process, large area, and low power penalty etc [8]. For removing these drawbacks, an SVL (switch controllable voltage level) technique, having low leakage power and high speed performance, is introduced. In the active mode, the developed SVL circuit generates the maximum supply voltage and minimum ground level voltage for the Full Adder load circuit while in standby mode slightly lower supply voltage and relatively higher ground level voltage are produced [7]. Here reduction in leakage current using USVL, LSVL, SVL are compared for Full Adder.

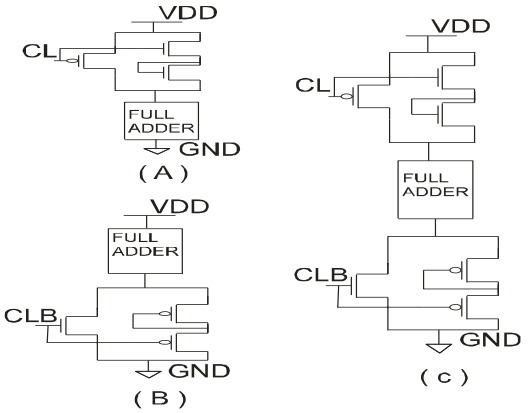

Fig.4 Full Adder with (A) USVL (B) LSVL (C) SVL technique

To implement the Full Adder with the help of EX-OR, AND, OR gate using above equation, 42 transistors are required and then circuit design need more area and more power consumption. In this paper a systematic approach to design 1-bit 28 transistor conventional Full Adder, used in ripple carry adders and array multipliers in different architectures of digital signal processors and microprocessors is presented. For implementing 1-bit 28 transistors conventional Full Adder the sum and carry function are represented by nested AND-OR-NOR structure [6]. The equation for implementing 28 transistors Full Adder is -

SUM = [(CARRY). (A+B+C)] + [A.B.C] and CARRY = A.B + (A+B).C

A. Full Adder with USVL technique

USVL circuit consist a parallel combination of single PMOSFET switch (p-SW) and several NMOSFET resistors (n-RS) in series [8], [9]. In the active mode p-SW turn on and then connect power supply to VDD while n-RS is switched off. In standby mode p-SW is off and n-RS is on and then VDD Supply is decreased. In standby mode when all inputs of Full Adder are zero. The pull up network of Full Adder operates in the linear region while the pull down network in the Full Adder is turned off. VDD is supplied to the Full Adder through several weakly 'on' n-RS then output voltage is -

$$VD = VDD - VN \quad (1)$$

Here VN is voltage drop of weakly 'on' on-RS. The drain to source voltage VDSN for NMOS of pull down network is -

$$VDSN = VD - VSS = VD \quad (2)$$

On varying the number of n-RS or channel width of n-RS, we can change the drain to source voltage VDSN for pull down network. When we increase VN then VDSN is decreased and this decreased VDSN increase the height of barrier close to the surface of the off NMOS in pull down network. In this way VDSN does not reduce barrier height more and drain induced barrier lowering (DIBL) effect in [13] is decreased and consequently threshold voltage VTHN of NMOS in pull down network is increased. Due to increase in VTHN there is decrease in sub threshold current from gate to source of the off NMOS in pull down network and also decrease in total leakage current.

B. Full Adder with LSVL technique

LSVL circuit consist a parallel combination of single NMOSFET switch (n-SW) and several NMOSFET resistors (p-RS) in series [8], [9]. In the active mode n-SW turn on and then connect ground supply to VSS while p-RS is switched off. In standby mode n-SW is off and p-RS is on and then ground Supply is increased. In standby mode when all inputs of Full Adder are zero. The pull up network of Full Adder operates in the linear region while the pull down network in the Full Adder is turned off. VSS is supplied to the standby Full Adder through several weakly 'on' p-RS then virtual

$$VS = VP \quad (3)$$

Here VP is the voltage drop of weakly 'on' p-RS. Thus the substrate bias VSUB,N (i.e. back gate bias) of the off NMOS in standby full inverter is increased and is given by

$$VSUB, = -VP \quad (4)$$

Furthermore, the equation of VDSN is given by

$$VDSN = VDD - VSS = VDD - VP \quad (5)$$

Here VDSN decreases. VSUB,N and VDSN can be changed by varying number of p-RS. The reduced value of VDSN decrease DIBL effect and increased VSUB,N increase back gate bias (BGB) effect. In this way VTHN is increased and sub threshold current is decreased and then total leakage current is decreased.

C. Full Adder with SVL technique

By applying USVL technique to the pull up network and LSVL technique to the pull down network of Full Adder we implement SVL technique based Full Adder [8], [9]. In active mode both p-SW and n-SW are 'on' while n-RS and p-RS are 'off'. Hence maximum supply voltage VD = VDD and minimum ground level voltage VS (= VSS = 0) are supplied to the active load circuit of Full Adder. In this way operating speed for Full Adder is also enhanced. In standby mode both p-SW and n-SW are 'off' while n-RS and p-RS are 'on'. The output voltages VD and VS for SVL circuit are expressed by equation (1) and (3). Here DIBL effect more reduced due to application of both USVL and LSVL and VDSN can be expressed as

$$VDSN = VDD - (VN + VP) \quad (6)$$

Back gate bias (BGB) effect is also increased due to LSVL. Thus there is more increase in threshold voltage VTHN and consequently more reduction in total leakage current.

IV. Simulation Result

The simulation of Full Adder for input and output waveform is shown in figure 6. In next figures the simulated leakage current waveform of conventional Full Adder and simulation for reduced leakage current waveform through USVL, LSVL and SVL are shown. All simulations are performed at 45nm technology using cadence virtuoso tool. The results for leakage current from voltage range of 0.5 to 1.2 volt for conventional Full Adder and SVL technique based Full Adder are shown in tab.2.

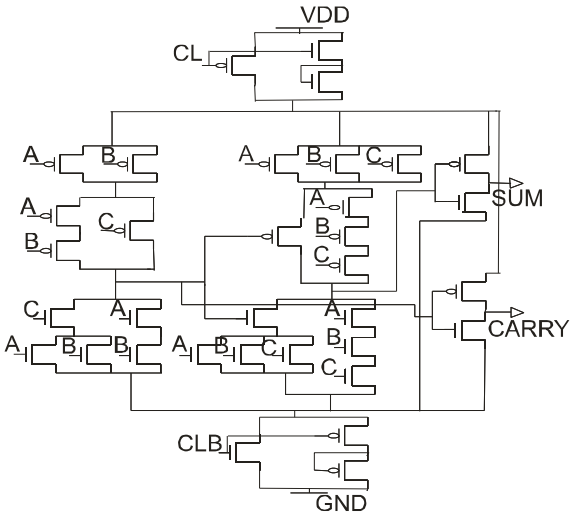

Fig.5 SVL Technique in Full adder

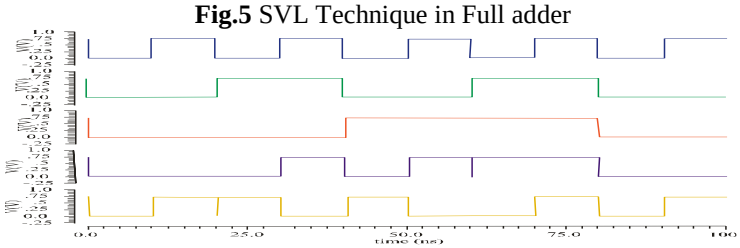

Fig .6 Input Output Waveform of Full Adder

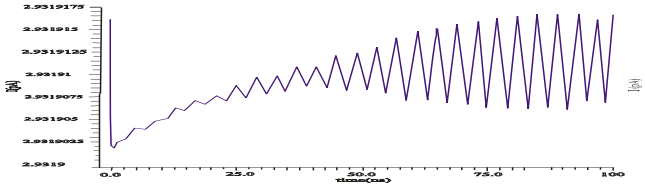

Fig.7 Leakage current Simulated waveform of Full Adder

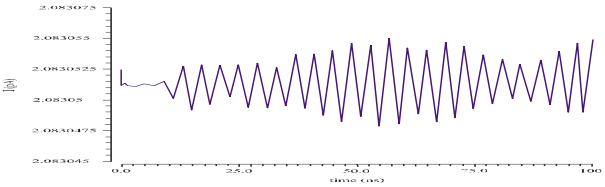

Fig.8 Leakage current Simulated waveform of Full Adder with USVL

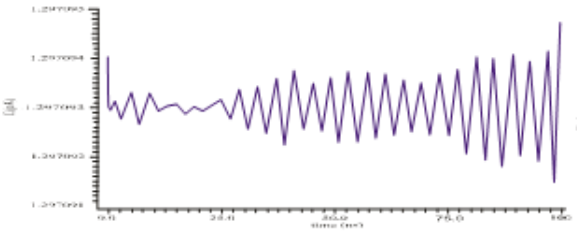

Fig.9 Leakage current Simulated waveform of Full Adder with LSVL technique

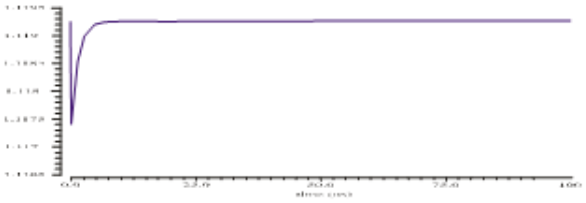

Fig.10 Leakage current Simulated waveform of Full Adder with SVL technique

Table.2 Table for comparison of Leakage Current in 28T Full Adder at different voltages

Voltage supply (V)	Conventional (pA)	USVL (pA)	LSVL (pA)	SVL (pA)
.5	2.323	1.907	1.179	1.083
.7	2.932	2.083	1.297	1.119
.9	3.487	3.475	1.401	1.398
1.0	3.749	3.748	1.451	1.451
1.2	4.898	4.258	1.557	1.557

V. Conclusion

The 1-bit 28 transistor conventional Full Adder is simulated here at 45nm technology for calculation of leakage current. The results for reduction in leakage current by using USVL, LSVL, SVL techniques are compared from .5volt to 1.2volt voltage range. The leakage current in Full Adder are reduced from 2.932 to 1.119 pico- ampere at .7volt using SVL technique. Hence from the above result we can conclude that SVL technique based conventional Full Adder is better than conventional Full Adder.

Acknowledgements

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References

[1]. Garg, D., Rai, M. K. 2012. CMOS Based One Bit Full Adder Cell for Low Power Delay Product. IJECCT. vol. 2, issue. 4, pp. 18-23.

[2]. Wairya, S., Nagaria, R.K., Tiwari, S. 2012. Comparative Performance Analysis of XOR XNOR Function Based High Speed Cmos Full Adder Circuits for Low Voltage VLSI Design. International Journal of VLSI Design and Communication System. vol. 3, No.2, pp. 221-242.

[3]. Reddy, P. P. K., Satyanarayana, K. V. 2014. Power Analysis of Different Full Adder With different CMOS Logic Design. International journal of Engineering Trends and Technolgy. Vol. 16.

[4]. Channegowda, .C, Dr. Aswatha, A. R. 2013. Low Power One Bit Full Adder Cell Using Modified Pass Transistor Logic. International Journal of Computer Science and Information Technologies. Vol.4, No.3, pp. 489-491.

[5]. Suresh, G., Rao, C. S. 2014. Performance Evaluation of Full Adder And its Impact on Ripple Carry Design. International Journal of Research in Engineering and Technology. Vol. 3, No. 4, pp. 23-28.

[6]. Kushwah,S. S., Maheshawari, R., Khandagre, Y. 2013. SVL Leakage Current Applied in 1 Bit Adder in VLSI" International Journal of Emerging Technologies in Computational Applied Sciences,Vol. 4. pp. 541-545.

[7]. Enomoto, T., Oka, Y., Shikano H. 2003. A Self Controllable Voltage Level Circuit And its Low Power High Speed Cmos Circuits Application. IEEE Journal of Solid Circuit. Vol. 38, No.7, pp. 1220-1226.

[8]. Khandelwal, S., Akashe, S. 2011. Supply Voltage Minimization Techniques for SRAM Leakage Reduction. Journal of Computational and Theoretical Nanoscience. Volume. 9, No. 8, pp. 1044-1048.

[9]. Manorama., Khandelwal, S. and Akashe, S. 2013. Design of a FinFET based Inverter using MTCMOS and SVL Technique reduction Technique. in proceeding of 2013 Students Conference on Engineering and Systems (SCES), Allahabad, India, pp. 1-6.

[10]. Agarwal, A., Roy, K. 2003. A Noise Tolerant Cache Design to Reduce Gate and Sub-threshold Leakage in the Nanometer Regime. ISLPED.Vol. 3, pp. 18-21.

[11]. Sikarwar, V., Khandelwal, S. and Akashe, S. 2013. Optimization of Leakage Current in SRAM Cell using Shorted Gate DG FinFET. In proceeding of 3rd International Conference on Advanced Computing and Communication Technologies (ACCT 2013). pp. 166-170.

[12]. Gupta.R, Pandey.Satya Prakash., Akashe.S, Vidyarthi.A. Analysis and optimization of Active Power and Delay of 10T Full Adder using Power Gating Technique at 45 nm Technology. IOSR Journal of VLSI and Signal Processing (IOSR-JVSP). Volume 2, Issue 1 (Mar. – Apr. 2013), PP 51-57.

[13]. Karim, M. A., Venugopalan, S. K., Chauhan, Y. S., Lu, D., Niknejad, A. and Hu, C. 2011. Drain Induced Barrier Lowering (DIBL) Effect on the intrinsic capacitances of nano Scale MOSFETs. NSTI Nanotech. vol. 2, pp. 814-817.