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Designing of Current-Mode Active Filter Using 45nm CMOS-Based CCII

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Abstract:*Conventional design techniques in VLSI are in voltage mode but we experience various drawbacks like smaller bandwidth, low linearity, higher power consumption, less gain etc. Also, the power of any circuit is proportional to the product of the biasing voltage and biasing current and, if we concentrate on current signal rather than the voltage signal, a better control over power can be observed. And hence, current mode circuits like current conveyors are getting prominent consideration in analog ICs designingdue to their higher band-width, greater flexibility, larger dynamic range, lower power consumption and less chip area. In this paper a new current mode active filter is proposed that uses a single current conveyor and a pair of capacitors and resistors. By varying the bias current and the values of the passive components, the desired low-pass, high-pass and band-pass responses can be obtained through the circuit simultaneously. All the responses were realized in 45nm CMOS technology and simulated through Cadence tool (Virtuoso).*

Keywords: *Active filter, Bandwidth, Cadence, CCII±, Current mirror, Current mode.*

I. Introduction

Most of the conventional analog circuits are in voltage mode whose performance is evaluated in terms of voltage level [1]. But such circuits suffer from various drawbacks like higher supply voltage, low slew rate, etc. and they are also not suitable for high frequency applications thus, limiting the bandwidth of the circuit [2]. However, a MOS based current conveyor seems to be a more favorable device for analog VLSI regime. MOS transistors can more efficiently process current over voltage because in both of the amplifier configurations i.e. the common-source and the common-gate, the output signal is a current. While the common-drain configuration of the amplifier provides voltage which has its own drawback of a bulk-effect present in typical CMOS processes. The MOS transistors based current conveyors serves as a good building block because it shows better performance in comparison to the previously used operational amplifiers and also they behave more or less like an opamp and so it comes handy as a good replacement in the true sense. Current conveyor (CCII) has an added advantage of design simplicity, higher slew rate, high bandwidth and low propagation delay. Such a current conveyorconsists of one high and one low impedance input and one high impedance output which make it favorable for both current mode and voltage mode circuits [3].

Researchers reported many current conveyors such as DDCC, CCCII, CDTA, etc. in the literature[4, 5]. Many circuit such as filters, rectifier, oscillator, etc. have been designed using various current conveyors. The circuits designed using current conveyors showexcellent response having higher bandwidth, low power consumption etc. So the researchers are attracted towards current conveyors for the designing of various circuits.

In this work, section I gives the introduction of the paper as a whole. Section II gives the brief description about the second generation current conveyor i.e.about their working, node and matrix relationship between input and output. Section III gives idea about how the CCII is designed. Section IV gives analysis information of CCII i.e. AC response and transient response. Section V depicts the designing of the proposed filter circuit. The simulation results have been shown in section VI. Section VII shows the results of the filter tuned for particular application. The paper is concluded in section VIII.

II. 2nd Generation Current Conveyor

A 2nd generation current conveyor is more design friendly as it does not require any high precision component and uses comparative biasing supply thus lead to design and realize different applications like filter, oscillator, etc. Fig. 1 shows the block diagram of a typical CCII, where X is the low input impedance terminal, Y is the high input impedance terminal and Z+ and Z- are the in-phase and out-phase output terminals respectively [1, 2].

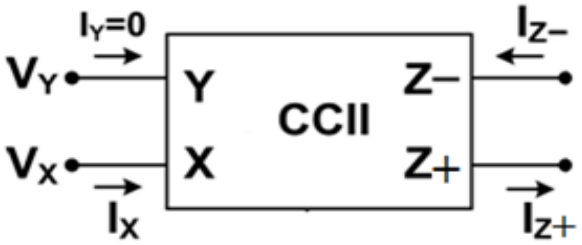

Figure1 Block diagram of CCII

In Fig. 1, terminal Y exhibits infinite input impedance. The voltage at X follows that applied to Y, thus X exhibits zero input impedance. The current supplied to X is conveyed to the high impedance output terminal Z where it is supplied with either positive (CCII+) or negative (CCII-) polarity. The relationship between the voltage and currents at the respective input output ports of CCII is depicted by the following matrix:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \qquad (1)$$

III. Design Approach Of Ccii

A CCII is usually simple in structure and design, and posses a generalized nature, therefore can be used as a prototype in the design of systems. The transistor level circuit diagram CCII± is shown in Fig. 2.

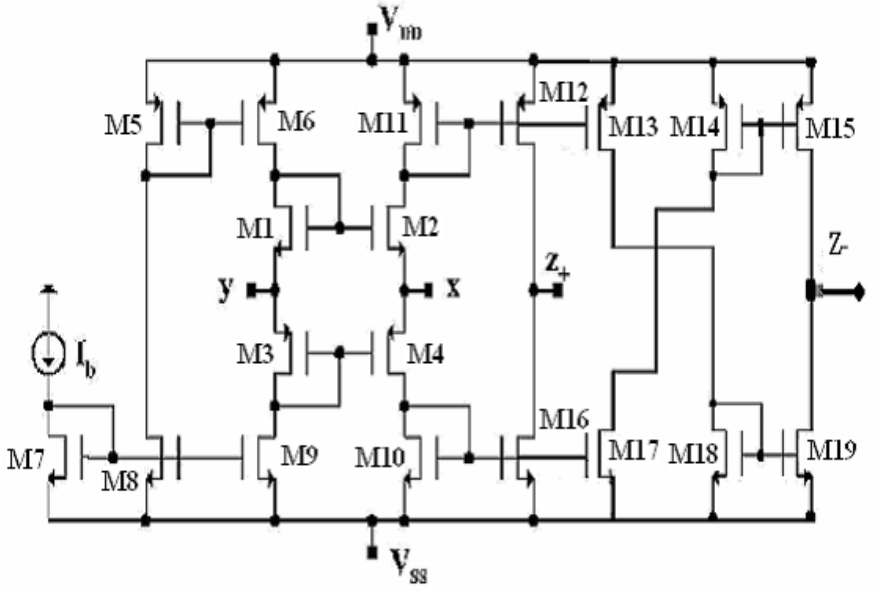

Figure 2 Transistor level circuit diagram of CCII

The CCII circuit shown in Fig. 2consists of one mixed trans-linear loop (transistors M1 to M4) as input cell, two current mirrors (transistors M5, M6 and M8, M9) which allow us to produce reliable output current as the replica of the input current in the circuit and also allows the trans-linear loop to be dc biased with the help of current I_b [6, 7]. The transistors M6, M11, M1, M2, M3, M4, M9 and M10 form a translinear push-pull output type structure, which is symmetrical and therefore balanced. This symmetry helps in reducing many abnormalities like temperature, mismatches, channel length modulation, etc. among various transistors due to MOSFET parameters. For the purpose of producing the out of phase output, two current mirrors are cross coupled. In Fig.2, '+' sign stands for the direction of current I_Z same as shown, '-' stands for the reverse direction of I_Z with respect to I_X. Node 'Y' is the voltage controlled node with no current. Impedance looking into node 'X' is ideally zero. The current I_Z remains independent of voltages V_X. In the present work, for implementing the active filter, CCII± circuit shown in Fig. 2 is used and is implemented in 45nm CMOS technology using Cadence tool (virtuoso).

IV. Design Analysis Of Ccii

The CCII Circuit shown in Fig. 2 is implemented using cadence by taking W/L ratio as 2/1. The circuit diagram is drawn in cadence as shown in Fig. 3, which can serve as a powerful active element. The performance of the CCII circuit has been verified by conducting its transient and AC analysis.

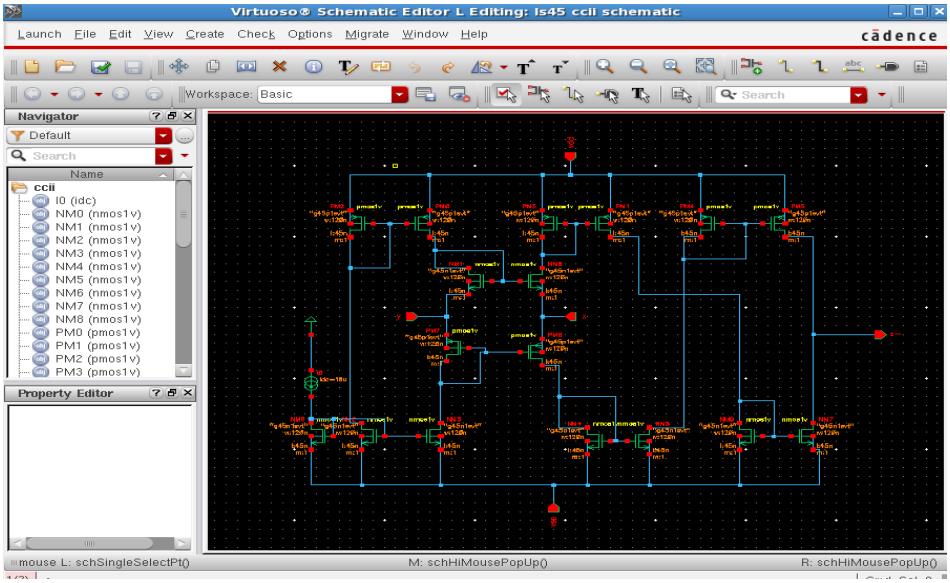

Figure 3 Circuit diagram of CCII implemented in CADENCE

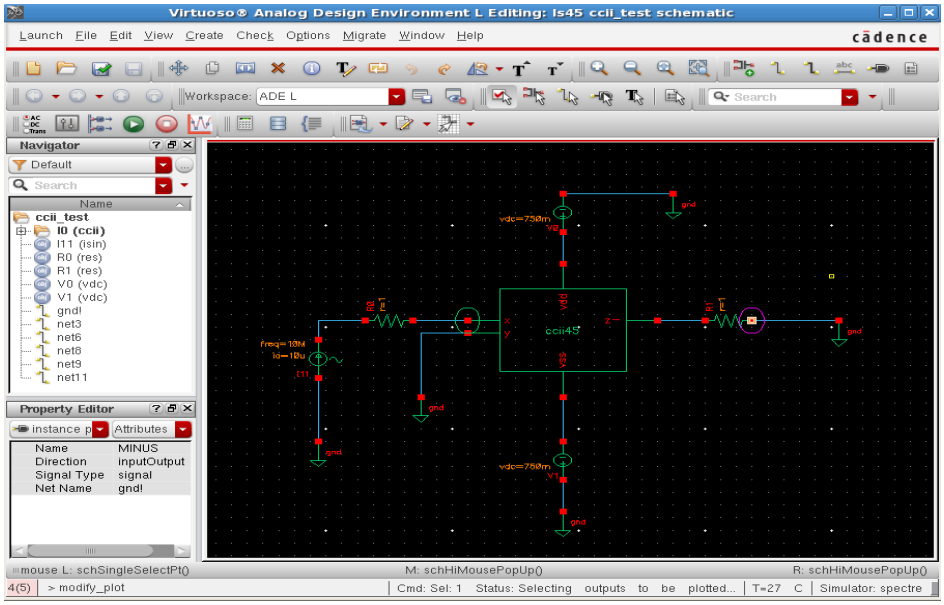

Figure 4 Symbolic test diagram of CCII in CADENCE

4.1 Transient Analysis

Transient analysis has been performed by taking a sinusoidal input of 10MHz frequency. Fig.5 shows the transient response of the CCII blockdesigned in cadence. It is observed that the output at Z- terminal is out of phase with respect to input at X terminal thus satisfying the Equation (1).

Figure 5 Transient response of CCII circuit

In Fig.5, the wave on the upper side (R_1) is the input provided at the terminal X and the wave on the lower side (R_0) is the corresponding out of phase output to the input provided, measured at terminal Z-.

4.2 Ac Analysis

Fig.6 shows the AC response of the CCII block designed in cadence. AC analysis reveals excellent conformity between input and output up to 7GHz according to the Equation 1.

Figure 6 AC response of CCII circuit

In Fig.6 the wave on the upper side (I_0) is the input provided and the wave on the lower side (R_1) shows the AC (3db) response to the input provided. Thus the CCII block designed is suitable for high frequency applications.

V. Active Filter

CCIIs are now widely used to realize active filters and also act as a popular building block in designing various analog circuits. The active filters played a very vital role in keeping pace with the need for reduction in size and cost of the circuits designed in comparison to the passive filters because it uses active elements in place of large and expensive passive ones. Activefilters are one of the most popular analog filters as they have a significant advantage that they do not contain any inductors, and hence reducing the problems associated with it and also the general filters responses i.e. low-pass, band-pass and high-pass can be obtained accurately[8-11]. A current mode active filter is implemented using a single CCII of Fig. 1, two resistors and two capacitors. The block diagram of the proposed filter is shown in Fig. 7. The filter designed using cadence is shown in Fig.8.By doing the routine analysis of the filter circuit of Fig.7, we obtain the expressions for band-pass and high-pass filter respectively as shown in Equation 2 and 3.

$$I_{R1} = \frac{sC_1R_1R_2}{s^2C_1C_2R_1R_2+sC_1(R_1+R_2)+1} I_i \quad (2)$$

$$I_{C2} = \frac{s^2C_1C_2R_1R_2}{s^2C_1C_2R_1R_2+sC_1(R_1+R_2)+1} I_i \quad (3)$$

The quality factor Q and angular frequency ω_0 are given by the following expressions:

$$Q = \frac{1}{R_1+R_2}\left(\frac{C_2R_1R_2}{C_1}\right)^{1/2} \quad (4)$$

$$\omega_0 = \frac{1}{(C_1C_2R_1R_2)^{1/2}} \quad (5)$$

Since, high-pass gain is equal to one, at the angular frequency (ω = ω$_0$), the gain of the band-pass response depends on the resistor ratio:

$$H_{BP}(\omega_0) = \frac{R_2}{R_1+R_2} < 1 \quad (6)$$

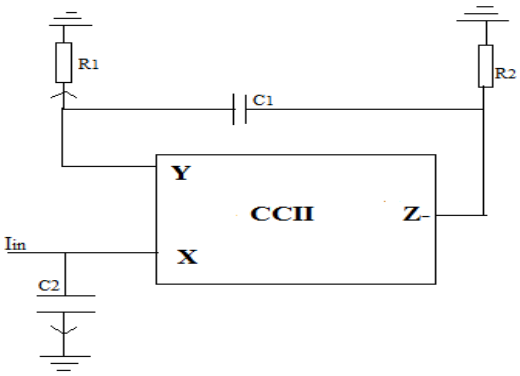

Figure 7 Block diagram of proposed active filter

VI. Simulation Results

The optimized results of the circuit implemented as shown in Fig.8 are obtained for the following values of the passive components; R_1=10KΩ, R_2=50Ω, C_1=1fF and C_2=10fF. The biasing current is chosen to be 10μA and the power supplies are selected to be ±0.75V. The low-pass, band-pass and high-pass response of the filter designed is shown in Fig. 9, 10 and 11 respectively.

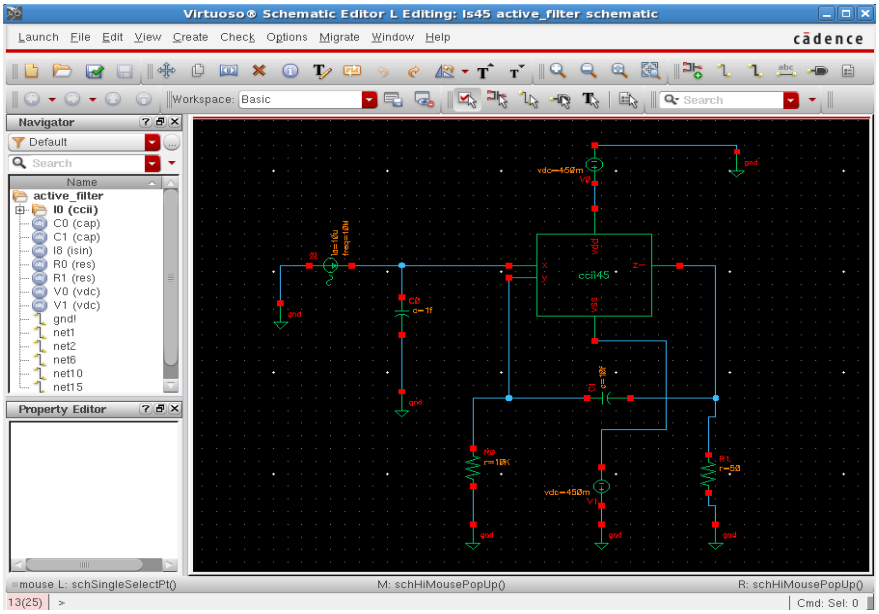

Figure 8 Active filterdesignin CADENCE

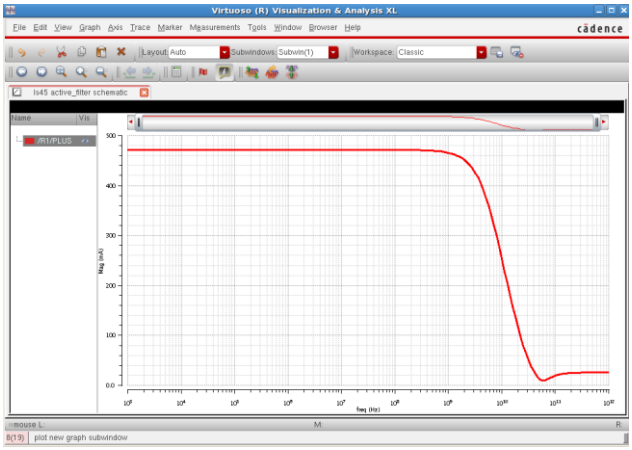

Figure 9 Low pass filter response

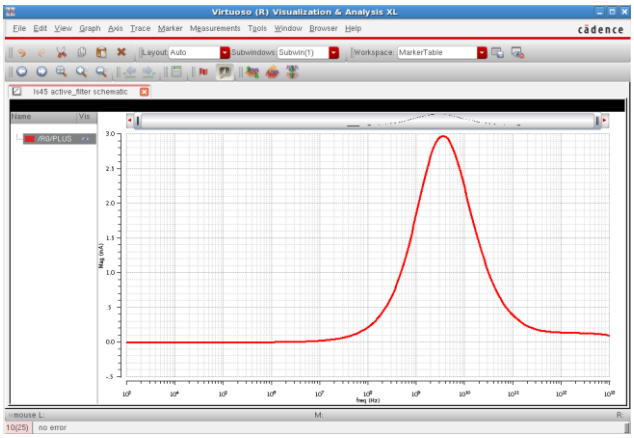

Figure 10 Band pass filter response

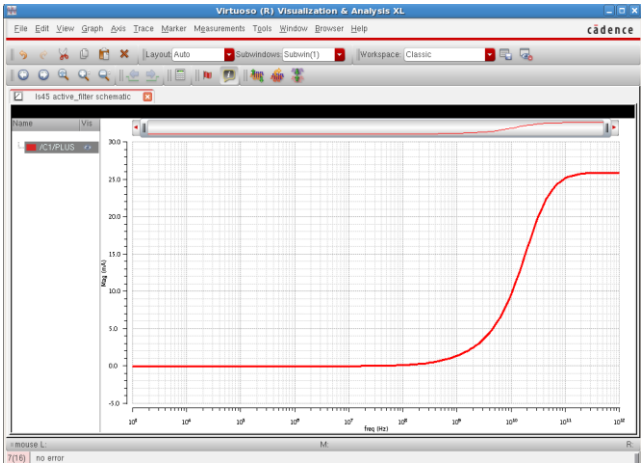

Figure 11High pass filter response

Table 1 shows the comparison of previous works[9], [10] using CCII with the present work.Here the comparison has been done based on technology, no. of active elements, no. of passive elements used etc.

TABLE 1: Comparison Table

	[9]	[10]	Work
Technology	CMOS	CMOS	CMOS
Technology node	180nm	500nm	45nm
No. of active element	2	2	1
No. of Resistors	1	4	2
No. of Capacitors	1	2	2
Type of active element	CCII±	CCII±	CCII-

VII. Filter Tuning

Bluetooth operates at frequencies between 2.402 and 2.480 GHz, or 2.4 and 2.483 GHz which includes guard bands 2MHz wide at the bottom end and 3.5MHz wide at the top. It can be shown that the filter designed in the present work can be tuned in the 2.4 GHz of ISM band for Bluetooth range. It has been done by varying the value of the passive resistances. The result of tuned filter has been shown in Fig. 12.

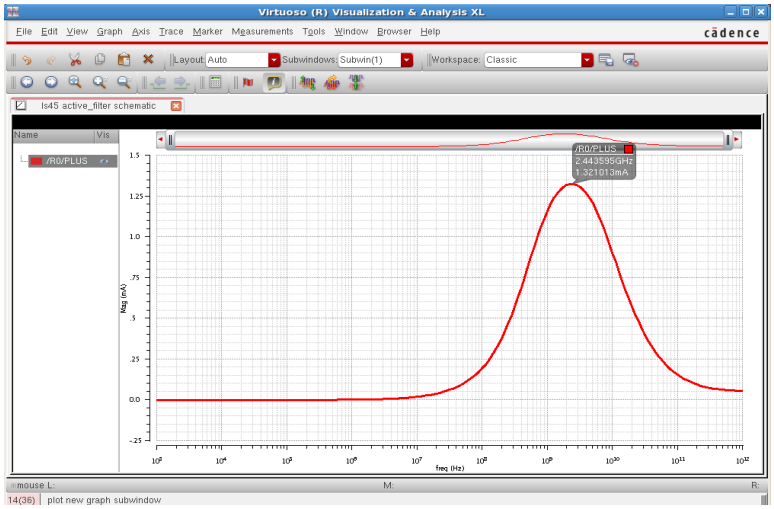

Figure 12 Tuned filter response

VIII. Conclusion

The active filter circuit proposed in Fig.7 was simulated using Cadence (virtuoso). Fig. 9, 10 and 11 shows the band-pass, high-pass and low-pass filter responses respectively. The values of the components used are R_1=10K, R_2=50, C_1=1f and C_2=10f. The circuit uses a single current conveyor as an active block. Transient analysis has been done that satisfies relation between the input current I_X and output current I_{Z-} as shown in Equation 1. AC analysis reveals the excellent conformity between input and output up to 7GHz. The bandwidth of the band-pass filter is 1.2MHz-11.19GHz and the low pass and high pass filter's cutoff frequencies are 6.64GHz and 26.19GHz respectively. It is shown in Fig. 12 that the filter can be tuned for Bluetooth applications. Thus theCCII can be used as a basic building block in various other circuits like oscillators, function generators, rectifiers, etc

References

[1]. K. C. Smith and A. Sedra, A second generation Current Conveyor and its application,IEEE trans. Circuit theory, 17, 1970, 132-134.
[2]. K. C. Smith, 'the current conveyor: a new circuit building block, Proc. IEEE, 1968, 1368-1369
[3]. Allen, P.E. y D.R. Holberg, CMOS analog circuit design. New York (Oxford University Press, 2002).
[4]. J. Sharma and K. Shrama, 'Performance Evaluation of Electronic Tunable Filter Using CCCII 45nm CMOS Technology for WIFI Applications', International Journal of Science and Research, 5(3),2016,2053-2056
[5]. J. Sharma and A. Shrama, ' Universal Filter Design using 45nm CMOS-based DDCC for Bluetooth/Zigbee Application', International Journal of Computer Applications, 134(13),2016
[6]. S. Maheshwari, Novel Cascacadable Current-Mode First Order All-Pass Sections,International Journal of Electronics, 94(11), 2007, 995-1003.
[7]. C. M. Chang, 'Current-mode lowpass,bandpass and highpass biquads using two CCIIs' Electronics Letters, 29(23), 1993, 2020-2021.
[8]. Doru E. Tiliute,' Second order active filter using a single current conveyor', 1(2), 2001, 1-2
[9]. Jiun-Wei Horng, Chun-Li Hou, Yi-Sing Guo, Chih-Hou Hsu, Dun-Yih Yang and Min-Jie Ho, Low input and high ouput impedances current-mode first-order allpass filter employing grounded passive components, Circuits and systems, 3, 2012, 176-179
[10]. Manish Kumar, M.C Srivastava, Umesh Kumar, Current conveyor based multifunction filter, International journal of computer science and information security, 7(2), 2010
[11]. D. Biolek and V. Biolkova, 'Allpass filter employing one grounded capacitor and one active element,' Electronics Letters, 45(16), 2009, 807-808