

Low Power Multiplexer Design Using Modified Dcvsl Logic

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Abstract: This paper is based on pre layout schematic simulations of a proposed design of 2:1 MDCVSL multiplexer circuit that shows improved performance than the existing 2:1 multiplexer circuit. The proposed design shows superiority in terms of power consumption and temperature sustainability when compared with existing 2:1 CMOS multiplexer and comparative analysis on 90nm technology. A power comparison with respect to supply voltage V_{DD} is done by varying it from 0.6 to 1.4 volts and power is calculated for both conventional and proposed design which results power in 15 μ w to 128 μ w. This shows considerable reduction in power from 25-32% and hence justifies the superiority of the proposed schematic.

Keywords: Multiplexer, Adiabatic Logic, Low Power, GDI Logic, MDCVSL Logic.

I. Introduction

Multiplexors are key components in VLSI design which are used to implement various logics as well as signal routing tasks. MUX is also heart of any arithmetic and logic circuit and are commonly basic building blocks for data switching structures, data paths and switch logic [1]. It is used in designing various circuits like CPU, Graphics controller, Digital video, computer networks, PLD's, Telecommunications [2]. Power dissipation is a major concern in modern VLSI industry. Currently the market is growing in more and more portable devices which have batteries as their power source. These batteries have limited size and capacity so their use is limited by how much power is being consumed. So due to this restriction of batteries the circuitry is to be designed to consume less power taking consideration of noise and cooling requirements.

There are various techniques used for power saving such as scaling or reduction of supply voltage, reduce capacitances, using less switching elements. Most of the energy supplied by power supply is almost dissipated by the circuit which causes heating and noise generation and instabilities which further degrades system performance [3]. Due to rapid growth in digital circuitry numerous research efforts are required to cope with demand of increase in speed, compaction of device and lowering the overall power dissipation. A Multiplexor can be analogue or digital in nature by either using transistors or logic gates[4].

II. Multiplexer Designs

A mux is device which has 2^n input lines and n select lines. These n select lines are used to select analog or digital input signals present on input lines and forward the selected signal to a single output line.

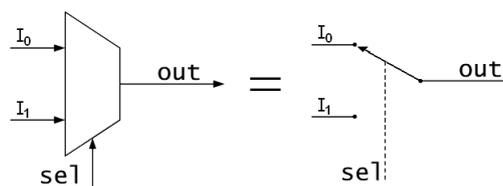


Fig 1: A basic 2-1 mux device can be seen equivalent to a line selector switch

The mux operation can be written as following equation

$$F = \sum_{i=0}^{2^n-1} S_i I_i \quad (1)$$

Where I_i is input signals and S_i is minterm equivalent of select lines.

There are different logic designs used to implement mux each having its own performance and characteristics some of which are reviewed here.

2.1 Transmission Gate Logic

A transmission gate is a electronic circuit element which can selectively pass a input signal level to a output line. It consists of a parallel connection of pMOS and nMOS transistors. Both gates are biased in complementary fashion so that both of these gates are either on or off simultaneously. When gates are biased such that both transistors are conducting then input is passed to output otherwise it is in high impedance state [1].

A Multiplexor can be designed using TG by taking two gates and providing them signals again in complementary form so that one gate circuit becomes active at once according to select logic but an additional inverter circuit is required to implement this.

This type of design reduces number of gates in the circuit and thus reduces overall power dissipation.

2.2 Adiabatic Logic

Adiabatic circuits use pulsed power supply or we can say AC power supply as compared to standard DC power supplies in CMOS circuits. The key idea behind this logic is to recycle the energy stored in the load capacitances in the form of ac power rather than to dissipate it in form of heat. In these circuits charging and discharging of capacitors is done by a constant current to reduce power consumption [3]. So as its name indicates instead of dissipating its energy in charging process at output node to ground it recycles this energy towards power supply hence reducing power consumption [8].

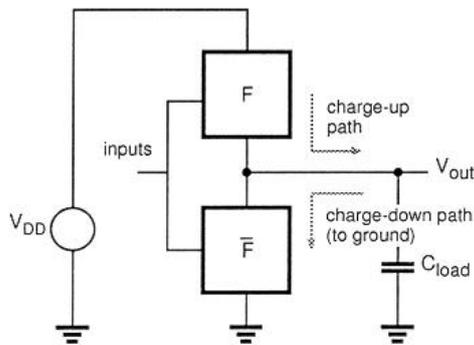


Fig 2: Conventional CMOS logic gate topology [12].

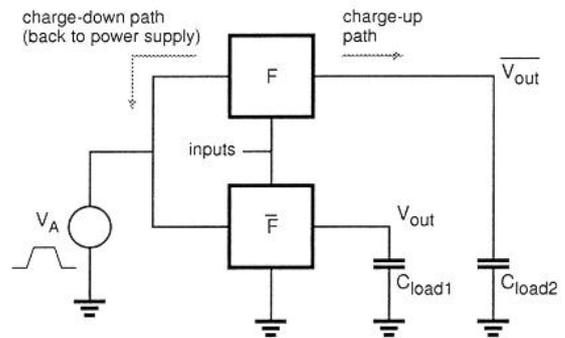


Fig 3: Same function implemented in adiabatic logic topology [12].

2.3 Dual Pass Transistor Logic (Dptl)

In DPTL logic parallel connection of PMOS and NMOS network is done and the source terminals are connected to some input signals instead of connecting to power lines [10]. This logic implementation reduces number of transistors and optimizes the circuit in terms of area and power dissipation [8].

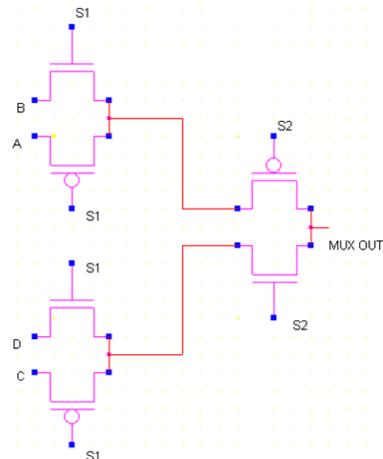


Fig 4: 4 to 1 mux design using DPTL logic [8].

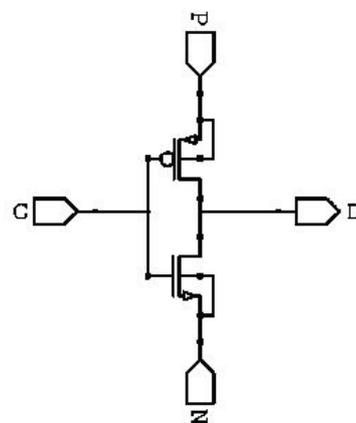


Fig 5: Basic GDI cell [11].

2.4 Gate Diffusion Input Logic (Gdi)

In GDI cell sources and their substrate terminals are not connected to supply instead they can be biased randomly it has one pMOS and one nMOS transistor similar to CMOS inverter structure.

The main advantage using this technique is that we realize some basic logic functions including mux with the help of this technique. The circuit designed with this approach has less number of components and higher operational speed. By reduction of number of gates it is suitable for low power designs.

III. Proposed Schematic

CVSL or Cascode Voltage Switch Logic refers to a logic family which is designed for certain advantages such as low power consumption.

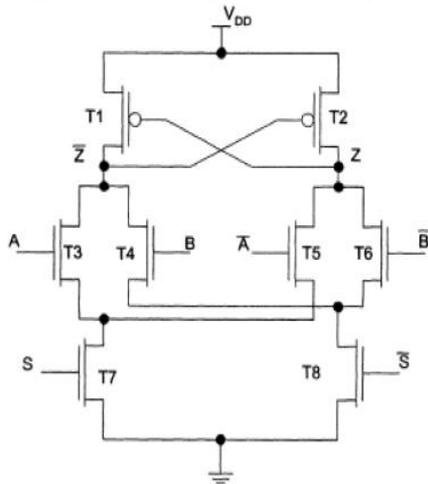


Fig 6 :Schematic of DCVSL Mux[2].

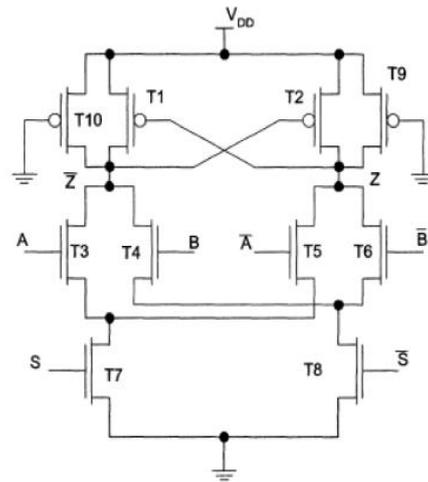


Fig 7:Schematic of Modified DCVSL Mux[2]

The complementary output is generated by pull down network of NMOS tree. DCVSL is advantageous in achieving logic density by eliminating large PFETS from each logic function. This circuit has two parts, a differential latching circuit and a cascaded complementary logic array. In this paper, the Modified Differential Cascode Voltage-Switch Logic (MDCVSL) circuit is designed. The key benefits of MDCVSL are consuming no static power as compared to standard CMOS and it uses a latch to compute output quickly. The main requirement of this circuit is true/complement inputs, and it also produces true/complement outputs. It benefits in the way that it allows “Complex” gates and never needs inverters on the logic path and low power consumption. A logic function and its inverse are automatically implemented in this logic style by adding two NMOS transistors in the pull up part of existing 2:1 multiplexer.

The circuit shows a remarkable improvement over the existing design. In the proposed circuit due to the excess added transistors there is a reduction in threshold loss in the circuit, which further causes the reduction in overall power consumption of the circuit. The two logic trees are capable of processing complex functions within a single circuit delay. The schematic of proposed 2:1 multiplexer is shown here.

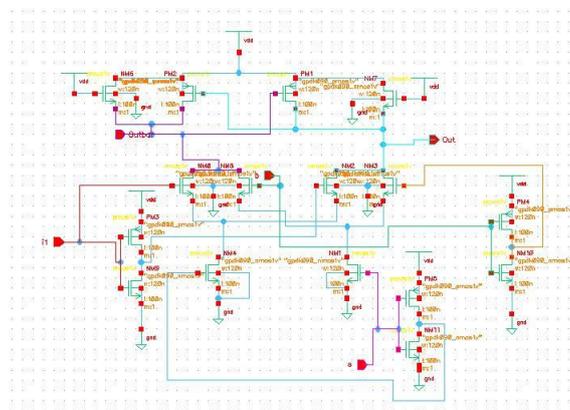


Fig 8: Proposed design of 2:1 mux

IV. Simulation And Analysis

The above circuit has been simulated using 90 nm technologies on simulation tool. To make the testing environment impartial testing all the circuits has been simulated on the same input patterns. And also all the simulations have been done on room temperature 27°C.

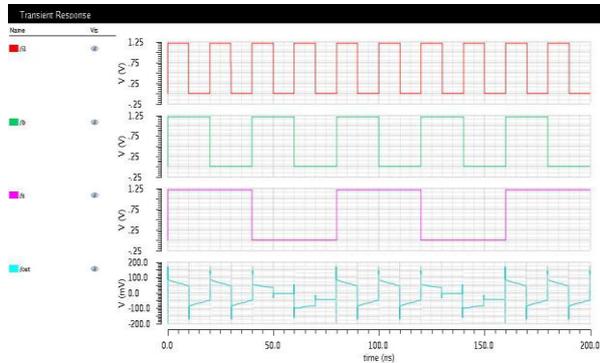


Fig 9: Simulation waveforms for proposed design

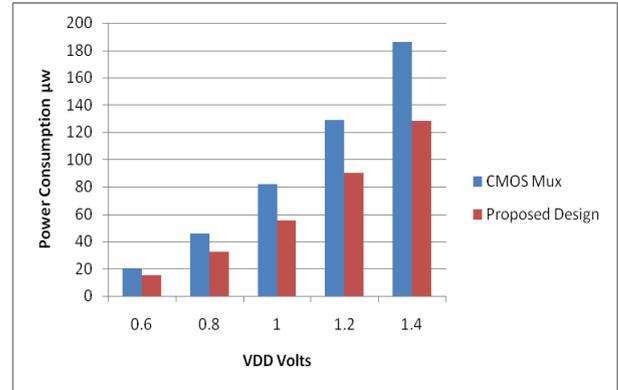


Fig 10: Comparison chart for both designs

The result obtained for proposed design in terms of power consumption are shown as following.

Table 1: Analysis of power consumption

V _{DD} (Volts)	Power Consumption		Percent Improvement
	CMOS Mux(μw)	Proposed Mux(μw)	
0.6	20.427	15.218	25.51 %
0.8	46.004	32.482	29.40 %
1.0	82.201	55.338	32.68 %
1.2	129	90.180	30.10 %
1.4	186	128	31.19 %

It is clear from above table that for proposed design power consumption is clearly less as compared to existing design.

V. Conclusion

The proposed 2:1 multiplexer is found to give better performance than the existing 2:1 multiplexer. The proposed circuit has been tested to have better temperature sustainability, frequency and significantly less power to achieve high performance. The proposed 2:1 multiplexer has been designed and studied using 90nm technology and proved it to be a better option for low power complex system design.. The net effect is that proposed 2:1 multiplexer shows a much better performance compared to existing 2:1 multiplexer. The results show that power is reduced upto 32% by using this schematic design as supply voltage is varied from 0.6 to 1.4 volts. The output power results in 15 μw to 128 μw as compared to 20 μw to 186 μw by using standard CMOS logic

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