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Analysis, Design and Implementation of Full Adder for Systolic Array Based Architectures – A VLSI Based Approach

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Abstract: *Full adder is the functional building block and basic component in several architectures found in VLSI and DSP applications, Adder is a versatile component and mainly used in addition and multiplication as the basic processing element; Adder in a VLSI application is used in ALU design, Address generation in processors, Multipliers and so on. In DSP applications it is used code for conversion, Signed addition and Signed multiplication, Transformations and signal processing applications. This defines the need and importance of designing an adder block in effective way. Systolic array architectures consists of processing elements(PE), where the computation of the task is divided and given to PE's and final result is obtained for these PE's; In systolic array multiplier we have 1-bit full adder as the Processing element in the structure. In this paper we have considered three different types of 1-bit full adder design namely 54Transistor CMOS design, 28Transistor CMOS design and 10Transistor GDI design, these designs are analyzed using CADENCE Design Suite 6.1.6 tool for transistor level design and implementation by the sub-tool Virtuoso, ADE, and ASSURA provided, performance is measured for GPDK 180nm technology and a comparative analysis of the adders is coated here with- Number of transistors/ Gate count, Delay, Power, and Power Delay Product. These are the prime concern parameters of performance measure in our design, for simplicity and ease of implementation we have not varied the width and length of the MOS devices used in this paper, Using the Comparative analysis coated in this paper for the full adder, a effective adder design can be chosen based on the performance criteria as required by the designer.*

Keywords*: Full adder, Systolic Array Architectures, CADENCE Design Suite, 28Transistor CMOS full adder design,10Transistor based GDI design, Gate count, Power, Delay, and Power Delay Product.*

I. Introduction

In recent years the growth of VLSI technology is augmented due to its application in computing devices and wireless communication systems. Technology trends nowadays shows that circuit delay is scaling down by 30% while performance and transistor density are doubled approximately every two years and transistor's threshold voltage is reduced by almost 15% for every generation [6]. Higher power consumption in CMOS circuits raises IC temperature and directly affects battery life in portable devices. Higher temperature circuits also require complicated cooling and packaging techniques [3]. The need for devices that consume minimum amount of power and minimum area for various applications is the major driving force behind fabrication of circuits. Since adders are basic block of VLSI and DSP applications, it is very important to design adders that occupy minimum area and reduced power consumption. Different full adder designs are used in VLSI technology according to the requirement of architectures and preferred outputs. Amongst adders 1-bit Full adders are used in applications such as Digital Signal Processors (DSP) Systolic array multiplier architecture, Multipliers (braun array, baugh Wooley, etc.) and adders (Ripple adders, carry save adders, etc) in VLSI application and Microprocessors (ALU, Address generation, etc). In this paper various 1-bit full adder designs are considered, namely 54Transistor CMOS design, 28Transistor CMOS design and 10Transistor GDI design are presented. The 1-bit full adder is designed by using GDI design style whereas the rest of the designs are done in CMOS design style. 10T is advantageous over other designs because of low area consumption when compared to higher gate count full adders [8]. The 1 bit full adder cells are designed using CADENCE Design Suite 6.1.6 and a back end transistor level implementation is made using Virtuoso, ADE, and ASSURA, performance is measured for GPDK 180nm technology and a comparative analysis of the adders is coated here with, Number of transistors/ Gate count, Delay, Power, and Power Delay Product are the prime concern parameters of performance measure in our design, for simplicity and ease of implementation we have not varied the width and length of the MOS devices used.

The rest of the paper is organized as section II provides literature survey carried out on various 1-bit full adder design styles. Section III gives information regarding CMOS and GDI design styles used to

implement 1-bit full adder. Section IV gives knowledge about the various 1-bit full adder designs considered in this paper. Section V consists of results and discussion regarding full adder simulations and the comparative analysis.

II. Literature Review

In [1] the authors have designed 1-bit full adder and performance analysis is carried out for the design styles CMOS, GDI, TG, and GDI-PTL; CADENCE tool is used for design and implementation with GPDK 45nm which differs from GPDK 180nm technology used in this paper and some of the second order effects can be neglected here. In [2] 28T CMOS full adder and 20T TG based full adder circuit is designed in Cadence and , the circuit if 28T full adder CMOS design is considered for one of designs for 1-bit full adder design in this paper. In [3] the power consumption equations for digital CMOS circuits are considered to cognize the power dissipation and delay in CMOS circuits. In [4] the equations for various 1-bit full adder designs is given, this gives a brief idea to understand different ways for designing 1-bit full adders. In [5] the GDI based full adder circuits is presented for low power application.

III. Design styles

i. CMOS design style

A CMOS network consists of pull up network (PMOS transistors) and pull down network (NMOS transistors). The PMOS transistor passes good logic '1' and weak logic '0' whereas the NMOS transistor passes good logic '0' and weak logic '1' to the next level. The output of this network is having full swing and the voltage levels are not degraded (no threshold voltage drop and in some cases body effect may be raised in due to the design). The average power dissipation in a basic CMOS digital gate is sum of the dynamic power, static power and short-circuit power. The dynamic power dissipation of a CMOS circuit depends on parameters such as supply voltage, clock frequency, node switching activities and number of nodes. The reduction in each of above parameters will result in reduction of dissipated power [9].

ii. GDI design style:

The basic GDI cell was first proposed by Morgenshtein [7]. This technique is used for low power and minimum area in digital combinational circuit design. The reduction in power consumption, propagation delay and area of digital circuits in GDI style is done while maintaining low complexity of logic design. One of the significant differences between CMOS and GDI based design is that the source of PMOS in a GDI cell is not connected to VDD and the source of NMOS is not connected to GND (ground) [5]. Every GDI cell consists of 3 inputs – C (common gate input for NMOS and PMOS), F1 (input to the source/drain of PMOS and F2 (input to the source/drain of NMOS).

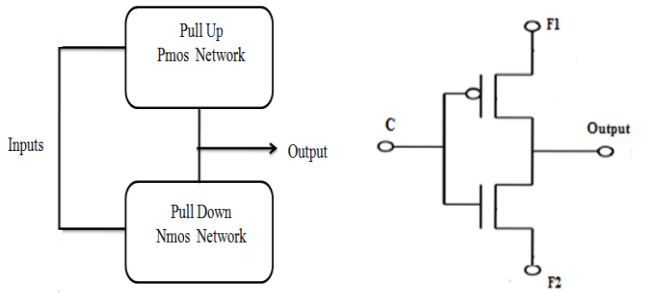

Figure 1. Pictorial representation of (a) CMOS design style and (b) GDI design Style

IV. Full adder design using different design styles

Basics of Full adder

A full adder performs addition of two single bits with carry in as third input. The result of addition at each position in 1-bit full adder is given by SUM bit and a Cout (carry-out) bit. For inputs A, B and Cin output of the full adder is Sum and Cout. Figure 2 gives the block diagram of 1-bit full adder and table 1 gives the truth table of 1-bit full adder. The equations for sum and carry out is given in (1) and (2). It is possible to derive many other types of equation based on the sum and Cout outputs of full adder.

Sum=A**XOR** B **XOR** Cin…… (1)

CarryOut=(A **AND** B) **OR** (B **AND** Cin) **OR** (Cin **AND**)……. (2)

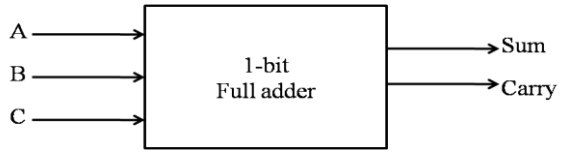

Figure 2: Block diagram of 1-bit full adder

Table 1:Truth table of 1-bit Full adder				
A	**B**	**Cin**	**Sum**	**Cout**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

i. 10T full adder (GDI design style)

In this method the 1-bit full adder design type is obtained from Sum output from the second stage of XOR circuit and the carry bit (Cout) output is calculated by multiplexing B and Cin. These structure style gives GDI based designed cell two extra input pins to use making GDI style flexible over CMOS design. GDI cell is expensive since it requires twin-well CMOS or Silicon On Insulator (SOI) process to realize. The drawback of GDI design style is degradation in the output signal which is highlighted in the simulation waveform. The number of transistor counts in this full adder 10 transistors. A,B, Cin are taken as inputs and the output of the circuit is taken from the Sum and Carry-out(Cout). From figure 3 we have transistors numbered as 1,3,5,7,9 are PMOS transistors whereas transistors numbered as 2,4,6,8,10 are NMOS transistors.

ii. 28T full adder design (CMOS style):

The conventional full adder based design is obtained using standard CMOS topology consists of pull-up and pull-down transistor offering full-swing output with good driving capabilities. Due to the increased number of transistors, power consumption is high and also use of PMOS transistor in pull-up network results in high input capacitances leading to increased high delay and dynamic power. This design offers reliable low voltage operation and consumes less number of transistors as this implementation is made based on the sum and cout equations provided in (1) and (2) and figure 4 shows the transistor level implementation of the same.

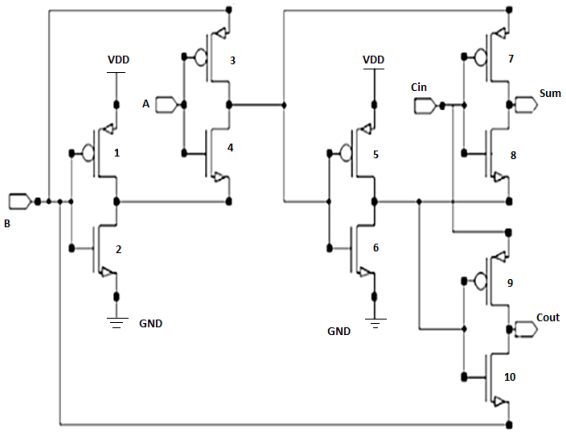

Figure 3: Circuit diagram of 10T GDI design style

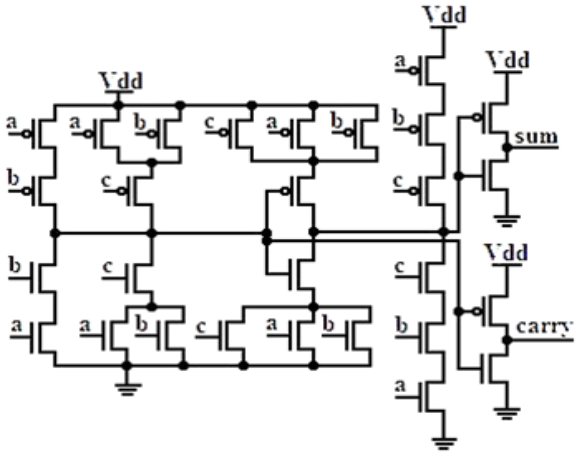

Figure 4: Circuit design of 28T full adder design (CMOS design style.

iii. 54T full adder design (CMOS style):

This is another type of realizing a full adder. CMOS design style is used for designing this 1-bit full adder. The sum output is generated in two level gate delay of XOR gate and Cout output is generated in three level gate delays of AND-OR gate logic, the delay of each gate is different with different logic used to design the given logic.The circuit diagram is shown below:

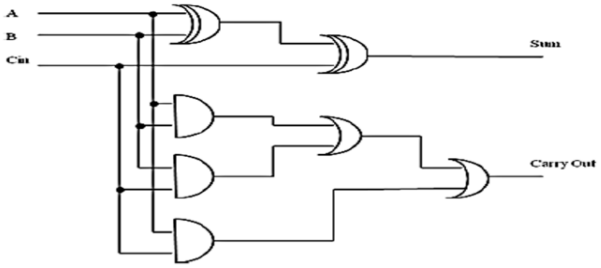

Figure 5: Circuit diagram of 54T full adder design

V. Results and Discussion

Simulation of the full adder design is performed on CADENCE Design Suite 6.1.6 using Virtuoso and ADE environment, all the test inputs are applied to full adder and the result for each case is verified and its output response and voltage levels are noted, in some scenarios the output is degraded not to the extent its logic level is toggled but this voltage level is to be amplified for future stages in some case.

i. Schematic and Simulation Results

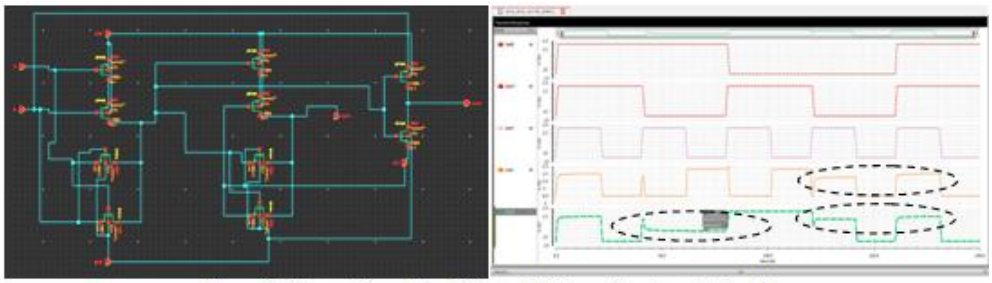

Figure 6. Schematic and Simulation of 10Transistor based full adder

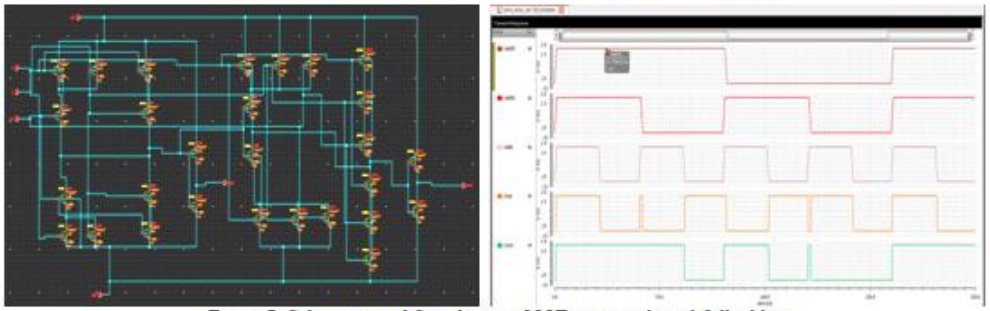

Figure 7. Schematic and Simulation of 28Transistor based full adder

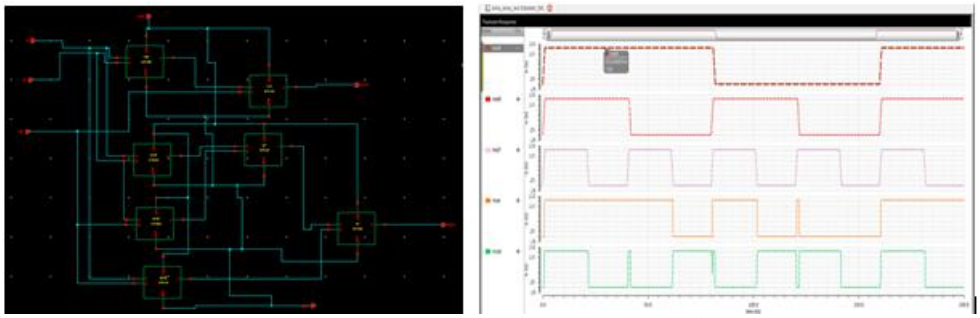

Figure 8. Schematic and simulation of 54Transistor based full adder

ii. Comparative Analysis

In this section we will discuss the results obtained in the design and implementation of the full adder using various techniques, the performance parameters considered are Number of transistors, Delay, Power and Power Delay Product. These measures are important to choose the adder element for a given application, if Area is the prime concern then 10transistor based full adder can be chosen than other design. The overall performance of a 10Transistor design is best suited for given systolic array based architectures as it consumes less area and delay compared to other adders and power consumption is also acceptable as per the comparison made here.

Parameters		***10Transistor Design***	***28Transistor Design***	***54Transistor Design***
Number of Transistor/ Gate count		10 Transistors	28 Transistors	54 Transistors
Static power		636.5e^{-9}W	4.82e^{-6}W	13.21e^{-6}W
Dynamic Power		0.262e^{-6}W	4.50e^{-6}W	12.88e^{-6}W
Total power		0.3743e^{-6}W	0.3194e^{-6}W	0.3206e^{-6}W
Power Delay Product		0.0107e^{-12}	0.275e^{-12}	0.789e^{-12}
Delay	*input to sum*	21.31e^{-9}sec	21.32^{-9}sec	21.32^{-9}sec
	input to carry out	41.01e^{-9}sec	61.31e^{-9}sec	61.31e^{-9}sec
Carry (output) degradation voltage		629.47mv	635.11nv	27.99uv
Sum (output) voltage during OFF cycle		1.24v	41.47nv	110.76nv

VI. Conclusion

This paper effectively shows the results for different 1-bit full adder designs. The results shown can be compared and utilized for designing 1-bit full adder distinctive purposes. The 10T 1-bit full adder design, designed with GDI style is much preferable when the area and delay is prime criteria and well suited for systolic array based applications. The degradation in output voltage clearly is one of the disadvantages which can be overcome by varying the width and length of the MOS devices in the design, in this paper we have not varied the width and length of the MOS devices which for the simplicity and to observe the response when all MOS devices have same width and length. The CMOS design style of full adder designs show a full swing in output with no degradation but consumes more number of transistors and generates more delay. Power delay product is one of the prime criteria for selecting the adders design style, it is clear from the result that the 10transistor design gives best PDP compared to other design.

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