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" A FPGA Implementation of Power Efficient Encoding Schemes for NoC with Error Detection"

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Abstract: *As technology gets smaller, the processor chips become progressively more parallel and the task played by the communication system becomes more important. The communication system accounts for key section of the total thermal energy dissipation in terms of links. The link energy utilization is mainly due to switching activities involved. Hence we propose a set of data encoding schemes in this paper to triumph over these problems encountered. In this paper we also introduce an error detection scheme to check for any mismatches or errors in the encoding-decoding process. We also present in this paper a SRAM memory block to generate the required inputs for the encoding-decoding process. This paper focuses on reducing the self and coupling switching activities through the encoding schemes, to a certain extent that, it would result in substantial reduction in the core thermal energy dissipation. And an error detection scheme sees that an effective error free communication takes place in a communication subsystem. The proposed encoding schemes with error detection technique is coded in Verilog HDL and developed in Altera Cyclone FPGA. The demonstration of the project work has been shown using Modelsim 10.1 Quartus II 11.0 simulator and cyclone FPGA kit.*

Keywords: *Coupling switching, data encoding, error detection, network on chip (NoC), power analysis*.

I. Introduction

With the increase in the degree of compactness of VLSI design, the intricacy of every element in a System-on-Chip increases hastily. In order to meet the wants of real-time applications, recent drift in the sector of embedded systems has been moving in the direction of System-on-Chip multiprocessor. Bus-based interconnection architectures may foil these systems to get together the essential factors like scalability, power, performance, and so forth with the raise in the number of IP modules in System-on-Chip. In order to rise above this setback in multi-core architectures and also to assure signal integrity challenges of next-generation designs Network-on-Chip (NoC) is generally viewed as the vital key.

The basic essence behind this paper is that networking elements are connected via a packet switched communication network on a single chip where link power dissipation is due to the self switching activity and coupling switching activity of the data traversing along the links of a NoC. Hence the data encoding schemes are designed to reduce the self switching and coupling switching activities. The encoding scheme use wormhole switching technique and operates on end to end basis. The implementation of these schemes does not affect the existing components of the communication subsystem. Proposed encoding techniques meets at guaranteeing the obligatory Quality-of-Service, piling up network throughput. SRAM gives the continuous stream of data for encoding process and error detection scheme introduced helps in error free communication.

The rest of the paper is organized as; section II which consists of the related work to this paper where the previously existing encoding technologies are discussed. Section III gives the overview of the proposal. It is further organized into three sub sections consisting of encoding for coupling switching activity, proposed architecture and hardware implementation of the encoding schemes. Section IV consists of results and discussions. Section V gives the future work. Section VI gives conclusion.

II. Related Work

Many related works has been proposed under NoC link power reduction for a communication subsystem that has focused on switching techniques, types, routing techniques etc. This includes encoding techniques reducing the occurrence of pattern " 010" and " 101" i.e. dealing with type II transitions only that makes use of wire shielding. This technique increases the data transfer time, link energy consumption and also increase in overall area **[**1**]**. In the case of correlated data pattern types T0-XOR is used **[**2**].** The gray code types of encoding techniques are used where the power reduction is due to the noise introduced in the links of a NoC which introduces errors in the communication subsystem. A binary to gray code converter and a gray code to binary converter are used at encoder and decoder side respectively [3]. The bus invert encoding techniques are introduced that deals only with odd inversion and self switching activity ignoring the coupling switching activity

[4**].** Techniques presented in **[**5**]** and **[**6**]** have high decoding complexity. Both odd inversion and even inversion methods are employed and the type of the inversion which reduces the maximum switching activity is performed on the flit that is about to traverse on the link **[**5**].**

III. Overview of The Proposal

3.1 Encoding for Coupling Switching Activity

The proposed data encoding schemes is based on 4 types of coupling transitions defined by **[**7**]**

1. One line makes a transition and the other line don' t for a Type I transition (00-10).
2. One line makes a transition from 1-0 and other line makes a transition from 0-1 for a Type II transition (" 01-10, 10-01").
3. Type III transition is when transition of type " 00-11, 11-00" occurs.
4. For a Type VI transition there is no transition happening. (00-00, 11-11)

Coupling transition is analyzed based on set of 2 bits which we call as " flit" . Transition of 2 bits to any other 2 bits will have a total of 16 combinations. From the transition table which shows how the transition gets effected by the odd inversion described in [8], and from the coupling driven encoding procedure presented in [7] which deals with the coupling switching activity, we arrive at the following combinations which can reduce the power when different schemes mentioned here are employed on them.

1. 00 to 00 Type 4 transition
2. 00 to 01 Type 1 transition
3. 00 to 10 Type 1 transition
4. 00 to 11 Type 3 transition
5. 01 to 00 Type 1 transition
6. 01 to 01 Type 4 transition
7. 01 to 10 Type 2 transition
8. 01 to 11 Type 1 transition
9. 10 to 00 Type 1 transition
10. 10 to 01 Type 2 transition
11. 10 to 10 Type 4 transition
12. 10 to 11 Type 1 transition
13. 11 to 00 Type 3 transition
14. 11 to 01 Type 1 transition
15. 11 to 10 Type 1 transition
16. 11 to 11 Type 4 transition

Here wormhole routing is employed and the scheme operates on end to end basis. The probability of occurrence of Type I and II transitions for a random set of data is 1/2 and 1/8 respectively. Hence type I transition weighs more than type II which weighs more than type III. The transition type III accounts for 2 bit change and hence plays a vital role in coupling switching power dissipation. Hence reduction of type I, type II and type III transitions results in considerable reduction in link power reduction and such transitions has to be reduced.

3.2 Proposed Architecture

The proposed architecture comprises of a SRAM block, encoder block, decoder block and an error checking block. The SRAM block here generates the necessary input data for the encoder block on which the encoder performs the encoding operation. The encoder has two inputs. (The flit that is about to traverse along the link (x) and the flit that that has previously traversed along the link (y) of a NoC).If the encoding operation has been performed on the flit, the select line (sel line) goes high indicating, decoder in the next Network Interface has to decode the encoded flit, if select line is low then the decoder output is the encoder input. The decoder output is then compared with the encoder input for any loss of data or the error induced while transmission along the link. If any mismatch in data found then the error detection bit(ED) goes high.

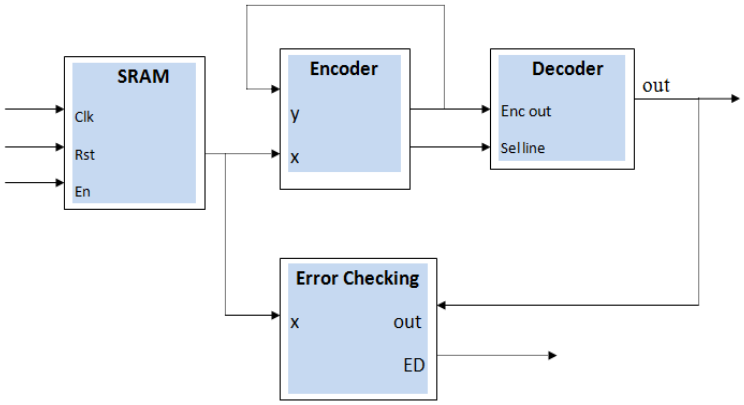

Fig. 3.1: Proposed Architecture

For this architecture 3 schemes are suggested. From the data encoding schemes proposed in [8] we have

- In **Scheme 1** only odd inversion is done.
- In **Scheme 2** odd as well as full inversion is done.
- In **Scheme 3** odd, full as well as even inversion is also taken into account.

3.2.1 Scheme I

In scheme I, we focus on reducing the type I transitions only. SRAM provides a continuous stream of data to the encoder in each cycle of time. The present flit about to traverse and previously traversed flit (8 bits each) along the link of a NoC is grouped into two bits each and given to the each Ty block (Ty1=x1x0y1y0, Ty2= x3x2y3y2, Ty3= x5x4y5y4, Ty4= x7x6y7y6) [8]. If Ty bock finds a transition of type I (in the 16 combinations mentioned in coupling switching activity section), it sets its output bit to high. A 4bit vector is obtained from the Ty blocks consisting of ones and zeros. The decision block checks if the number of the ones in the vector is greater than number of zeros. If this condition is satisfied odd inversion is performed on the flit that is about to traverse along the link. Decoding is performed at the decoder block. At the end encoder input(x) is compared with decoded output to check for error.

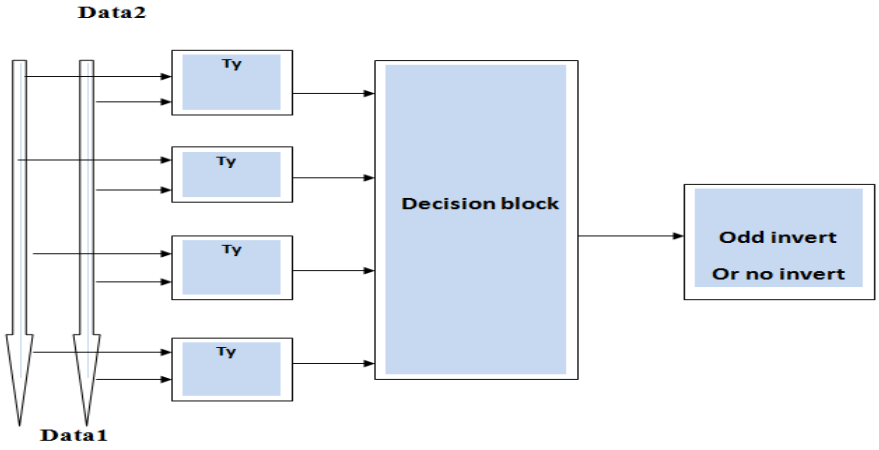

Fig. 3.2: Proposed Architecture for Scheme I

3.2.2 Scheme II

In scheme II, we focus on reducing the type I, type II and type III transitions. . SRAM provides a continuous stream of data to the encoder in each cycle of time. The present and previously traversed flit (8 bits each) along the link of a NoC is grouped into two bits each and given to the each T_y, T_2 and T_4^{**} blocks. If T_y bock finds a transition of type I, T_2 bock finds a transition of type II and T_4^{**} block finds a transition type III (in the 16 combinations mentioned in coupling switching activity section), it sets its output bit to high. A 4bit vector is obtained from the T_y, T_2 and T_4^{**} blocks consisting of ones and zeros.

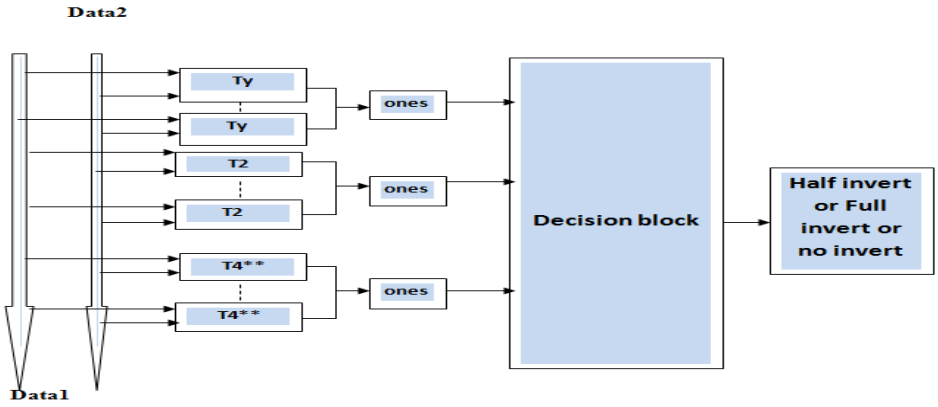

Fig. 3.3: Proposed Architecture for Scheme II

Now, defining [8] the odd inversion condition is obtained as:

$$2(T_2 - T_4^{**}) < 2T_y - w + 1, \qquad T_y > \frac{(w-1)}{2} \quad \ldots\ldots (1)$$

If condition (1) is satisfied odd inversion is performed on the flit that is about to traverse along the link. The full inversion condition is obtained as:

$$2(T_2 - T_4^{**}) > 2T_y - w + 1, \qquad (T_2 > T_4^{**}) \quad \ldots\ldots (2)$$

If condition (2) is satisfied full inversion is performed on the flit that is about to traverse along the link. If equation (1) and (2) is not satisfied then no encoding is performed. Decoding is performed on the decoding side. At the end encoder input(x) is compared with decoded output to check for error.

3.2.3 Scheme III

Here we focus on reducing the type I, type II and type III transitions as that in scheme II but involves even inversion in addition to the inversion schemes in scheme II. SRAM provides a continuous stream of data to the encoder in each cycle of time. The present and previously traversed flit (8 bits each) along the link of a NoC is grouped into two bits each and given to the each T_y, T_2, $T_4^{**}$and $T_e$blocks. If T_y and $T_e$bock finds a transition of type I, T_2 block finds a transition of type II and T_4^{**}bock finds a transition type III (in the 16 combinations mentioned in coupling switching activity section), it sets its output bit to high. A 4bit vector is obtained from theT_y,T_2, $T_4^{**}$and $T_e$blocks consisting of ones and zeros.

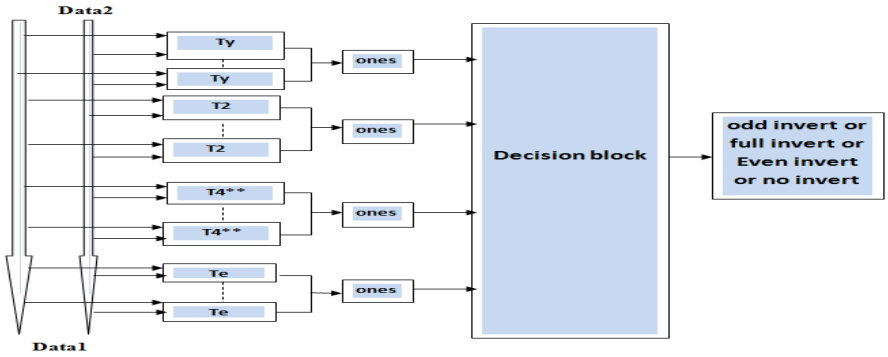

Fig. 3.3: Proposed Architecture for Scheme III

The even inversion is performed on satisfying the condition: [8]

$$T_e > \frac{(w-1)}{2}, \qquad T_e > T_y, \qquad 2(T_2 - T_4^{**}) < 2T_e - w + 1 \quad \ldots\ldots (3)$$

The full inversion and odd inversion is performed on satisfying the condition, (2) and (1) respectively. If none of the above conditions are satisfied then no inversion is performed.

3.3 Hardware Implementation of the Encoding Schemes

The hardware implementation is done on the Cyclone-EP1C3T144C8 FPGA kit. The eight LED' s glow (six on the FPGA and two on the circuit setup on breadboard) indicating the 8-bit output of encoder. The red LED indicates an Error Detection bit which remains OFF indicating there is no error in the decoded data. Since the input data to the encoder is continuous stream of values coming from a SRAM block and these streams of values are encoded in the each successive cycle with a time gap of 0.1nsec and a frequency of 50MHz it is not possible to differentiate the transition in the states of the output happening on the LED' s by the human eye and hence the LED' s remains in the on state continuously. In order to preserve the data transfer speed frequency is kept low.

IV. Results and Discussion

4.1 Scheme I

For scheme I, when both the enable and reset control signals are high the odd inversion is performed. The encoded data appears after three cycles from the input, were three cycles are utilized for storing the encoder input from the SRAM into registers, calculation of vector, the count for ones and zeros(sel line goes high if encoding is to happen). The fourth cycle from input gives decoded output. The encoder input is transferred from cycle 1 to cycle 5 so that it can be compared with the decoded output at cycle 5. If any mismatch found the ED signal goes high in the cycle 6 of the clock cycle.

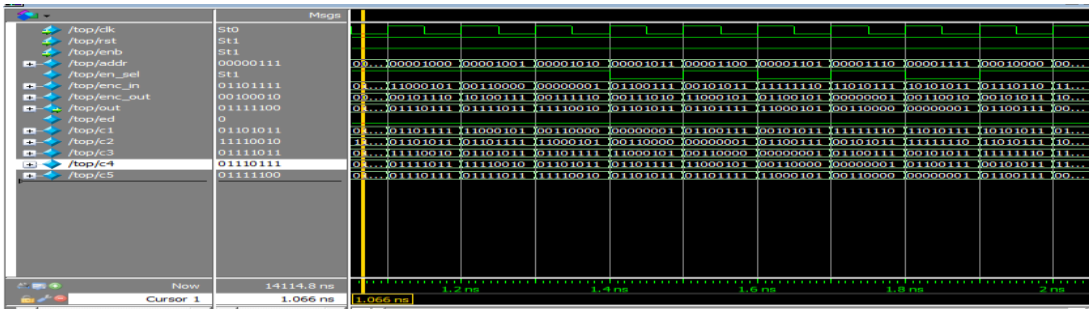

Fig. 4.1: Simulation Results for Scheme I

4.2 Scheme II

Scheme II follows the same procedure as that of scheme I. In scheme II the " 00" value of sel line indicates the encoder input is neither half inverted nor full inverted, " 01" value of sel line indicates the encoder input is half inverted, " 11" value of sel line indicates the encoder input is full inverted at the 4th cycle from the encoder input.

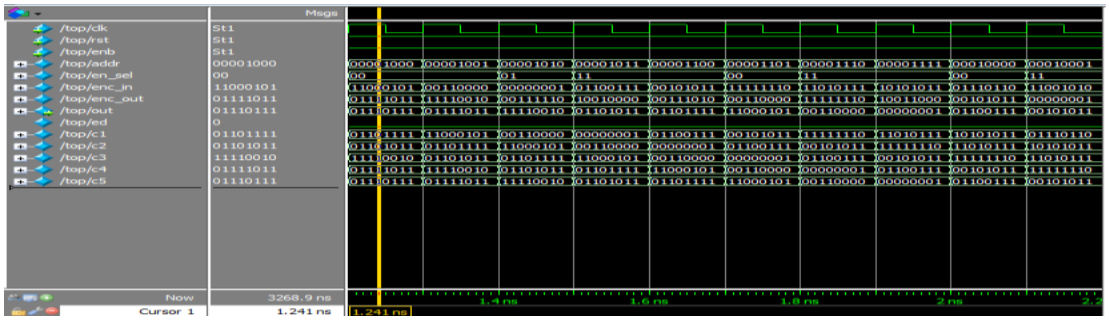

Fig. 4.2: Simulation Results for Scheme II

4.3 Scheme III

Scheme III follows the same procedure as that of scheme I. In scheme III the " 00" value of sel line indicates the encoder input is neither half inverted nor full inverted, " 01" value of sel line indicates the encoder input is half inverted, " 10" value of sel line indicates the encoder input is even inverted and " 11" value of sel line indicates the encoder input is full inverted at the 4th cycle from the encoder input.

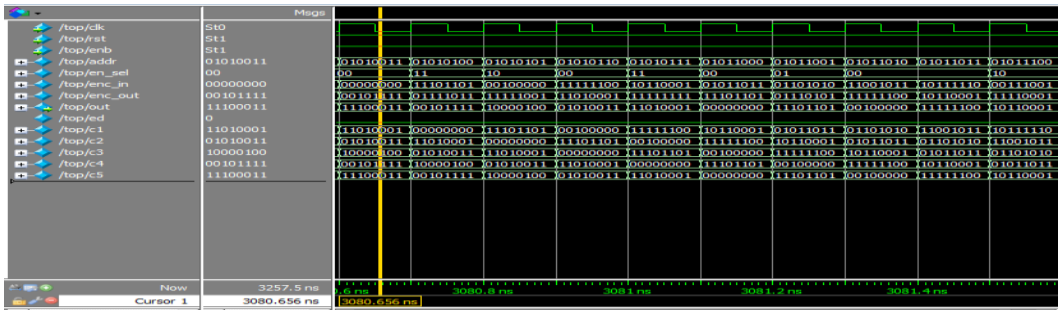

Fig. 4.3: Simulation Results for Scheme III

4.4 Area and power comparisons

Schemes	Total logic elements	utilized	Percentage (%)	Core dynamic(mW)	Core static(mW)	Core I/O(mW)	Total(mW)
Bit Based	2910	300	10	0.12	48.00	34.02	82.15
Scheme I	2910	284	10	0.13	48.00	33.52	81.65
Scheme II	2910	325	11	0.12	48.00	31.36	79.48
Scheme III	2910	344	12	0.11	48.00	29.95	78.07

Table. 4.1: Area and power comparisons

4.5 FPGA Implementation Results on Cyclone Kit

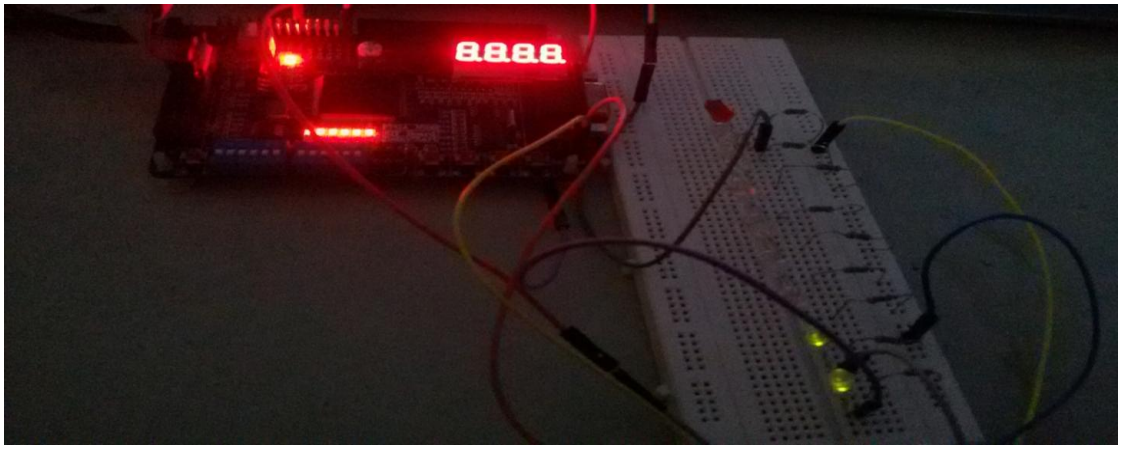

Fig. 4.4: FPGA Implementation Results on Cyclone kit and Breadboard.

4.6 FPGA Implementation Flow Summary

Schemes	Total Logic Elements	Total Pins	Total Memory Bits
Scheme I	294/2910 (10%)	12/104 (12%)	24/59904 (< 1%)
Scheme II	335/2910 (12%)	12/104 (12%)	24/59904 (< 1%)
Scheme III	354/2910 (12%)	12/104 (12%)	24/59904 (< 1%)

Table. 4.2: Hardware implementation Flow Summary

V. Future work

Going ahead with this work and previous work these schemes and techniques can be expanded in similar fashion. Instead of comparing 2 bits transitions to 2 bits transitions it can be implemented for comparing 3 bits transitions to 3 bits transitions or may even be 4 bits transitions to 4 bits transitions. But if it is implemented for 3 bits to 3 bits transitions and 4 bits to 4 bits then the number of comparisons would be 64 and 256 respectively, which in turn would require more registers and gates which can be even increased to such extent that the power reduction using encoding technique will be subdued by the power consumed due to increased area and gates, which clearly is not an advantage. On similar grounds this technique can be used for implementation of 16 bit or higher number of data bits in transmission, but it would again require more number of registers and gates, and will eventually increase the area and hence again the power reduction technique may not be efficient.

VI. Conclusion

The proposed data encoding schemes aims at plunging both the self switching and the coupling switching activity of the links of a NoC which is very much vital criteria for the current communication subsystem. These schemes can be employed in any multi-core SoC architectures which would serve the many purposes like wearable laptops, embedded processors etc. The data encoding schemes presented are transparent with respect to primary NoC fabric. Scheme III provides the smallest amount of power dissipation when compared to scheme I and scheme II and hence is the most efficient scheme. The proposed architecture is coded using VERILOG language and is simulated and synthesized by means of Modelsim software and is also tested on a cyclone board for hardware execution.

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