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Double Gate Heterostructure Based Tunnel FET with 51.5 mV/decade Subthreshold Slope

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Abstract: *This paper presents design of a Double Gate (DG) heterostructure based tunnelling FET with Subthreshold less than 60 mV/decade. The designed DG-FET has attained the sub-threshold slope (SS) of 51.5 mV/decade and provides on-current of 1.93 nA/μm^2 for Si_3N_4 as tunnel dielectric material. Due to non-similar doping of the regions there is no ambipolarity in the device characteristics which further reduces the off currents by 9.29fA/μm. The on-current in this structure can be enhanced by increasing the height of the source region. Low threshold voltage (V_{th}) is achieved due to the band to band tunnelling through thin dielectric. At 4nm the threshold voltage (V_{th}) is 0.301 V and at 1 nm it lower downs to 0.131 V but at the cost of increased subthreshold slope. The designed structure successfully achieves a high I_{on}/I_{off} ratio of 2.07 x 10^5 for a gate dielectric thickness of 4nm. It has been observed that as thickness of gate dielectric is scaled down to 1nm, the I_{on}/I_{off} ratio degrades to 1.538 x 10^2 due to sharp increase in I_{off} current.*

Keywords: *Double Gate (DG), Tunnel FET (TFET), Subthreshold Slope (SS), Heterostructure, Threshold Voltage, I_{on}, I_{off}.*

I. Introduction

As the scaling of MOSFET is happening at a large scale there is need of exploring new devices which employ tunnelling to drive ON-current. In tunnelling devices ON and OFF current drives just by varying the gate voltage and due to band-to-band tunnelling causes transition from ON state to OFF state [1]. The tunnelling field effect transistors fall in class of steep slope transistors having a subthreshold swing less than 60 mV/ decade [2]. The tunnelling transistors with steeper sub-threshold swings can fulfil OFF current requirement at lower supply voltages than conventional MOS transistors resulting in reduced OFF state leakage and power dissipation at the same voltage. Supply voltage scaling can be regained by lowering the sub threshold swing of transistors [3]. Thus, the TFET concept has received much attention in past few years. Thus, tunnelling FET emerged as a very interesting candidate for quasi-ideal switch. It can be used for low power consumption applications owing to its reduced OFF current and where a very low threshold swing is required [5]. The tunnelling mechanism also helps for low power consumption. The carrier must have to tunnel through barrier when the device is turned ON in order to make current to flow between drain and source. It possess very large barrier for carriers when this device is turned OFF, by which carriers does not flow through the barrier [6]. Hence, between drain and source region there is no flow of current in OFF state. The OFF-current in case of tunnelling FET is very low as compared to conventional MOSFETs [7].

Tunnel FETs are p-i-n structured. The device operation requires reverse bias to realize tunnelling phenomenon between source and drain regions with a sufficient level of gate voltage [8]. In n-type TFET, the drain is n-type and source is p-type with a positive voltage applied across gate while converse is true for p-type TFET. The energy bands in the intrinsic region below gate are lifted up on application of negative gate voltage and the energy barrier come close enough for band to band tunnelling process to occur between valence band of intrinsic region and conduction band of n^+ region [9]. Similarly, on application of positive gate voltage, the energy bands are pushed down in intrinsic region resulting in tunnelling phenomenon between valence band of p^+ region and conduction band of intrinsic region. Also, the width of the energy barrier between the p^+ region and intrinsic region significantly impact the TFET's ON current. The tunnelling current depends exponentially on width of the energy barrier between the regions. At high values of gate voltage (V_{gs}), the width of the barrier starts saturating [10]. The function of the gate electrode in this device is to regulate the potential of i-region so that it can regulate the tunnelling phenomenon from the source to the channel region [11].

In this paper, section II presents work carried out by other researchers in field of tunnel FETs. Section III describes design of the heterostructure based Double Gate Tunnel FET and its operation. Section IV illustrates simulation results and analysis of the designed DG-FET. Conclusions are covered in section V.

II. Related Work

D. J. Pawlika *et al*. presented fabrication and characterization of a sub-micron Esaki tunnel diode. They described the operation of tunnel devices in which band to band tunnelling mechanism occurs in the n++ source to the p++ drain [12]. Jang Hyun Kim *et al.* presented a vertical type double gate tunnelling FETs with thin tunnel barrier [13]. They analyzed the effect of large tunnelling area and a thin tunnel junction. To achieve an abrupt subthreshold swing (SS) and a high I_{on} current, tunnelling area on the source side has been enlarged [13]. Zhijiong Luo *et al.* presented an innovative tunnel dielectric-based tunnel FET (TD-FET) structure. In this device structure tunnelling current over the ultrathin dielectric forms the drive currents despite of using band-to-band tunnelling currents to form drive currents [14]. Sang Wan Kim *et al*. presented an illustration of L-shaped tunnel field-effect transistor. They introduced perpendicular to the channel direction band-to-band tunnelling resulting in improvement of more than 1000 times higher ON-current (I_{on}) with the scalable gate overdrive (V_{ov}) of 0.8 V than conventional planar TFETs [15]. Pei-Yu Wang *et al*. presented a new SixGe1-x Epitaxial Tunnel Layer Structure for p-Channel TFET Improvement employing band-to-band tunnelling for its operation. It is a promising device to be used for applications that consumes very low power [16]. Kathy Boucart *et al*. Introduced a DG TFET with high-k gate dielectric. They reported enhancement in this device structure as compared to single gated devices by using a SiO_2 gate dielectric. Gated p-i-n diode is used as the basic design. A high-k dielectric is employed very first time by optimizing its design parameters to achieve I_{on} current of as high as 0.23 mA with the gate voltage of 1.8 V [17]. Motohiko Fujimatsu *et al.* presented a 71 mV/decade of subthreshold slope in vertical TFETs with GaAsSb/InGaAs heterostrutures using a 5-nm-thick Al_2O_3 dielectric [18]. Tejas Krishnamohan *et al*. presented a DG strained-Ge heterostruture TFET over an UT-SOI substrate reporting record high drive currents and less than 60mV/decade subthreshold slope [19]. W. Hsu *et al.* presented modulation-doped gate-normal tunnel FET for improved turn-on abruptness [20]. Shinichi Takagi *et al*. presented III-V/Ge MOSFETs and TFETs on silicon platform for low power logic applications. To meet requirement of advanced ICs consuming low power in the future, CMOS making use of high mobility III-V/Ge channels on Si substrate is perceived to be the best device structures due to their high current drive capability [21]. D. Cutaia *et al*. introduced fabrication and analysis of vertical p-type InAs-Si Nanowire Tunnel FETs inside nanotube templates [22]. Kathy Boucart *et al.* presented DG Tunnel FET with ultrathin silicon body and high-k gate dielectric. The simulations results report significant improvement in many characteristics as compared to single-gated Tunnel FET [23]. Kevin J. Yang *et al.* presented MOS capacitance measurements for high-leakage thin dielectrics [24].

III. Device Structure And Operation

Scaling of the MOSFET was done at a large scale so as to achieve high performance but as the scaling increases it leads to some critical problems related with power consumption. The techniques to meet low power consumption requirements can be achieved either by lowering the operating voltage or by reduction in OFF-current (I_{off}). But, to lower the operating voltage it is also required to scale down the subthreshold voltage and subthreshold slope (SS). Hence, the device structure having subthreshold slope and subthreshold less than the conventional MOS transistors will be a promising candidate for future circuits and systems. Among all such devices TFETs are considered as best. The L-shaped TFET structure achieved subthreshold slope of 50 mV/dec employing thin tunnelling barrier and wide tunnelling region. This L-shaped TFET uses the technique of selective epitaxial growth (SEG). Thus, it has been observed that SEG layer results in small subthreshold slope and high ON-current. This work employs a vertical shaped TFET structure using a 3D structure. The Figure 1 shows basic structure of the Double Gated FET. The Figure 2 shows structure of the Double Gated hetero-structure based TFET. The channel region is of 40 nm. The gate dielectric thickness is 4nm. The positive voltage is applied to the drain and gate terminal. When there is no voltage at gate terminal then the energy barrier is much wider in between intrinsic region and p+ region and we can say in this state the device is in off state. But as soon as the positive voltage is given to gate terminal there is decrease in the energy barrier width because intrinsic band will be pushed down narrowing the tunnelling barrier and tunnelling current will start flowing.

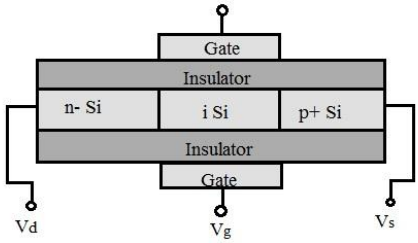

Figure 1 Basic Structure of Double-Gate FET [17]

The performance of a Tunnel FET is mainly evaluated by following parameters:

- **Subthreshold Voltage (V_{th})** When a dielectric of high-k is inserted over the channel then due to the band-to-band tunnelling, there is decrease in the subthreshold voltage (V_{th}) and due to this decreased sub threshold voltage (V_{th}) there will be low power consumption. Thus, lower is the subthreshold voltage, lower will be power consumption. But it also results in increased leakage currents.

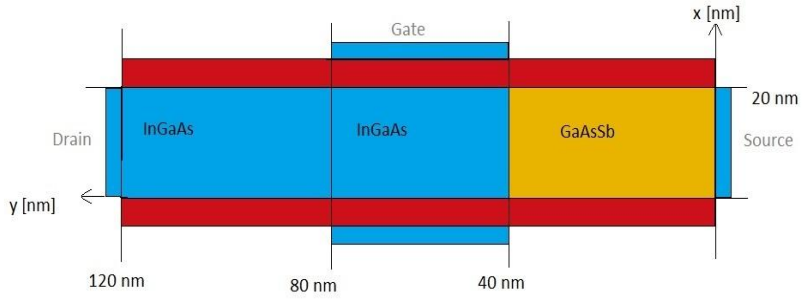

Figure 2 Structure of designed vertical DG-Tunnel FET

- **Subthreshold Slope (SS)** depends on the gate voltage and drain current. Subthreshold voltage for Tunnel FET is less than MOSFET; hence needed power supply will be less resulting in lesser static and dynamic power dissipation. The subthreshold slope is calculated using equation (1).

$$SS = \frac{\eta KT}{q}\ln(10) \quad (1)$$

Here, η is a factor which expresses the efficiency of the gate voltage in changing the semiconductor surface potential.

- **I_{ON}/I_{OFF} Ratio** the I_{on} current should be in the range of 10^{-4} to 10^{-6} A/μm and I_{OFF} current should be negligibly small in range of 10^{-12} A/μm to 10^{-15} A/μm to have higher I_{ON}/I_{OFF} ratio to make it ideal switch. The I_{on} current depends on the width of the energy barrier between the intrinsic and p+ region. Heterostructure materials are used in order to decrease the energy barrier width in the source and the channel junction and higher width in the drain channel junction. Due to this OFF current will be low.

The added gate in double-gated FET enhances the on-current while it does not affect the OFF-current as it remains in the range of fA or pA.

IV. Double-Gate Heterostructure Tunnel FET

In this structure of tunnel FET heterostructure based dielectric has been employed. In such dielectrics the energy band gap of source material has a small value so that during on-state the energy barrier is small and electron can easily tunnel from valence band to conduction band. Drain material has a large value of energy band gap in order to create largest possible value of energy barrier width to keep off current at low value. But it is not obvious that any low band gap material can be taken as source and high band gap material can be taken as drain. In order to make their bands naturally line up with each other at the heterojunctions it is necessary to consider their electron affinities. These material are quite interesting because at two junction independent manipulation of semiconductor properties is allowed. Also using low band gap material at source region increases the ON current in tunnel FETs.

There is improvement in the device characteristics like lower sub-threshold slope by selecting the right kind of gate dielectric. There is increase in the current as the dielectric constant value increases. We have used Si_3N_4 dielectric with physical thickness ranging from 1 to 4 nm. This high-k dielectric material have dielectric constant of 7 and energy band gap of 5.5 eV. By this less OFF-current < 1fA and higher ON-current can be attained at compatible voltage. In Tunnel FET ON-current highly depends on the intrinsic and p+ region energy barrier width.

The Tunnel FET structure in Figure 2 has been designed and simulated. In tunnel FET the 3 regions source, channel and drain are differently doped. In this structure source region is p-type GaAsSb having doping of $3x10^{19}$ cm^{-3} , i-type channel region of InGaAs and drain region is n-type of InGaAs having doping of $1x10^{19}$ cm^{-3}. In order to get minimum OFF current doping of source region has been kept slightly high in comparison to drain region. In between p-type source and i-type channel there is formation of type-II hetero-junction. To avoid any kind of fabrication process the thickness of the regions is kept as 20 nm and width of each region is kept as 40 nm.

Table 2 Doping and material of DG-FET

Region	Doping	Material
Source (p-type)	$3x10^{19}$atoms/cm^{-3}	GaAsSb
Channel (i-type)	$1x10^{17}$atoms/cm^{-3}	InGaAs
Drain (n-type)	$1x10^{19}$atoms/cm^{-3}	InGaAs

V. Results And Analysis

The DG tunnel FET structure has been designed and simulated in Silvaco ATLAS-3D simulator. The energy band diagram shown in Figure 3 of the tunnel FET structure is plotted using ATLAS-3D simulator. The energy band gap of the regions is highly dependent on the type of dielectric and its thickness. The performance of the designed DG tunnel FET structure has been analyzed by varying the dielectric width from 4 to 1 nm. The subthreshold slope, ON-current, and OFF-current parameters have been extracted from simulation results. When the dielectric thickness is 1 nm, the tunnelling distance is smaller near the heterojunctions region. The Figure 4 shows simulated transfer characteristic when the drain voltage V_d is at 0.3 V. There is change in the subthreshold slope as there is change in the thickness of dielectric layer. For 4 nm Si_3N_4, the subthreshold slope of 51.5 mV/decade has been achieved. According to the structure biasing threshold voltage has been calculated. Because if there is decrease in the threshold voltage then device will consume less power due to low power supply requirements.

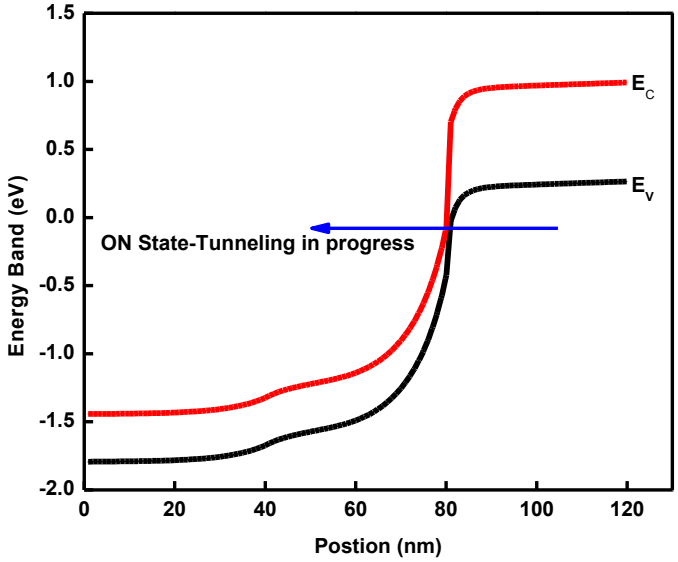

Figure 3 Energy Band Diagram of designed DG heterostructure Tunnel FET

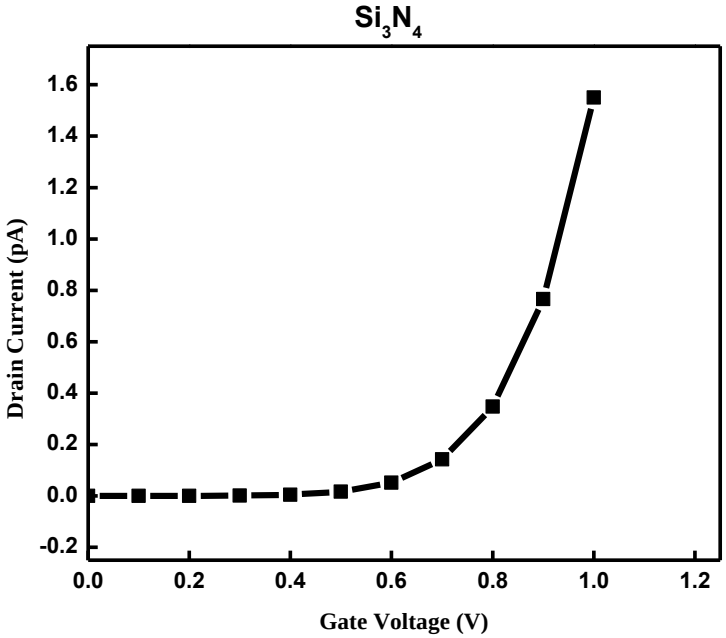

Figure 4 DG-FET transfer characteristics at 4nm

The Figure 5 shows transfer characteristic when the dielectric thickness is varied from 1 to 4nm.

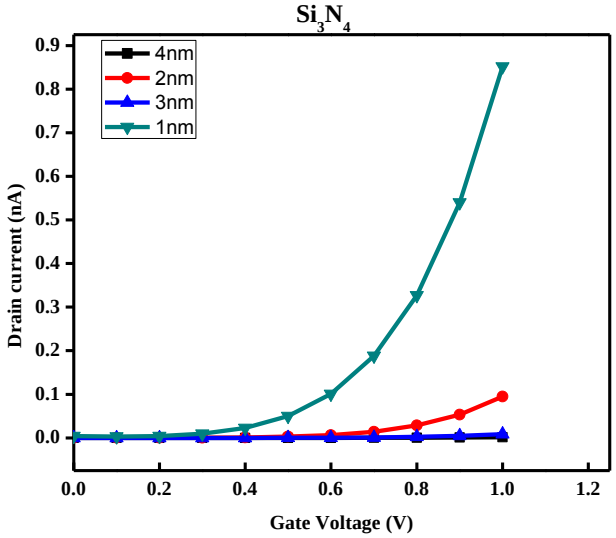

Figure 5 DG-FET transfer characteristics for 4 to 1nm dielectric thickness variation

While varying dielectric thickness from 4 to 1 nm, there is increase in the on-current as well as off-current. In Figure 5 transfer characteristics has been plotted for varying dielectric thicknesses. Subthreshold Slope is steep at 4nm for Si_3N_4 dielectric based DG-Tunnel FET and very low threshold voltage is obtained at 1 nm. Table 3 lists the computed performance parameters of the designed DG heterostructure tunnel FET. It is observed that as the dielectric thickness reduces from 4 to 1 nm, there is sharp increase in subthreshold slope from 51.5 to 267 mV/decade, Ion current increases from $0.193x10^{-8}$ to $0.854x10^{-5}$ A/µm^2, I_{off} current also sharply increase from $0.929x10^{-14}$ to $0.555x10^{-7}$ A/µm^2, I_{on}/I_{off} ratio significantly degrades from $0.207x10^{6}$ to $1.538x10^{2}$.

Table 3 Computed Performance parameters of the DG heterostructure tunnel FET

Parameters	**Dielectric Thickness**			
	4 nm	**3 nm**	**2 nm**	**1 nm**
V_{th}(V)	0.301	0.283	0.198	0.131
SS (mV/decade)	51.5	65.5	243.282	267
I_{on} (A/µm^2)	$0.193x10^{-8}$	1.09310^{-8}	$0.748x10^{-6}$	$0.854x10^{-5}$
I_{off} (A/µm^2)	$0.929x10^{-14}$	$0.128x10^{-13}$	$0.143x10^{-8}$	$0.555x10^{-7}$
I_{on}/I_{off}	$0.207x10^{6}$	$8.544x10^{5}$	$5.217x10^{2}$	$1.538x10^{2}$

Various capacitance parameters such as gate-to-drain (C_{gd}), gate-to-source (C_{gs}) and drain-to-source (C_{ds}) have been extracted from AC analysis of the designed structure. The gate voltage has been varied from 0 to 1 V. The gate-to-drain (C_{gd}) capacitance varies from 1.5 to 4.18 atto Farad, gate-to-source (C_{gs}) capacitance varies from 2.86 to 2.56 atto Farad, and drain-to-source (C_{ds}) capacitance varies from 0.0956 to 0.568 atto Farad as shown in Figure 6, 7, and 8 respectively.

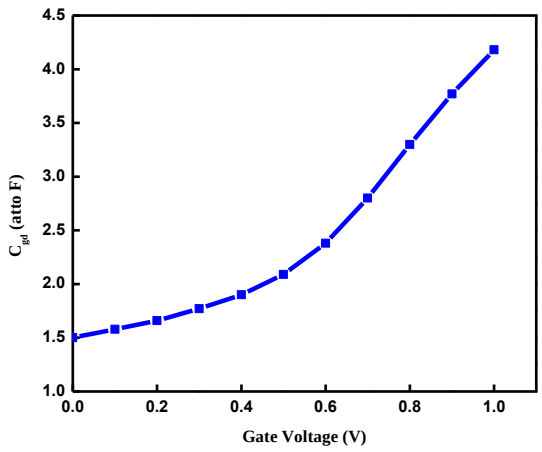

Figure 6 Gate-to-drain (C_{gd}) capacitance at 4 nm dielectric thickness

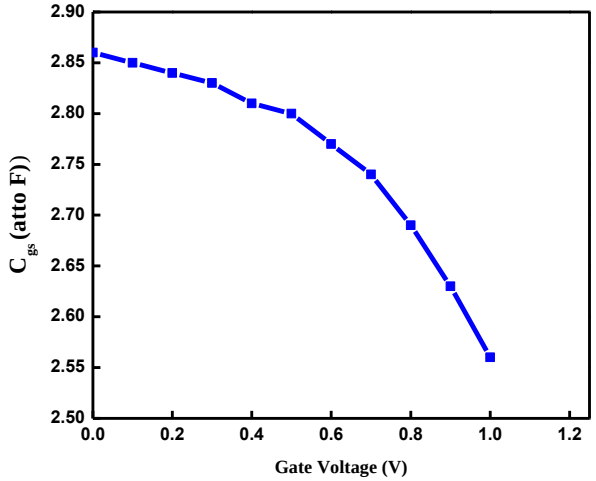

Figure 7 Gate-to-source (C_{gd}) capacitance at 4 nm dielectric thickness

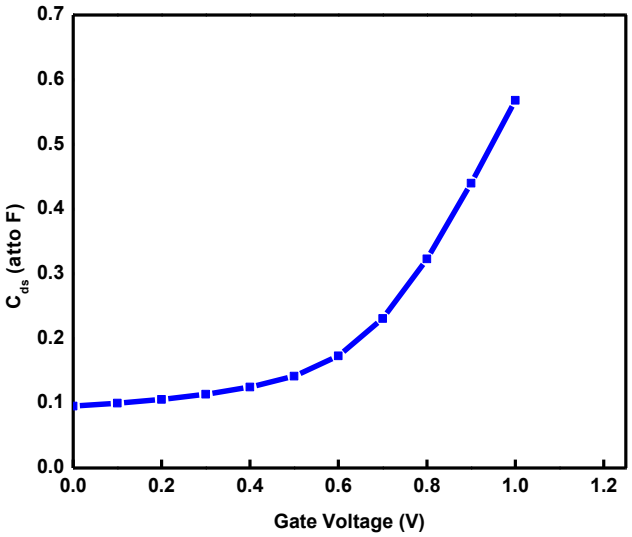

Figure 8 Drain-to-source (C_{ds}) capacitance at 4 nm dielectric thickness

VI. Conclusion

The work investigated the performance of Heterostructure based Double Gate Tunnel FET. It is observed from the output characteristics that by varying the thickness and material used for dielectric, the optimization of I_{on}/I_{off} ratio can be performed. In order to investigate DG-TFET, geometrical and material parameters have been varied. By using heterostructure based material best characteristics has been achieved as the band gap is small near tunnel junction and due to this threshold voltage and ON-current has been improved. Also because of the large band gap near drain region there is decrease in the OFF-current that further reduces power consumption. It is observed that as the dielectric thickness reduces from 4 to 1 nm, there is sharp increase in subthreshold slope from 51.5 to 267 mV/decade, Ion current increases from $0.193x10^{-8}$ to $0.854x10^{-5}$ A/μm^2, I_{off} current also sharply increase from $0.929x10^{-14}$ to $0.555x10^{-7}$ A/μm^2, I_{on}/I_{off} ratio significantly degrades from $0.207x10^{6}$ to $1.538x10^{2}$.

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