Low Power & High Speed Carry Select Adder Design Using Verilog

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Abstract: *The binary addition is the basic arithmetic operation in digital circuits and it became essential in most of the digital systems including ALU, microprocessors and DSP. Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but they lead to increase in area. Carry Select Adder is a compromise between RCA and CLA in term of area and delay. This paper focuses on the design analysis of carry select adder based on Multiplexer using Verilog. The delay (9.970ns) and power (34mW) is minimized. The proposed architecture of carry select adder is simulated in ModelSim6.5b and synthesized in Xilinx ISE14.7.*

Keywords: *Carry select adder, Verilog, Power, delay, Modelsim6.5b, Xilinx ISE14.7.*

I. Introduction

The addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also it serves as a building block for synthesis all other arithmetic operations. In digital adders, the speed of adders is limited by the required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The major speed limitation in any adder is in the production of carries. The carry select adder is used in many computational systems to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. Power consumption is an important efficiency factor in designing very large scale integrated (VLSI) circuit. Moreover with the explosive growth of VLSI technology the demand and popularity of portable devices has driving designers to strive for smaller silicon area. The central electronic circuit used for addition is adder. Adders are fundamental for wide variety of digital system. Many adders exist but the fast adding with Low area and Power still challenging. There are different types of adders such as Ripple carry adder, carry skip adder, carry look ahead adder, carry save adder, etc. among them RCA shows compact design but their computation time is longer. It has lowest speed amongst all adders because it has large propagation delay but occupy less area. Then, in CLA can derive fast result but it leads to increase in area, among these adders CSLA have small area but delay is increased due to ripple carry adder.

II. Proposed work
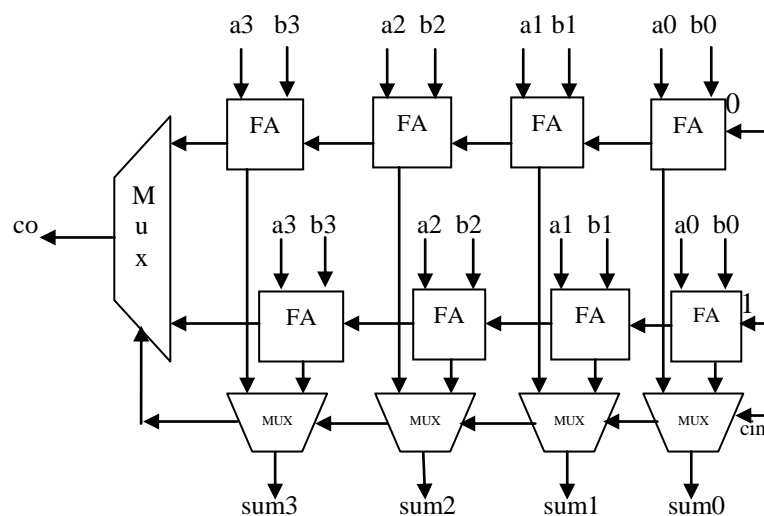
Figure1: Architecture of Carry select adder

The carry-select adder generally consists of two ripple carry adder and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The number of bits in each carry select block can be uniform, or variable When variable, the block size should have a delay, from addition inputs 'a' and 'b' to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out is calculated just in time. The delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of Mux delays. However, the carry select adder is not area efficient because it uses multiple pairs of Ripple Carry Adders to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the multiplexers.

This design has efficiently reduced the delay thereby increasing the speed making it a high speed carry select adder. The factor which are desirable in adders are as follows:

➢ High speed
➢ Low power consumption
➢ Area efficient
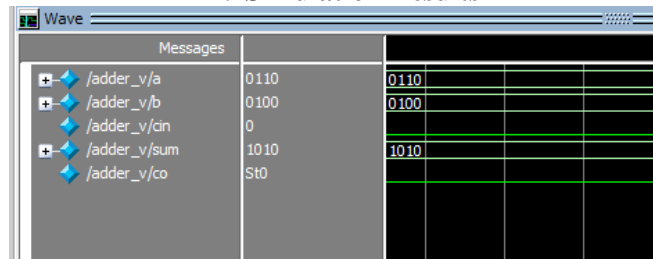
III. Simulation Results

Figure 2: Simulation result of carry select adder in ModelSim6.5b.

The above figure shows the output waveform of carry select adder. Three inputs a, b and cin and two outputs sum and co. Here input a=0110, b=0100 and cin=0 then output sum=1010 and co=0.
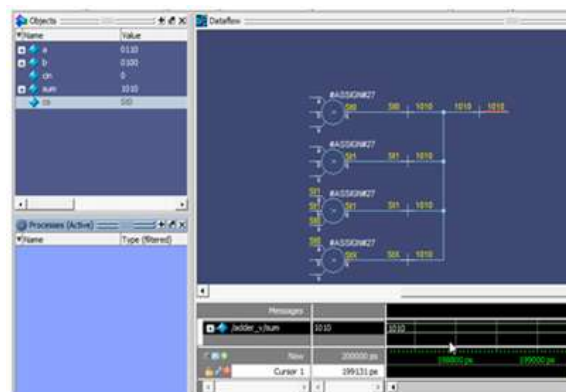

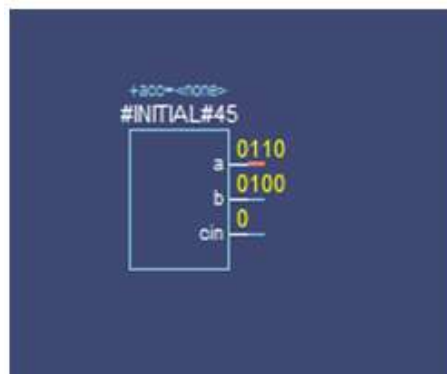**Figure3:** Dataflow model of carry select adder output side in ModelSim6.5b.

Figure4: Dataflow model of carry select adder input side in ModelSim6.5b.
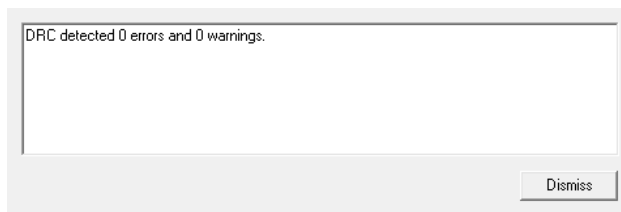
DRC detected 0 errors and 0 warnings.

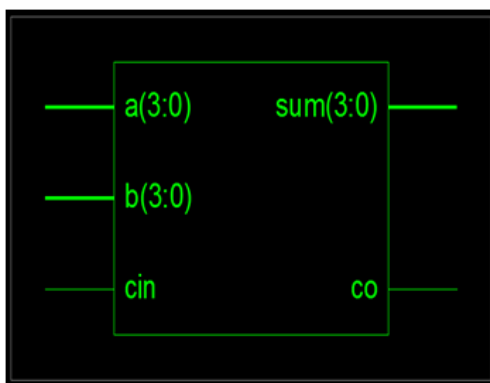Dismiss

Figure5: DRC verified

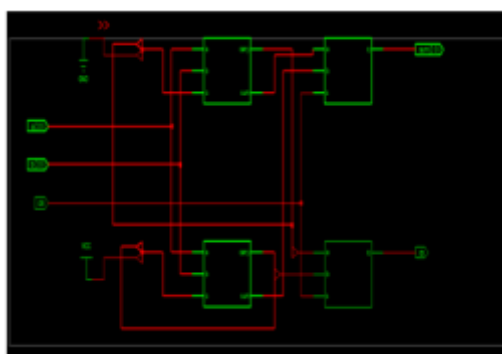**Figure6:** Top module of carry select adder in Xilinx
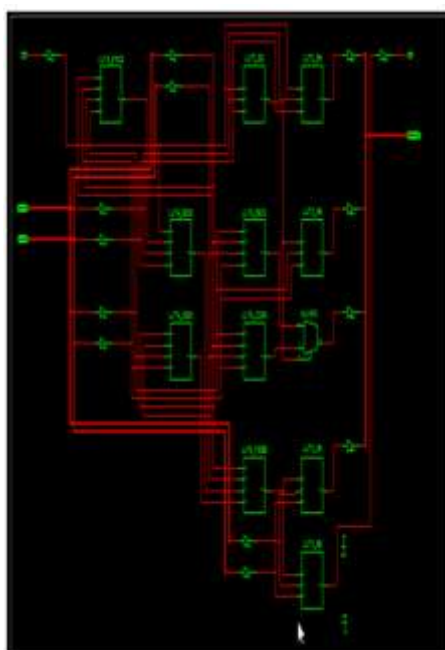
Figure7: RTL Schematic of Carry select adder in Xilinx

Figure8: Technology view map of carry select adder in xilinx

IV. Synthesis results

Power Analysis

Power summary:	I(mA)	P(mW)
Vccint 1.20V:	8	10
Vccaux 2.50V:	8	20
Vcco25 2.50V:	2	4
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	0	0
Signals:	0	0
Quiescent Vccint 1.20V :	8	10
Quiescent Vccaux 2.50V:	8	20
Quiescent Vcco25 2.50V:	2	4
Total estimated power consumption:		34

Figure9: Power summary of carry select adder

Delay Analysis:

Timing constraint: Default path analysis
Total number of paths / destination ports: 49 / 5

Delay: 9.970ns (Levels of Logic = 6)
Source: b<1> (PAD)
Destination: co (PAD)
Data Path: b<1> to co

Cell:in->out	Gate fanout	Net Delay	Delay	LogicalName
IBUF:I->O	5	1.218	0.808	b_1_IBUF
LUT4:I0->O	1	0.704	0.455	x12/q119
LUT4:I2->O	1	0.704	0.499	x12/q124
LUT4:I1->O	2	0.704	0.482	x12/q141
LUT3:I2->O	1	0.704	0.420	x13/q1
OBUF:I->O		3.272		co_OBUF (co)

Total   9.970ns (7.306ns logic, 2.664ns route)
                 (73.3% logic, 26.7% route)

Device utilization summary:
Number of Slices: 6 out of   960   0%
Number of 4 input LUTs: 11 out of 1920   0%
Number of IOs: 14
Number of bonded IOBs: 14 out of   108   12%

HDL Synthesis Report
Macro Statistics
Xors   : 8
1-bit xor3   : 8

Final Report
Design Statistics
IOs   : 14
Cell Usage :
BELS   : 12
LUT3   : 5
LUT4   : 6
MUXF5   : 1
IO Buffers   : 14
IBUF   : 9
OBUF   : 5

V. Conclusion

Delay, Power and area are the constituent factors in VLSI design that limits the performance of any circuit. This paper presents a simple approach to reduce the area, delay and power of Carry select adder architecture. The proposed design of carry select adder is simulated in ModelSim6.5b and synthesized in Xilinx ISE 14.7 and the source code is written in Verilog. This proposed carry select adder has delay 9.970ns and power 34mw.

References

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