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High Gain Amplifier Design for Switched-Capacitor Circuit Applications

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Abstract: *In early decades, CMOS technology made its way into analog circuit design through discrete systems comprised of Switched-Capacitor circuits. Robust amplifier designs made it suitable for multiple applications. Few of these amplifier designs are implemented in this paper to meet the requirements of switched-capacitor integrator circuitries. One of the designs is a Two-Stage OP Amp and another one is Folded Cascode OP amp. Both the designed OP Amps are analyzed and tested for providing optimum Switched-Capacitor performance requirements. In accordance with this design strategy, both the proposed OP amps are optimized with design rules of 0.18µm CMOS technology. Small signal analysis is done in order to achieve the required design parameters.*

Keywords - *Two-Stage amplifier, Folded Cascode amplifier, Miller Compensation, Slew Rate, DC gain, Phase Margin.*

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I. Introduction

The From the last few decades CMOS OP amps have been of interest in designing of analog circuits and systems. Multiple algorithms have been developed in the past which are having signals in mega-hertz range. Single stage amplifier is preferred in various applications as its performance can be tailored easily. It has been found that operational amplifiers are promising in implementing analog circuit design using switched capacitor technique [1, 2]. Operational amplifier is the major component in Switched-Capacitor circuits responsible for maximum power dissipation. Thus, an optimum design of amplifier is necessary for the implementation of analog circuits. Analog designers are well aware of the fact that the aspect ratio and bias of CMOS transistors are their design variable, while design model is the resource to achieve the desired performance of the considered application architecture. Thus, an amplifier can be scrutinized for the purpose of providing deviated performance in a specified area. The main focus of this paper is to optimize the design of the amplifiers for Switched-Capacitor applications, which find huge importance in implementing analog circuit and systems such as filters [3, 4]. The Two-stage Miller compensated (MC) amplifier can have quite large gain and can reduce significantly the Miller effect that would be beneficial for providing improved frequency response as compared to other applications. But the tedious amount of calculations keep the designers away from introducing any further compensation structures as it becomes more complicated to enhance the structure of operational amplifier. Here aspect ratio plays important role in providing deviated performance. The use of complex compensation structures would uncertainly deteriorate the reliability and robustness of the amplifier [5]-[11].
In case of differential Folded Cascode amplifier, high dc gain and amplification can be achieved when the transistors are in saturation region. To ensure this fact bias potential is adapted accordingly. Besides high current consumption the merit of Folded Cascode OP amp is higher output swing, which makes it beneficial for the desired application [12]-[14]. The bulk driven CMOS designs are avoided in case of amplifiers designed for switched capacitor applications as its effective transconductance (g_{mb}) which is four to five times smaller than the gate transconductance.This paper is organized in the following sections. Section II consists of the basic idea about Two-Stage amplifier. Section III comprises of conventional architecture of Folded Cascode amplifier. Section IV and V provides the design equations and parameters of both the amplifiers. Section VI provides the simulation results, to obtain high gain, slew rate and gain bandwidth at lower power dissipation.

II. Conventional Amplifier Designs

a. Two-Stage MC Amplifier

The conventional two-stage amplifier is reviewed in this section and both large signal and small signal responses will be examined thoroughly.

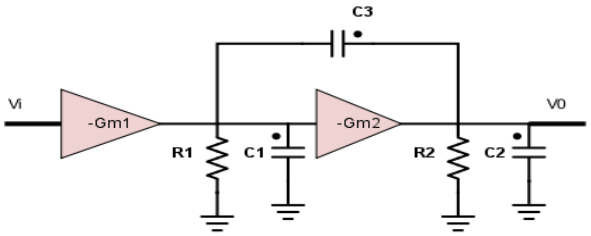

Fig. 1 Two-Stage MC amplifier structure.

Fig. 1 shows the two stage MC amplifier structure. V_i and V_0 denotes the input and output voltages respectively. The output resistance and transconductance of the first and the second stages are R_1 and R_2, as well as G_{m1} and G_{m2} respectively. At the output of first gain stage there is parasitic capacitor C_1.
The transfer function of the two-stage MC amplifier shown in fig. 1 is given by [12].

$$\frac{V_o(s)}{V_i(s)} = \frac{G_{m1}G_{m2}R_1R_2\left(1-s\frac{C_m}{G_{m2}}\right)}{1+sC_mG_{m2}R_1R_2\left(1+s\frac{C_m}{G_{m2}}\right)} \tag{1}$$

Where, $k_mG_{m1}G_{m2}R_1R_2$ is the low frequency gain and the dominant and non-dominant poles are given by $p_1$and p_2, while right half plane (RHP) zero z_{RHP} is given by [12].

$$p_1 = \frac{1}{C_mG_{m2}R_1R_2} \tag{2}$$

$$p_2 = \frac{G_{m2}}{C_0} \tag{3}$$

$$z_{RHP} = \frac{-G_{m2}}{C_m} \tag{4}$$

Phase Margin (PM) of about 60^o can be achieved by keeping the designed gain-bandwidth product (GBW) to half of pole p_2, which means

$G_{m1}G_{m2}R_1R_2\ X\ p_1 = \frac{p_2}{2}$, to obtain [8]

$$GBW = \frac{G_{m2}}{2C_0} \tag{5}$$

And thus the required Compensation Capacitor is given by [8]

$$C_m = 2\left(\frac{G_{m1}}{G_{m2}}\right)C_0 \tag{6}$$

Uncertainly PM is reduced due to z_{RHS} which leads it to be lesser than 60^o. From the later two equations it is clear that, larger the value of G_{m2}, larger will be the GBW and smaller will be the C_m. Therefore PM can be increased by placing the z_{RHS} at higher frequency. The slew rate behavior of the amplifier can be studied from the fig. 2 of typical two-stage MC amplifier design as shown in fig. 2.

The aspect ratio of nMOSFETs and pMOSFETs can be denoted by $(W/L)_N$ and $(W/L)_P$ and 1,2,…,m denotes the size ratio. Input supply voltages are denoted by V_{DD} and V_{SS}. Calculative analysis, such as non-dominant pole, low–frequency gain, current consumption and GBW of the two-stage MC amplifier, based on previous equations are systemized in the following progress.

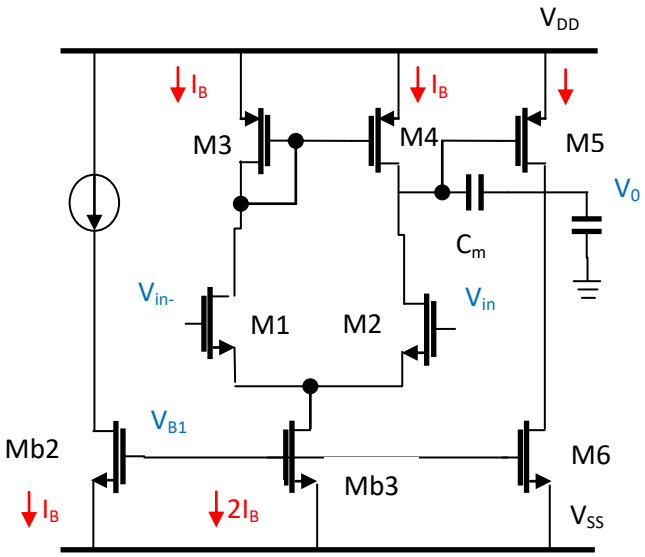

Fig. 2 Two-stage MC amplifier circuit structure.

Gain, non-dominant pole, GBW, slew-rate (±) and IDD are given by equations (7) to (12).

$$gain = g_{m1}g_{m5}(r_{o2}//r_{o4})(r_{o5}//r_{o6}) \quad (7)$$

$$p_2 = {}^{g_{m5}}/_{C_0} \quad (8)$$

$$GBW = {}^{g_{m5}}/_{(2C_0)} \quad (9)$$

$$SR^+ = i_{SD5} - mI_B/C_0 \quad (10)$$

$$SR^- = mI_B/C_0 \quad (11)$$

$$I_{DD} = (m+3)I_B \quad (12)$$

Also, $v_{UO} = v_{i+} - v_{GS2} + v_{VDS2}$, therefore both v_{SG5} and i_{SD5} are dependent on V_i. Based on the required performance characteristics, the two stage operational amplifier is analyzed to produce results applicable to switched-capacitor applications. The gain, GBW, PM and slew rate performance depends on the previous equations discussed in section II. Those can be calculated with the help of the following equations.

$$g_{m1} = \sqrt{2I_B\mu_N C_{ox}(W/L)_1} \quad (18)$$

$$g_{m5} = m\sqrt{2I_B\mu_p C_{ox}(W/L)_p} \quad (19)$$

$$g_{m6} = \sqrt{2I_B\mu_N C_{ox}(W/L)_N} \quad (20)$$

The aspect ratio and conduction capacitor Cc is adjusted in accordance to provide desired results. The aspect ratios can be clearly seen from table 1.

Table 1. Transistor aspect ratio for Two-stage MC OP amp

Transistor Name	W/L
M1, M2	03µ/0.5µ
M3, M4	3.5µ/0.5µ
M5	06µ/0.5µ
M6	62µ/0.5µ
M7	53µ/0.5µ

Table 2. Design specification of Two-stage MC OP amp.

Specification	Values
DC Gain (dB)	76
Equivalent Load (C_L-pF)	0.5
GBW (MHz)	33
PM (deg.)	69
Slew Rate (V/µs)	19
Power Consumption (µW)	35

It can be seen from the analysis that as the value of Cc increases noise decreases as well as GBW is reduced, which is not desirable. Thus, a tradeoff between both the parameters will be required for optimization. Also, as current increases, slew rate improves but gain of the device is compromised. For, switched-capacitor integrator based applications, optimum gain and high slew rate is favorable. Therefore, following specifications are obtained from the design optimization, these can be seen from table 2.

b. Folded-Cascode OP amp

Folded Cascode OP amp employs a cascoding at the output stage combined in a remarkable fashion with differential amplifier to achieve fair input common-mode range. Hence a folded cascode OP amp offers good input common-mode range and is self compensated. The benefit with this design is that, keeping each transistor in saturation region is simpler from various other designs [15]. The term "folded-cascode" arises from the fact of reforming nMOSFETs cascode active loads of differential-pair to pMOSFETs. As seen from the fig. 3 M1/M1A and M2/M2A forms two different cascode structures. Differential signal is converted by the current-mirror into single output by the help of M1A, thus forming folded-cascode structure. Bias is obtained by the help of current-sources M11 and M12, which should be larger than $|I_{D5}|/2$. Thus the current equation and output resistance R_o is given by following equations,

$$I_{D1A} = I_{D2A} = I_{D11} - |I_{D5}|/2 = I_{D12} - |I_{D5}|/2 = I_B - I_T/2 \quad (13)$$

$$R_o = (R_{out}|M_{2A})||(R_{out}|M_{4A}) \quad (14)$$

$$R_{out}|M_{2A} = (r_{o2}||r_{o12}) + r_{o2A}[1 + (gm_{2A} + gmb_{2A})(r_{o2}||r_{o12}) \quad (15)$$

$$\approx [gm_{2A}(r_{o2}||r_{o12})]r_{o2A} \quad (16)$$

Similarly, $R_{out}|M_{4A} \approx (gm_{4A}r_{o4})r_{o4A}$ (17)

To optimize the power dissipation, drain current should be reduced but being in proportionality, gain also reduces. Thus, only compromise can be made to reduce the override voltage of each device but keeping in mind the drive enough to have each transistor in saturation region. Therefore, a tradeoff will be the optimized solution.

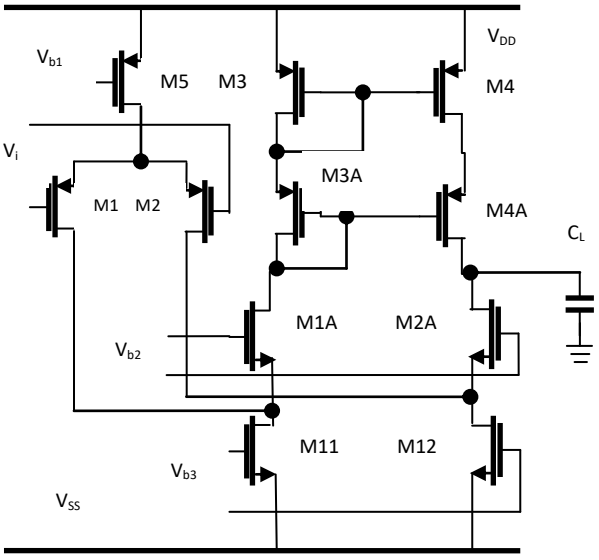

Fig. 3 Folded-Cascode OP amp with PMOS input

Table 2. Design specification of Two-stage MC OP amp

Specification	Values
DC Gain (dB)	76
Equivalent Load (C_L-pF)	0.5
GBW (MHz)	33
PM (deg.)	69
Slew Rate (V/µs)	19
Power Consumption (µW)	35

III. Proposed Amplifier Design

Differential pair being the most significant part in Folded-Cascode OP amp design, requires appropriate matching. In general, OP amp consist of a differential pair in the first stage followed by a common-source design in the second stage to enhance the overall gain but an additional capacitance for frequency compensation is needed which leads to an additional pole in the system. In this proposed design the overall gain is to be generated in the first stage itself. Also, this design is assistant in obtaining low noise. Fig. 4 explains the complete schematic of this differential Folded-Cascode OP amp. This design comprises of pMOSFETs differential layer i.e. M_1 and M_2, which is accompanied by common-gate stages i.e. M_7 and M_8, current sources M_5 and M_6, and a self-biased current-mirror i.e. M_9-M_{12}. Bias current for differential pair is provided by input

pair M_3/M_4. V_{b1} and V_{b2} are bias voltages. To keep all the transistors in saturation region bias voltages are adjusted accordingly. Current equation across M_7/M_8 can be given by $I_a = I_b - I_{ref}/2$. Thus, I_b should be significantly greater than $I_{ref}/2$. I_b is set to 30µA and I_a to 10µA. therefore, the current at the output across the load will be 20µA (i.e. $2I_a$). W/L ratio can be determined mathematically from the following equation

$$I = (1/2)\mu_{N,P} C_{ox} (W/L)_i (V_{OV})^2$$

where, i = 1,2,…

Tuning has to be done to achieve desired specifications. A list of specification and aspect ratio is given in table 3 and 4.

Table 3. Design specification of Diff. Folded-Cascode OP amp

Specification	Values
DC Gain (dB)	73
Equivalent Load (C_L-pF)	1.4
GBW (MHz)	30
PM (deg.)	67
Slew Rate (V/µs)	17
Power Consumption (µW)	66

Table 4. Transistor aspect ratio, Folded-Cascode OP amp.

Transistor Name	W/L
M1, M2	12µ/0.5µ
M3, M4	56µ/0.5µ
M5-M6	32µ/0.5µ
M7-M8	32µ/0.5µ
M9-M12	16µ/0.5µ

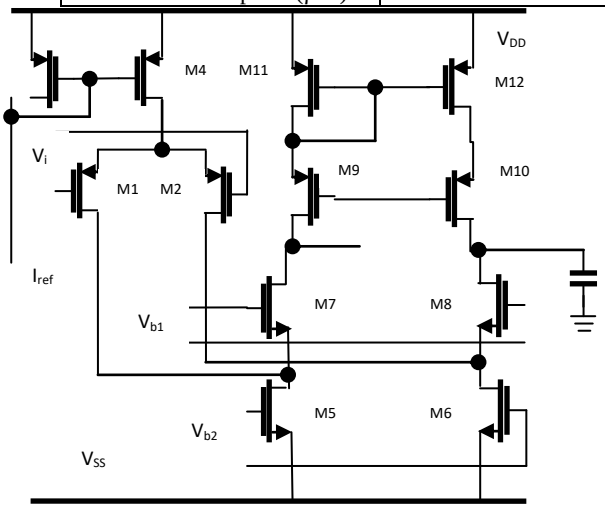

Fig. 4 Proposed Diff. Folded-Cascode OP amp

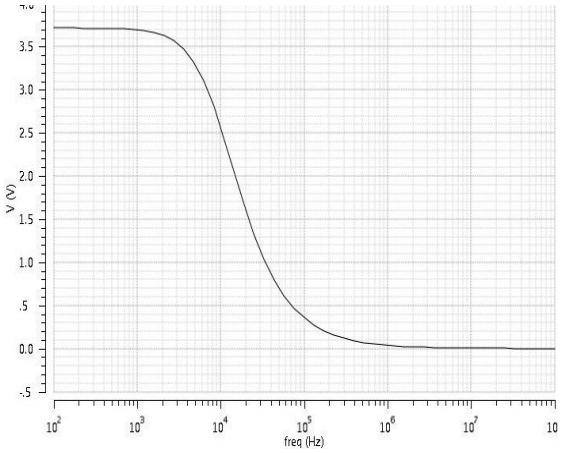

Fig. 5 AC analysis of Two-Stage MC OP amp

IV. Analysis

Simulation is done using 0.18µm CMOS technology. AC analysis, DC gain analysis, phase margin and slew rate calculation of Two-Stage MC OP amp is done using the following obtained waveforms is shown in fig. 5 and 6. Output noise analysis of Two-Stage OP amp is shown in fig. 7. Expressions to calculate the DC gain of Differential Folded-Cascode OP amp is given by the following equations.

$$A_V = G_{m(1,2)} R_o \quad (21)$$

$$G_{m(1,2)} = GBW \times C_L \times 2\pi \quad (22)$$

Where, M_1/M_2 have transconductance $G_{m(1,2)}$. The gain and phase analysis , phase margin and slew rate calculations are done with the help of following waveforms shown in fig. 8 and 9. As it could be clearly seen from the shown analysis that noise is a decreasing function at the output, moreover the size of the OP amp increases on addition of any circuit capacitance. The comparative analysis from [16] is shown in table 5, which shows that few parameters are improved, keeping the desired design responses in concern.

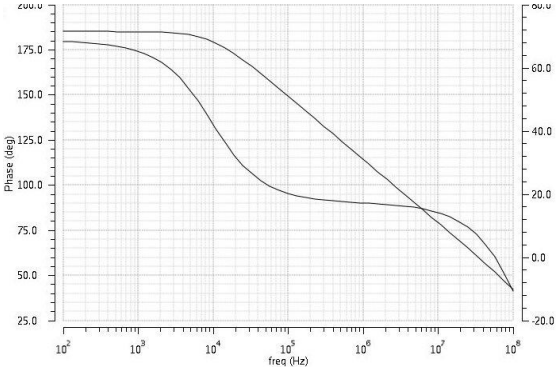

Fig. 6 Gain and Phase analysis of Two-Stage OP amp

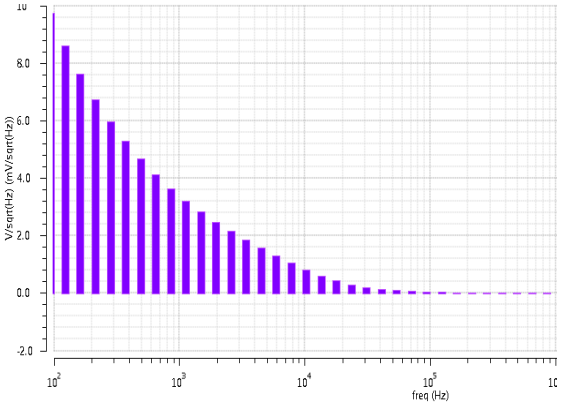

Fig. 7 Output Noise analysis of Two-Stage OP amp.

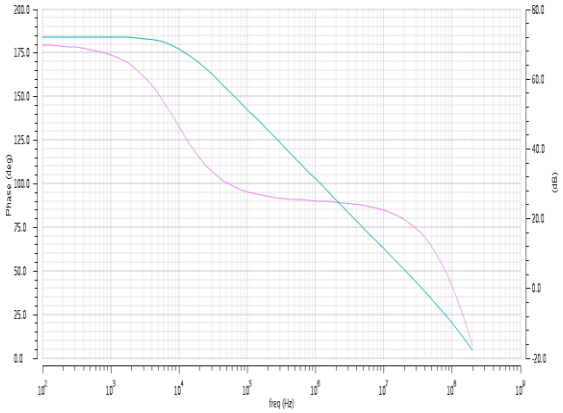

Fig. 8 Gain and Phase of Differential Folded-Cascode. OP amp

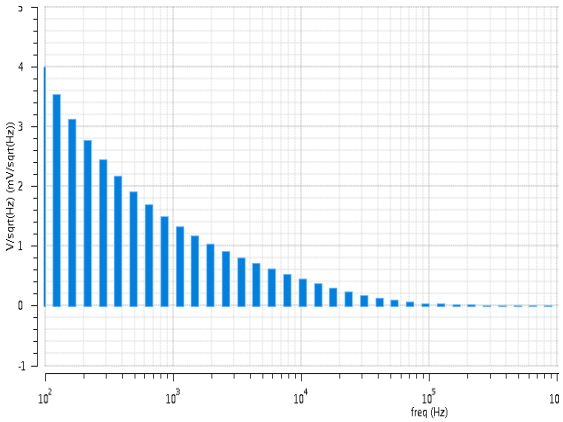

Fig. 9 Output Noise of Differential Folded-Cascode OP amp

Table 5. Comparison table of analyzed designs with previous work.

Specification	OTA 1[16]	OTA 2[16]	Two-Stage OP amp	Diff. Folded-Cascode OP amp
Technology	0.18µm	0.18µm	0.18µm	0.18µm
DC Gain (dB)	68	70	76	73
Equivalent Load(C_L-pF)	1.2	0.56	0.5	1.4
GWB (MHz)	20	27	33	30
Phase Margin (deg.)	80	81	69	67
Slew Rate (V/µs)	13	20	19	17
Power Consumption (µW)	62	31	35	66

amplifiers are giving satisfactory performance in few design parameters. Whereas, a tradeoff will always be there for one or two parameters based on the area of application selected.

V. Conclusion And Future Scope

The OP amp designs analyzed and proposed in this paper are implemented for switched-capacitor circuit based applications. The simulation and analysis is done in 0.18µm CMOS technology. The results can be clearly seen from the comparative table, which shows the an improved gain and slew rate is obtained which is favorable for desired application. As it is clear from various research works, that a tradeoff is always there depending upon the choice of application. The design specification of this paper is based on the application of switched-capacitor circuits. To further improve the design of Two-stage OP amp, multiple gain stages could be added to it. Whereas, in case of Differential Folded-Cascode OP amp, robust structures could be implemented for improving the design parameters.

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