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Process-Simulation-Flow And Metrology of VLSI Layout Fine-Features

George P. Patsis[1*]
[1]*Department of Electronic Engineering, Athens University of Applied Sciences, Aegaleo, Attiki, Greece*
*Corresponding Authour: George P. Patsis1**

Abstract: *Increasing complexity of VLSI designs makes it hard to follow fine details within a large design. Especially in variability studies it is important to be able to determine for example, edge lengths in the x and y direction of mask shapes, within a device or a circuit. The line-edge roughness variation vs. length scales within the circuit is valuable information for the effects of variability of circuit performance. In the current article a simulation flow is presented to help circuit designer, gain more understanding of the fabricated features of their circuits. Is starts from mask files in CIF format and decomposes them into their corresponding layers in order to be used in electron-beam-lithography simulations, stochastic-lithography simulation and line width roughness metrology studies. The code is integrated in a complete software suite.*

Keywords: *Matlab, VLSI, layout, CIF, electron-beam lithography, stochastic-lithography, roughness, metrology.*

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I. Introduction

Caltech Intermediate Format (CIF) is a data file format suitable for the description of integrated circuit layouts [1]. Created by the university community, CIF has provided a common database structure for the integration of many research tools. CIF provides a limited set of graphics primitives that are useful for describing the two-dimensional shapes on the different layers of a chip. The format allows hierarchical description, which makes the representation concise. In addition, it is a terse but human-readable text format. CIF is therefore a concise and powerful descriptive form for VLSI geometryEach statement in CIF consists of a keyword or letter followed by parameters and is terminated with a semicolon. Spaces must separate the parameters but there are no restrictions on the number of statements per line or of the particular columns of any field. There are only a few CIF statements and they fall into one of two categories: geometry or control. The geometry statements are: LAYER to switch mask layers, BOX to draw a rectangle, WIRE to draw a path, ROUNDFLASH to draw a circle, POLYGON to draw an arbitrary figure, and CALL to draw a subroutine of other geometry statements.

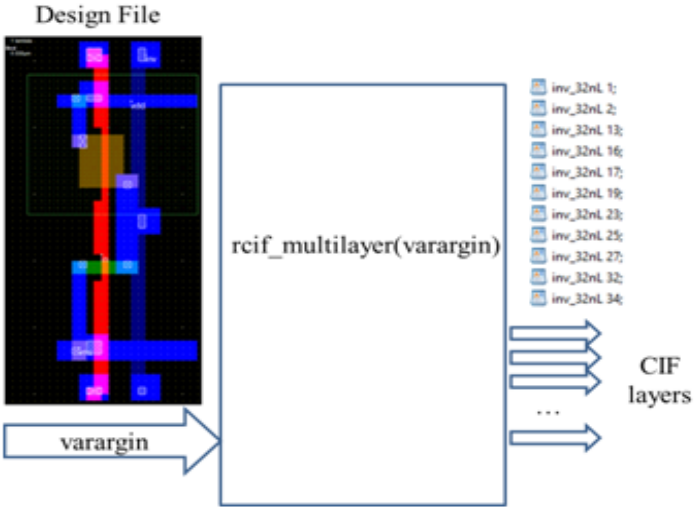
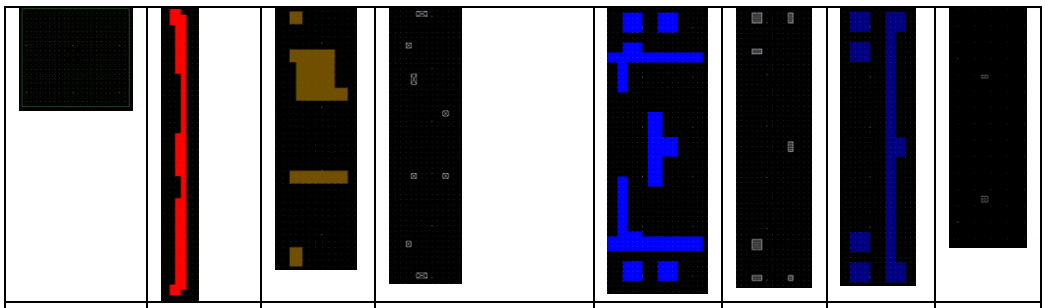


Figure 1. Qualitative modeling flow. (vargin = variable-argument-in)

Figure 1 shows an overall qualitative presentation of the fist step of the current simulation flow. A mask file of a cirguit file (Design File, in this case an inverter-gate) stored in CIF format is provided as input to a Matlab code function (rcif_multilayer.m), which produces a directory containing each mask layer as a separate CIF file.Figure 2 shows the decomposed series of layers (each one saved as a separate text file). Such layer-masks can be imported in the electron-beam lithography simulator developed by the author [2] and produce an exposure-pattern (energy deposition), which can be analyzed for proximity-effects and any type of size-pattern analysis.



1;	L 13;	L 17;	L 19;	L 23;	L 25;	L 27;	L 32;
nwell	**poly**	**diffp**	**contact**	**metal**	**via**	**Metal2**	**via2**

Figure 2. Decomposition of inverter gate into its constituent sublayers.

The complete modeling flow is seen qualitatively in Fig. 3.

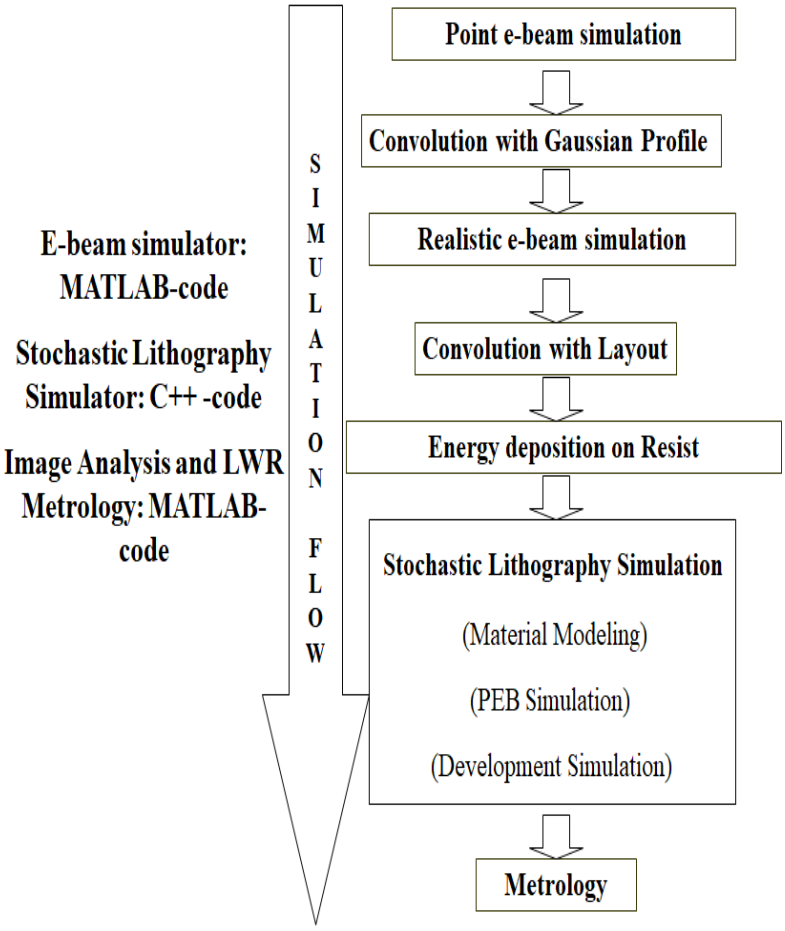


Figure 3. Simulation flow of electron beam exposure to metrology. PEB stands for Post-Exposure Bake.

II. Qualitative Description Of The Proposed Simulation Flow

The starting point is that of electron beam exposure simulation, where electrons are considered as particles colliding with the matter of the photoresist and the substrate. Figure 4 shows qualitatively the modelling approach for the simulation of electron transport in matter. Collisions are random events in the materials found along the electron track. Using a suitable discretization, the energy deposition in the resist and the substrate is obtained [3].

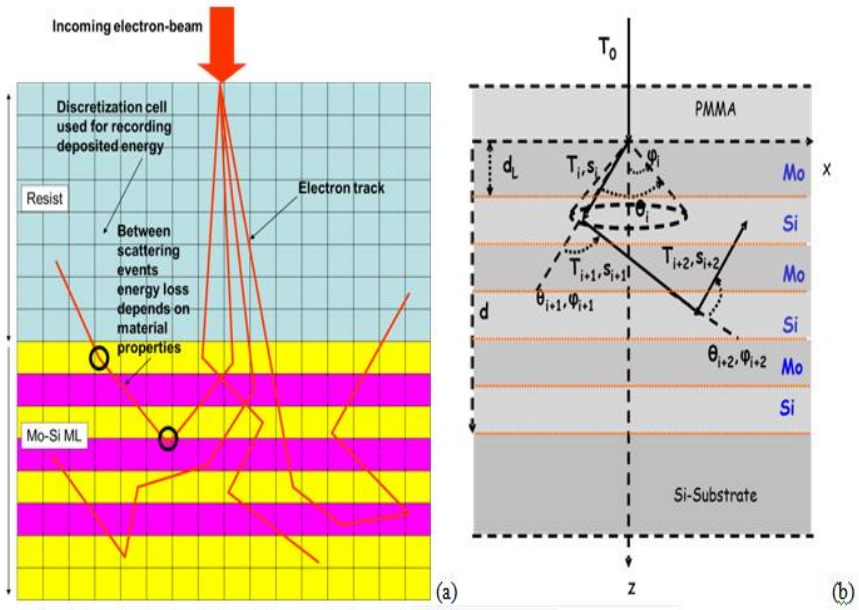


Figure 4. (a) Qualitative description of the electron scattering process and energy deposition in photoresist and substrate (in this case the substrate is considered as a multilayer of Mo/Si layers). (b) More detail in the electron scattering process. T0 is the initial electron energy which dissipates in the resist (PMMA in this case) and in the multilayer substrate, with each collision event.

Figure 5 presents the electron energy deposition function (EDF) in keV/nm^3/electron of an initially E_0=100keV electron beam impigin on 150nm PMMA photoresist on top of 40 layers of Mo/Si. 100000 electron trajectories have been simulated. In order to obtain a realistic electron-beam, the initial point beam is convoluted with a gaussian profile function (with 30nm standard deviation) and the result is also seen in Fig. 5. The multilayer stack was considered in order to check the effect of the increased backscattering attenuation of a high atomic number material (Molybdenum in this case).

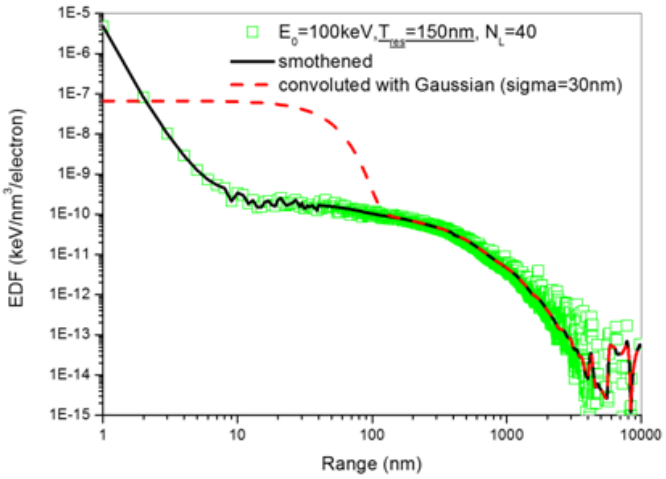


Figure 5. Point-spread function (PSF) squares corresponds to energy deposition function (EDF) for the simulation scenarios of electron-energy and material stack, and the continuous line to the smoothened version of the EDF which is used for convolution with the Gaussian shaped beam. The dashed line is the final Gaussian-convoluted EDF used in the current work for writing the layouts. N_L is the number of Mo/Si layers in the substrate stack.

The patterns were simply closely spaced single exposures. In order to simulate a real beam, this function is then convoluted with a Gaussian profile with sigma matching the experimentally determined one as possible. The effect of convolution on the original point spread function is to smooth and flatten energy deposition from the point of origin up to about beams' sigma (e.g., 30nm). Then is decreasing up to 50-100nm and then again is producing a smooth and slowly decreasing energy deposition tail up to ranges far exceeding 1μm. This tail is due to backscattered electrons from the substrate depositing small amounts of their energy over a long distance from the point of beam origin. The use of a high atomic number Mo layer between resist and silicon substrate, leaves the energy deposition up to 80-100nm range unchanged. In addittion, decreasing by almost two orders of magnitude the deposited energy of the tail, the amount of backscattered electrons from the substrate to reach the resist film is being decreased. The convoluted point spread function is used to expose, point – by – point a desired pattern mask, which is input to the process as a CIF file. The user has to specify only the distance between the adjacent point exposures and the software will do the rest, producing the energy deposition matrix for the corresponding pattern. At this point, one is able to either perform metrology on the energy deposition and obtain a first idea of the final pattern on the photoresist considering a simple on-off dissolution algorithm, or can proceed using more advanced dissolution models (as is proposed here) using an elaborate stochastic lithography simulator which models the photoresist polymeric structure, the post-exposure bake acid diffusion (in the case of chemically amplified photoresists) and the stochastic nature of the development process [4]. Figure 6a shows a front view (with resist depth) of the stochastic lithography simulator. Photoresist's polymer chains are modeld as self-avoiding and mutually excluded random walks in this case. The green color represents the acid diffusion area after post exposure bake simulation in the case of chemically ampliefied photoresists. Edge roughness is seen in this case after development. Figure 6b shows a top-down view of a photoresist area, with acid diffusion profile, and Fig. 6c, the profile after dissolution.

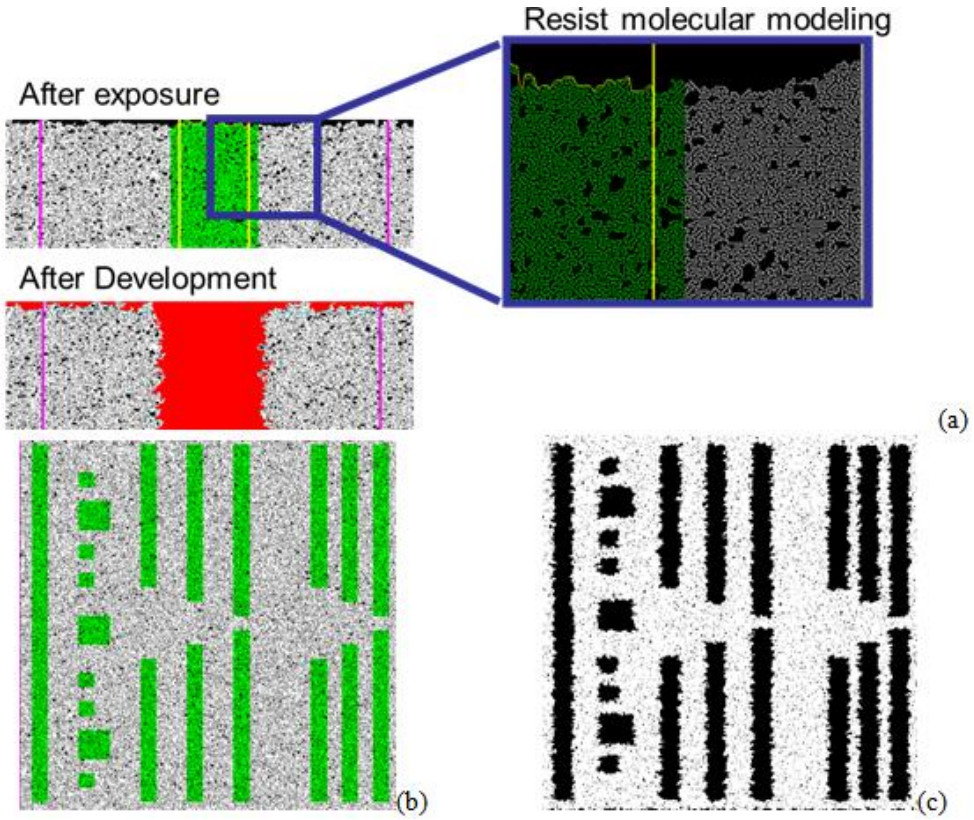


Figure 6. (a) Front view (with resist depth) of the stochastic lithography simulator. Photoresist's polymer chains are modeld as self-avoiding and mutually excluded random walks in this case. The green color represents the acid diffusion area after post exposure bake simulation in the case of chemically ampliefied photoresists. Edge roughness is seen in this case after development. (b) Top-down view of a photoresist area, with acid diffusion profile, (c) after dissolutionFinally, metrology can be performed as well on the developed photoresist profiles for deep understanding and quantification of the overall fabrication process. The metrology software is also developed in house, in matlab and incorporates image analysis and advanced edge extraction techniques and statistical analysis [5], [6]. Figure 7 shows compactly, the metrology's work in order to obtain the edges of the layout. Then any kind of analysis on the edges can be programmed.

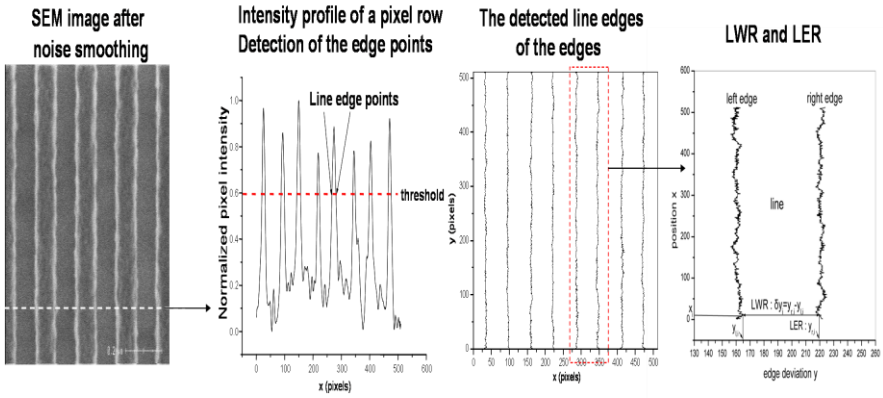


Figure 7. Example of the metrology process (in this case on an actual scanning electron microscopy image of photoresist lines spaces).

Using this simulation tools, one is able to simulate and quantify quite complex layouts as seen in Fig. 8, where the metrology on the energy deposition and on the final photoresist pattern can reveal the effects of the processing parameters on the final layout. This information could then be directed to layout designers to close the loop of design-fabrication process.

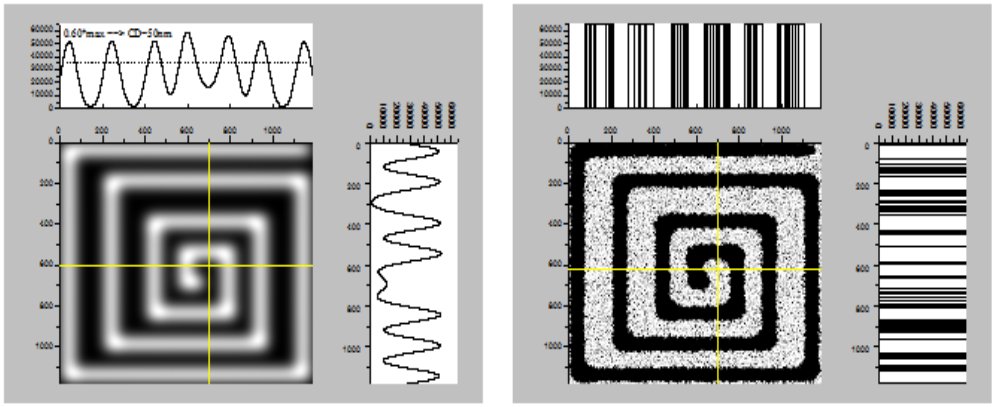


Figure 8. (a) Metrology on electron-beam energy deposition profile. (b) Metrology on the photoresist profile, after stochastic lithography simulation.

Finally, the in-house developed software-Graphic User Interface (GUI) for the whole analysis is seen in Fig.9.

III. Conclusion

Design and fabrication of integrated circuits are so far performed by groups of individuals that do not have much interaction. In this work a simulation flow was presented that enables a circuit designer to obtain both qualitative and quantitative idea of the fabrication aspects of his design, through specific modeling of each stage of the lithography process. Electron-beam exposure is used to define very fine feature on a circuit mask. The information obtained from the metrology of the finally fabricated layouts can be directed back to the designer in order to modify appropriately his design.

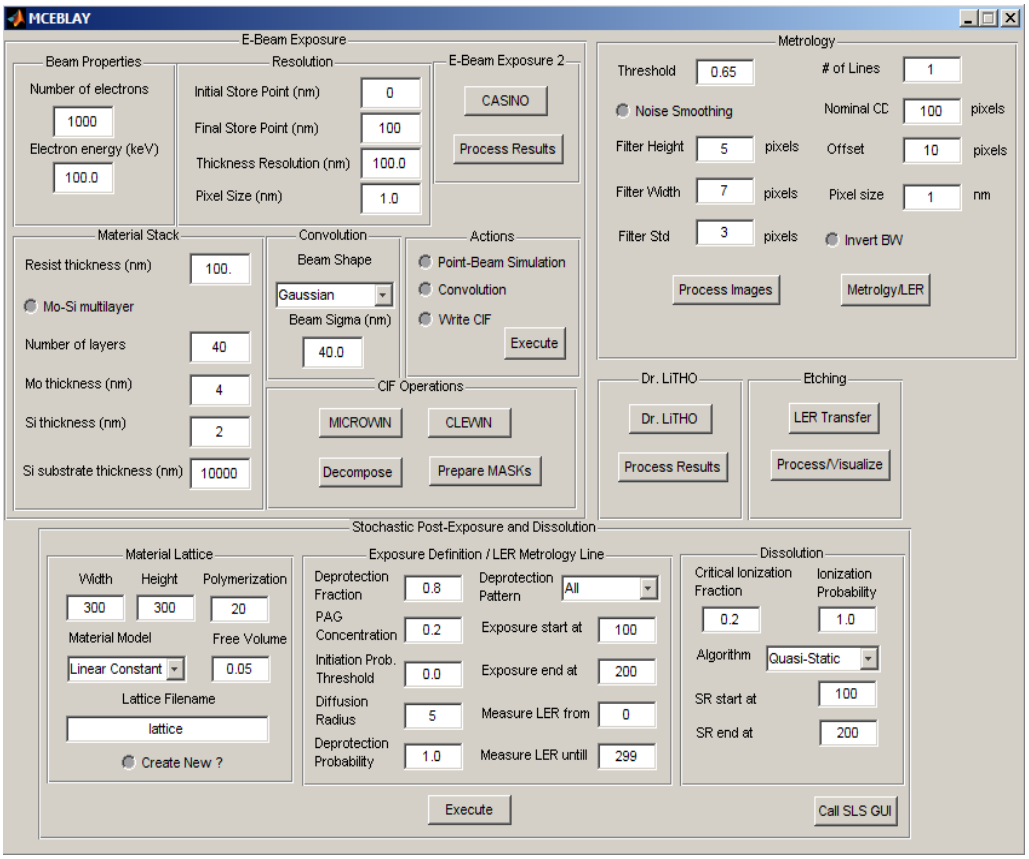


Figure 9. GUI of developed software for CIF decomposition, electron-beam simulation lithography, and metrology of developed patterns.

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