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Impact of Priority Based Heading One Detector on H.265/HEVC

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Abstract : *In this paper, the latest standards of video-coding H.265/HEVC is designed with highly efficient video decoder. The contrary decoding techniques are brought to bear at various stages to emend the data throughput and coding efficiency. The priority based heading one detector is used to the efficiency of decoder. Simulation and synthesis is done by Xilinx 14.7 ISE and implemented on Virtex5 FPGA. The simulation result shows the computational period of decoder architecture is scale down with optimized power reduction and speed.*

Keywords – *Baseline Decoder, CAVLC Decoder, Heading one detector, H.265/HEVC, priority Detector*

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I. Introduction

The combined effort of the iut-t video coding expert group and iso/iec moving picture expert group(mpeg) is the current standard highly efficiency(hevc). The main purpose of this paper is adapting and testing the priority based heading one detector from h.264 to h.265 video codec standards, and assisting the industry community to use standards, the standardization efforts. Paper organization is as follows: section ii explains the complete design flow of hevc. Section iii explains the cavlc decoder in h.264 and impact of priority based heading one detector on h.265. Section iv represents a performance analysis of heading one detector and conclusion in the last section.

H.265/HEVC design process flow

The H.265/HEVC are one of the standards which are designed to achieve multiple tasks and goals, which also includes the coding efficiency, ease of transport system integration and data loss resilience, and also have great ability of implementations using parallel processing architectures.

In the video coding layer of H.265 variation have been made keeping in mind the end goal to accomplish noteworthy compression productivity when contrasted with past principle.

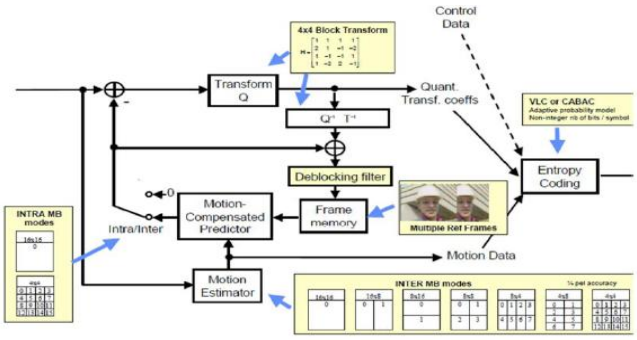

Figure 1: Architecture of HEVC.

The HEVC architecture block consists of:

- Integer Transformation block,
- prediction block: intra & inter prediction
- scalar quantization
- Encoder block &
- Decoders block

In H.265, initially the source video is distributed into bits of luma and chroma. Then the improvement approximation and check, utilized the man handle transient and special redundancies. By the change coding, quantization and entropy coding are related in sequential, which at long last make the yield bit stream. This can be utilized to convey over structure or set away with visual or appealing limit gadgets. The whole number change square, forecast piece and scalar quantization pieces.

II. Background Work

Initially look into the heading one bits of information in entropy coding. In context of the recognition, a need based heading one marker is then anticipated.

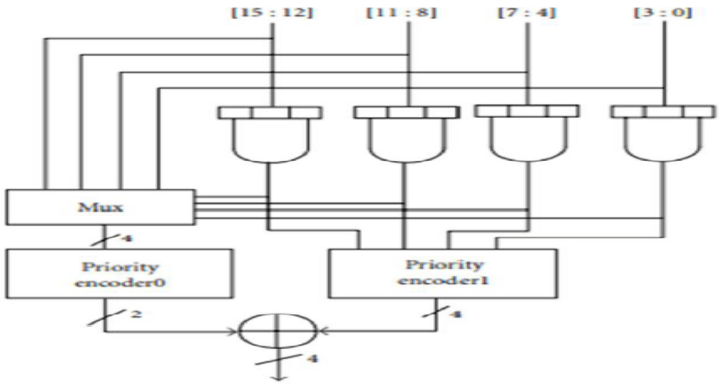

Figure 2 : Evenly partitioned detector

Regardless of the way that there are a couple of diagrams in writing overseeing Exp-Golomb or CAVLC translating, few of them said how heading one area was made sense of it. The essential reference setup is established in. It proposed a locator that comparably parts the sense of duty regarding 4 sub words. From each sub word, the proximity of "1" is perceived. Then these outcomes will make sense which sub word ought to be likewise attempted, as appeared in Figure 2.

Need encoder0's yield shows the situation of "one" in the sub word, while require encoder1's yield demonstrates which sub word has the heading one. Truly, it's 2 level encoder and can't keep running in parallel. Encoder1 picks a sub word in light of need where part [3:0] has the most raised need and part [15: 12] has the scarcest need. As exhibited encoder1's sign, encoder0 picks one right sub word out of 4 and encodes the heading "1" in the picked sub word as the last heading one site.

With a specific extreme target to consider the whole bit stream analyzing procedure where entropy unraveling is gone along with, we built up an unusual state system appear, imitating control and correspondence certifiable video deciphering. Its yield veered from JM9.4 programming with insist cure work. The system indicates has inside kiosks to check the aggregate no of Exp-Golomb codes and CAVLC codes which require heading one exposure. It comparably has specific hostages to measure of these codes in various heading one point. 5 unmistakable test accounts, termed as akiyo, news and car phones, and foreman, with QCIF 300 bundling strategies at 30 22fps are utilized. The quantization constraints set to 22, 25, 28, 32, and 36, freely which are encoded by JM programming. The honest to goodness outline of heading one's location was thus gotten by preoccupation with these information bit streams The intraframe and interframe have to some degree phenomenon heading one quantifiable position rate since for the most part the intraframe has all the more holding up data and requires more CAVLC decoding exertion.

For instance, private interframe, guides undefined toward or in excess of 10 start to have appropriate around 0 (under 0.01%) codes scrambling, while for intra sort out, this inspiration driving confinement is incremented to a high location it shows the particular positions 14 and 15 have around 0 codes dispersal in any case, both intra and interframes share a proportionate inclination of the location is, the fewer open entryways that a heading one is established.

III. proposed architecture

This paper is an adaption or extension of priority based heading one detector from H.264/AVC [1], [2], to H.265/HEVC decoder design. The 16-bit input is non-uniformly divided into three sub-detector with individual enabling control signal, as shown the below architecture (figure. 3).

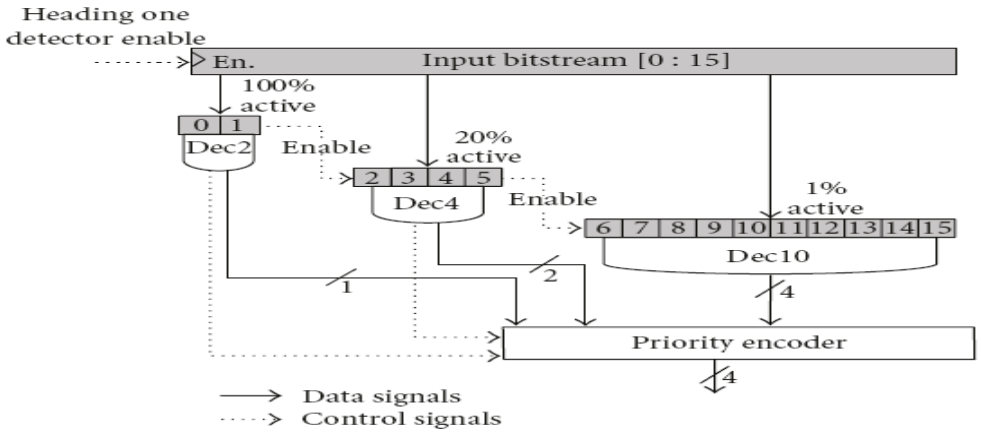

Figure 3: Heading one detector architecture [1]

From the examination, we reason that the condition of heading one no uncertainly occurs about the 2nd data bit (position = 1). The initial two positions (position0 + position1) address basically 80% of all situations and initial 6 positions (position0 + ⋯+ position5) address practically 99%. Therefore we recommend a need based non-uniform package heading one discoverer where data 16bits are separated into three uneven sub detectors and each sub detector can be especially drawn in and debilitated. Figure 4 displays the anticipated plot.

In our outline, input bit stream from bit stream buffer is organized by an "enable" flag. On the off chance that present code word needs heading one location, the entire 16bits are empowered and gone to the heading one indicator, else the finder is handicapped to decrease superfluous exchanging. The whole locator is divided into three sections, every one of which handles an alternate lump of information bits with shifting need. Dec2, which has the most noteworthy need, frames the initial two data bits and is dynamic every one of the chance to recognize whether there is a "1" and it's looking at location (just 1st bit location or 2nd bit location). If "1"is found in dec2, which flags a convincing distinguished proof regarding the heading "one" in a codeword, the position data is send to the last require encoder to influence a going to place. Meanwhile, the last require dec4 and the most immaterial dec10 are obstructed to spare control.

Then again, there is 20% believability that dec2 will dismissal to detect a "one" and dec4 will be able along these lines. dec2 and dec4 both can't discover a heading one more once in a while and dec10 will be dynamic yet has just 1% plausibility. Regardless, if the main decoder which looks [3:0] finds a "1", paying little notice it what the possible result of the other three decoders is, one can expect that the initial "1" is in bits [3:0].

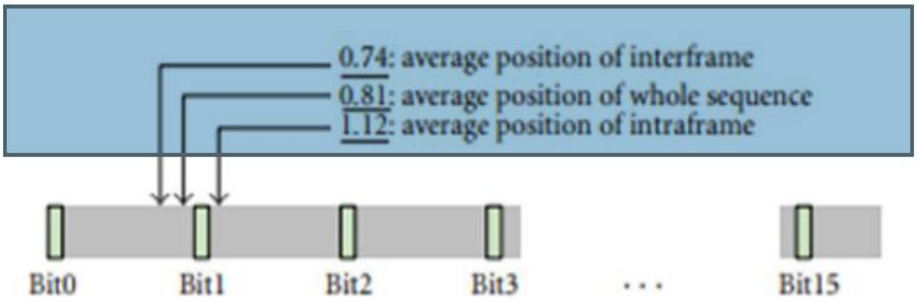

Figure 4: Average heading one position [1]

IV. performance analysis

H.265/HEVC decoder is implemented on FPGA Virtex5 with verilog HDL, simulation and synthesis is done by using Xilinx 14.7 ISE. Akiyo video input with 300 frames QCIF is used for the decoder, which will shows the following results. In particular this paper focused on priority based heading one detector statistical results, found to be more efficient than the existing one, in terms of area, power and propagation delay [table1].

TABLE: 1 Synthesis output of heading one detector

Supply voltage	1.0V
Maximum frequency	250MHz
Number of Slice LUTs (Detector)	11
Number of slice LUTs (Decoder)	157
Dynamic Power (Detector)	0mW

Dynamic power (Decoder)	88mW
Propagation delay (Decoder)	12.94ns
Propagation delay (Detector)	6.15ns

Video sequence is read from the circular bit-stream buffer as 16-bit data and given for statistical computation of heading on detector, where starting from the MSB bit if binary bit '1' found in first two bits then 100% efficiency will be gained and need not proceed for the further calculation and hence computation speed will be enhanced as show in simulation results (fig 5).

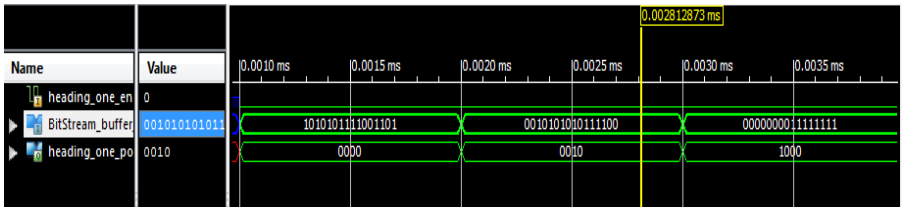

Figure 5: Simulation results of heading one detector.

The further following results shows the area optimization (fig. 6) and Register transfer logic (RTL) Schematic of heading one detector (fig. 7) and figure 8 shows the internal logical structure of the same.

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Device utilization summary:
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Selected Device : 5vlx50tff1136-1


Slice Logic Utilization:
 Number of Slice LUTs:                    11  out of  28800     0%
    Number used as Logic:                 11  out of  28800     0%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:      11
   Number with an unused Flip Flop:       11  out of     11   100%
   Number with an unused LUT:              0  out of     11     0%
   Number of fully used LUT-FF pairs:      0  out of     11     0%
   Number of unique control sets:          0

IO Utilization:
 Number of IOs:                           21
 Number of bonded IOBs:                   20  out of    480     4%
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Figure 6: Device utilization of heading one detector

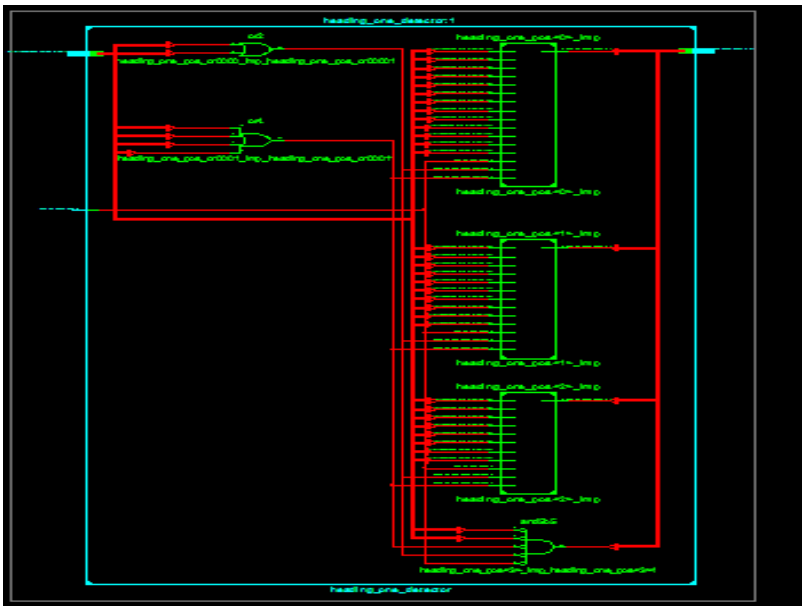

Figure 7: RTL schematic of heading one detector

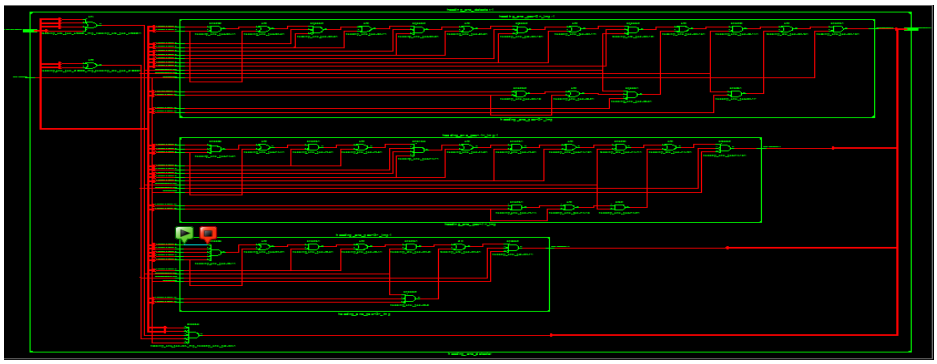

Figure : 8 Internal stucture of heading one detector

V. Conclusion

This paper describes the implementation of H.265/HEVC baseline decoder architecture and priority based heading one detector to enhance the throughput and reduce the power consumptions. By using the variant design of entropy decoder the speed of conventional decoder is enhanced. Priority based heading one detector exploits the statistical results of detecting output in partition the input bit-stream into three parts of heading one decoding detector. The low power techniques like clock gating, memory access reduction pipeline and parallel, optimization based statistical based input are used which are suitable for the battery power video displays. The proposed implementation has successfully verified by FPGA development board of proposed H.265 decoder.

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