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FPGA Based Embedded System For Plasma Diagnostics

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Abstract*: Speed, reliability and flexibility are the essential requirements for achieving high performance in various applications of Physical and Engineering Sciences. FPGA's are considered to be the ideal devices for maximizing the efficiency and productivity of the system. This paper discusses the development of FPGA based fast acquisition system to determine the plasma characteristics using Langmuir probe in a plasma chamber. The plasma is created using Radio Frequency (RF) power input, operating at a frequency of 2MHz. The RF power pulse repetition rate (PRR) is 2 Hz with ON time of 0.5 msec. The FPGA based embedded system has been prototyped using Very-High-Speed Integrated Circuits Hardware Description Language (VHDL). The FPGA based design consists of various interface modules like an ADC, Pre-amplifier, RS-232 Interface and stepper motor controller for alignment of Langmuir probe. A Graphical User Interface has also been designed using LabVIEW to control, automate and store acquired data remotely.*

Keywords*: FPGA, VHDL, Embedded System, Graphical User Interface*

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I. Introduction

RRCAT has developed H^- ion source which is capable of delivering 12 mA ion current at 50 keV to continue the work on Indian Spallation Neutron Source (ISNS). The Hydrogen gas is being used to create H- ions in plasma using the Radio Frequency (RF) ionization technique, 2 MHz RF source has been used. The RF based Ion source setup uses the electric field to further extract and accelerate the generated H- ion inside the plasma chamber. The pulse plasma with PRR 2 Hz has been generated using RF ionization technique. H- Ion current beam quality depends on the quality of the created plasma. To maintain the beam quality, it becomes mandatory to monitor the plasma parameters to tune the various parameters for required beam profile.

The plasma diagnostics has been playing a crucial role by measurement of plasma properties to enhance the plasma quality and hence the H- Ion beam for further research and development in the field of ISNS. The embedded system design discussed in this paper considers Langmuir probe as an analog transducer to perform active plasma diagnostics and FPGA as custom designed hardware for control, monitoring and data acquisition. The Langmuir probe helps in determining the fundamental plasma properties and thus measures the plasma parameters like floating potential, plasma potential, electron temperature, electron density and ion density etc.

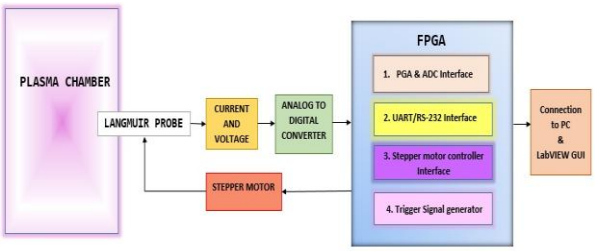

Fig. 1 Block Diagram

The embedded system designed using FPGA offered the advantage of high speed and improved flexibility over the microcontroller based embedded system. The designed digital hardware has been implemented in Xilinx Spartan 3AN development board using VHDL as the programming language.

The main design components included a programmable gain amplifier, an analog to digital converter, RS-232 (UART) and stepper motor controller. The graphical user interface has been developed using LabVIEW to perform remote control and high-speed data acquisition of various signals.

II. Data Acquisition Using FPGA

An Embedded system is designed to perform the acquisition of the real-time signals. Its development involves the design, simulation, and Implementation of various sub-modules in FPGA for plasma characterization of H- ion source using Langmuir probe.

The hardware components have been designed using VHDL programming language. The designed interface modules are Analog to Digital Converter (AD-7606-4, LTC-1407), Programmable Gain Amplifier (LTC-6912), Stepper motor driver and Universal Asynchronous Receiver and Transmitter along with Switches and LEDs for control and indications. The data is supposed to be captured during the on time of the pulse generated by the H- ion source. The analog to digital converter (AD7606-4) samples the captured data at a sampling rate of 200 Ksps. The data is stored in the memory of the FPGA and can be sent to the computer using RS-232 serial communication protocol for further processing.

III. HARDWARE IMPLEMENTATION AND RESULTS

The individual modules created using VHDL were simulated and verified using Xilinx EDA tool. The simulator created a virtual environment to test the concept of the design. The test benches were written for each interface module using VHDL and then the stimulus signals were applied to test the functionality of the design. The simulation results were observed on ISim simulator by Xilinx.

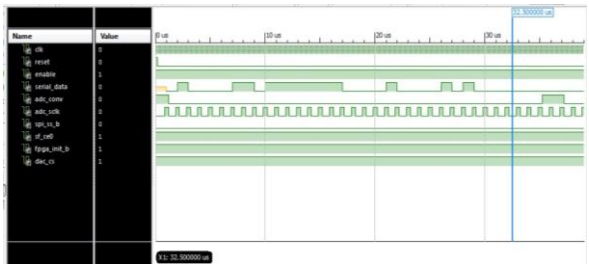

Fig.2 Simulation for ADC

The simulation results for analog to digital Converter Interface have been shown below in fig.2.The converted signal in ADC (adc_conv) enables the conversion of the data. When the convert signal goes low, the data conversion is done with respect to the SPI clock. A sequence of 34 clocks exists between two convert signals. Here spi_ss_b, sf_ce0, fpga_init_b, dac_cs indicate the SPI bus signals for other devices on board and their values are set accordingly to avoid bus contention. The result of the digital data was also observed on the led's available on the board.

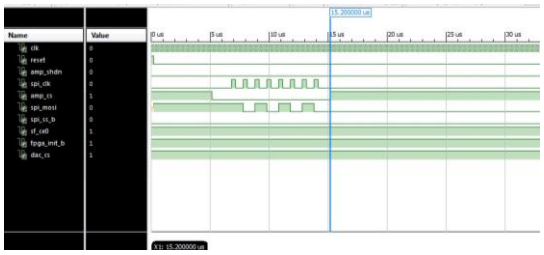

Fig.3 Simulation for Pre-amp

Fig.3 shows the simulation results of a preamplifier. The SPI clock has been generated and as soon as the chip select (amp_cs) goes low the value of the gain is set inside the gain register. The gain register is 8 bits, so 8 clocks are needed inside the preamplifier chip select to load the value. The amp_shdn is the shutdown signal for the Programmable Gain Amplifier. For the pre-amp also the spi_ss_b, Sf_ce0, FPGA_init_b, dac_cs are the SPI bus signals for other devices on board. The value of these signals is set accordingly to avoid bus contention. VHDL module for the stepper motor was simulated, the pulse signal was given as the input to the motor.

Fig.4 Simulation for Stepper Motor Controller

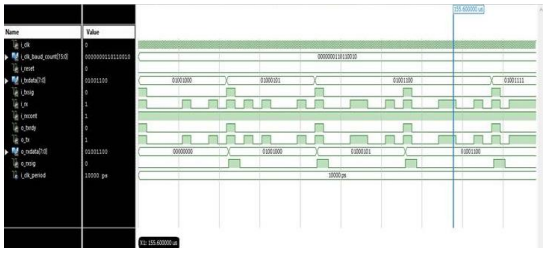

Fig.5 Simulation for UART (RS-232)

In fig. 4 the sequence for the rotation of the motor can be observed on the seq_out signal. If the direction signal is set low, the sequence of the motor will get reversed.The UART interface designed was also tested where the input from the RX is sent to the TX to test the echo back (seen in fig.5).The UART was designed to work for eight data bits, zero parity and one stop bit. The signal I_clk is sixteen times the baud rate and I_clk_baud_count is the number of cycles of I_clk between baud ticks. The I_clk_baud_count is used to define the baud rate for the receiver and the transmitter. The implementation gave the actual realization of the design. The digital oscilloscope was used to check the internal signals generated by the FPGA. The implemented design was tested using ADC board and Stepper Motor Driver board which was designed and developed by RRCAT. A Graphical User Interface has been designed using LabVIEW to control and store acquired data.

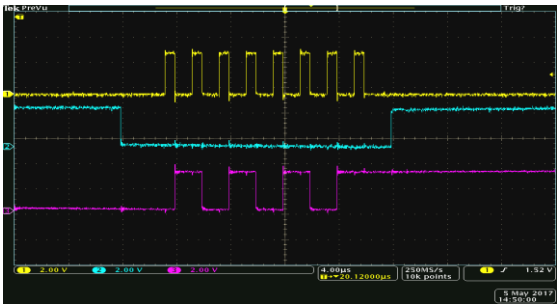

Fig.6 Implementation for Pre-Amplifier

Fig.7 Implementation for ADC

Fig.6 shows the signals of the pre-amplifier. The SPI clock (Yellow) was seen along with the chip select (Blue) of the amplifier and the MISO (Master in serial out) (Purple) data was also observed. The gain of the PGA is set with respect to the SPI Clock. The implementation of the ADC is shown in fig.7. The ADC convert signal (Blue) goes low for 34 clocks. The serial data (Purple) that the chip generates is also seen with respect to the SPI clock (Yellow). The stepper motor implementation shows the results of the sequence (Blue, Purple and green) (only 3 bits are shown here) generated for its rotation in fig.8. The sequence along with the pulse (Yellow) can be observed. If the direction of the motor is set low then the sequence will run in opposite direction.

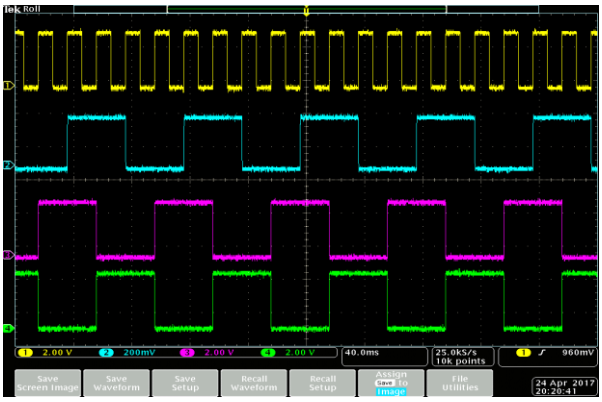

Fig.8 Implementation for Stepper Motor Controller

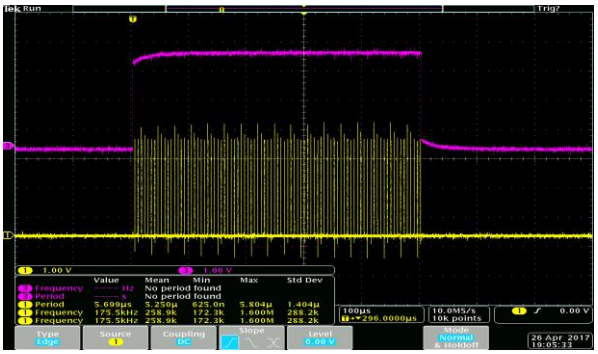

Fig.9 Data acquisition samples obtained within the on time of 0.5 msec

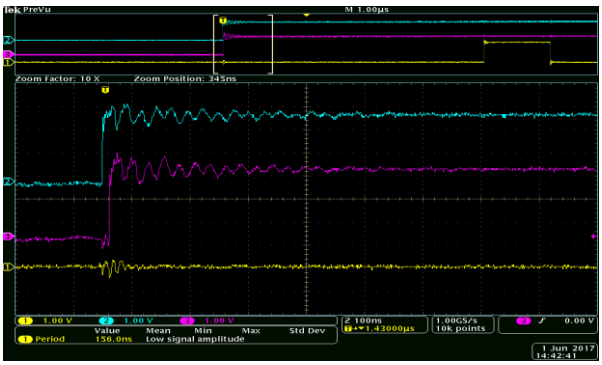

Fig.10 Synchronization of an external trigger signal with acquisition signal

The results of data acquisition were observed on the oscilloscope fig. 9. The trigger signal **(Purple)** of 2Hz frequency and 0.5 msec on time was generated using VHDL. Multiple samples **(Yellow)** of the data can be acquired during the on time of the trigger signal. The fig.10 shows, the adc_conv **(Yellow)** and the acquisition enable signal (**Purple**) have been synchronized with respect to the External trigger signal **(Blue)**. The delay between the external trigger and acquisition enable signal is found to be less than 20 ns and it can be reduced by increasing the synchronization frequency.

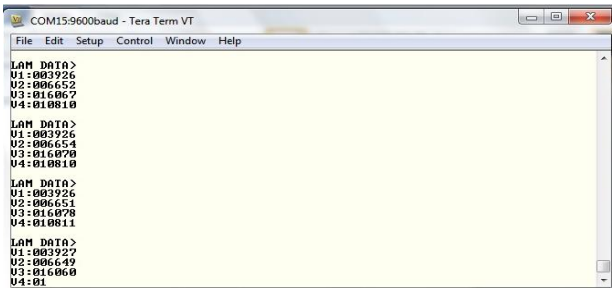

Fig.11 HyperTerminal displaying real time values

From Fig.11 we can see that V1 (channel one) is 3926 so after performing the conversion we get the digital equivalent of the analog voltage applied.

$$\frac{3926}{32767} \times 10 = 1.198156 \text{ volts}$$

Similarly, the conversions for V3 and V4 can be done
V3 (channel three) is 16067

$$\frac{16067}{32767} \times 10 = 4.9034089 \text{ volts}$$

V4 (channel two) is 10810

$$\frac{10810}{32767} \times 10 = 3.2990508 \text{ volts}$$

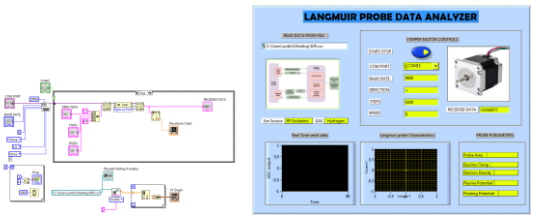

Fig.12 GUI Block Diagram and Front Panel in running mode

The GUI created using LabVIEW is also able to capture the correct data, this can be seen in the Fig.12.This verifies the functionality of the interfaced modules and the working of the GUI.

IV. Conclusion

An embedded system design using an FPGA has been successfully developed. The design of embedded system involves design, simulation and Implementation of various sub-modules in FPGA for plasma characterization of H- ion source using Langmuir probe. VHDL programming language has been used to interface the peripherals with FPGA. The designed controllers in VHDL include UART, PGA (LTC-6912) and ADC (LTC1407), Stepper motor controller along with Switches and LEDs for control and indications. The communication link with the graphical user interface and development board was also verified. The stepper motor control and sample analog voltages have been captured using the designed GUI and displayed. The results captured by the GUI were compared to the results observed on the HyperTerminal. This verified the correctness of Graphical user interface design.

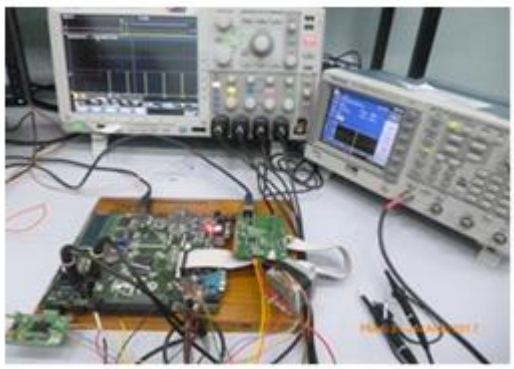

Fig.11 Embedded system Setup

V. Future Scope

Due to time constraints, the task of acquiring the I-V characteristics for Langmuir Probe remains pending. The GUI design can be enhanced to provide more utility to the user.

In this project, the ADC (AD-7606) has been implemented using the serial protocol, which could be configured in the parallel mode to increase the no. of samples in given time, thus increasing the speed of operation. Later the FPGA based embedded system setup can also be integrated with the USB-4000

Spectrometer by ocean optics. Since functionality and feasibility of the proposed work are implemented and tested on Xilinx Spartan 3AN development board along with RRCAT designed boards, later a dedicated custom board can be developed to serve the purpose.

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