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Performance Analysis of FINFET Based 16:4 Encoder and 4:16 Decoder-A Design Perspective

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Abstract: *The growing technology for the silicon chip is becoming a demand day by day to ensure the optimization in area, power consumption and speed in the digital circuits. The CMOS technology is fast growing domain where the analog and digital circuits are designed and fabrication of IC's but still there is tradeoff in area i.e size of CMOS transistor, delay and power consumption. To optimize these parameters, the proposed research work incorporated the 32nm FinFET technology for designing of 16:4 encoder and 4:26 decoder. The comparative study has been done for silicon area, delay and power consumption and it is found that FinFET based encoder and decoder are produced better results. The 16:4 encoder occupied an area of 189.88um2, 4:16 decoder area is -170.04 um^2, power consumption of encoder and decoder are 2.68uW and 1.98uW and their delays are 24.4 microseconds, 19.56 microseconds. All simulation results and analysis are performed on 32um using Cadence Virtuoso software tool.*

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I. Introduction

In the applications such as wireless remote control system, home or industry automation system, health monitoring system, cryptography, robotics, image or signal processing systems, computer graphics, communication networks and digital applications, any type of analog signals is converted to digital signal and vice versa. The sole focus of the signal conversion is information of the signal, which is obtained in digital form using the process of encoding and decoding. The encoding is the process of providing binary equivalent to the information signal and decoding is the process of obtaining data from the coded value. Based on the type of applications, different types of encoders and decoders are available. Specifically, the binary decoders and encoders are used for digital applications in functions of address decoding, seven segment displays and multiplexing or de-multiplexing.

In the design perspective of digital circuits, CMOS technology is the well-established semiconductor technology. As the demand for battery-operated devices have increased due to miniaturization, the low power consumption and less area become the primary requirement of any design. The consequence of scaling down of transistor's dimension end-up in the change of its channel behaviour and increases the leakage power consumption. To achieve low power design, the innovative MOS structure called finFET is used. The benefit of finFET's double gate structure exhibits in the maximization of the gate-to-channel capacitance and minimization of the drain-to-channel capacitance [15]. The main objective of the paper is to design and analyse the performance of 16:4 encoder and 4:16 decoder using finFET 32nm technology node and compare the performance with CMOS 90nm technology node using the metrics: power, delay and area.Presently a day, control scattering assumes a vital job in the structure of VLSI circuits, particularly when there is an expanding pattern of pressing increasingly more rationale components into littler and littler volumes and timing these circuits with higher frequencies. The rationale components are ordinarily irreversible in nature and as per Landauer [16], irreversible rationale calculation results in vitality scattering because of intensity misfortune. This is on the grounds that, eradication of each piece of data disperses at any rate KTln2 joules of vitality, where K is Boltzmann's steady and T is the supreme temperature at which the activity is performed. In the event that Moore's law keeps on being as a result, it is anticipated that by year 2020 this will end up being a generous piece of vitality scattering.

The paper is organised as follows: Section II discussed literature review and related works; Section III discussed the logic circuit of encoder and decoder; Section IV discussed the finFET and CMOS circuit design and its simulation results; Section V discussed the performance comparison and concluded the paper in the Section VI.

II. Literature Review And Related Works

Literature Review

According to International Roadmap for Devices and Systems (IRDS 2016-17), finFET is the key device architecture that could sustain scaling for high performance logic applications [2]. The path towards denser and faster integration of CMOS technologies scaling faces challenges due to the increasing negative impact of the short channel effects. The resulting degradation in the device performance, reliability and increased power consumption forces the device engineers to develop a non-planar, double gate transistor built on a SOI subtract based on the single gate transistor design [3]. The device which uses a thin silicon fin like structure wrapping-up the channel is called as finFET. The advantages of finFET devices are channel control, over scaling, cost effective and negligible short channel effects. Since finFET is the most promising technology than other semiconductor technologies, the digital circuit is designed using finFET devices to provide better performance and low power consumption.

Related works

Many of the researches contributed in the low power design perspective of digital circuits as follows:
AkasheShyam et al. [1] designed CMOS based 2:4 decoder using self-controllable switch technique to achieve low power and high speed performance
Amuthavalli et al. [4, 6, 7, 9, 12] elaborated the design of different digital circuits in CMOS technology and achieved the reduced subthreshold leakage using leakage reduction technique.
T. B. Singha et al. [5] achieved low power solution to CMOS based 4:2 priority and 2:4 decoder in context of adiabatic logic.
Amitraut et al. [8] discussed the performance of 2:4 decoders using reversible logic for low power consumption.
Vanshikha Singh et al. [10] achieved less area and low power in the design of CMOS decoder.
Pranay Kumar Rahi et al. [11] exhaustively discussed the performance of 2-to-4 decoder using 32nm, 45nm and 65nm CMOS technology.
C Y Lee et al. [13] discussed the CMOS based low power encoding technique in the detector application.
SakshiSaini et al. [14] achieved low power using leakage reduction technique in CMOS based encoder.

III. Logic Circuit Of 16:4 Encoder And 4:16 Decoder

16:4 Encoder

A 16:4 encoder is digital circuit which provides binary equivalent (1010101010101010) of any of the asserted input signal (0110010001000001). The truth table of 16:4 encoder is given in equation (1) and its logic circuit is given Fig.1.

The equation (1) shows the number of variables for all digital 16:4 encoder and its inputs lines are $I_{15}I_{14}$ I_{13} I_{12} I_{11} $I_{10}I_9$ I_8 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0 and output lines are O_3 O_2 O_1 O_0. The logic state '1' presents in the Table.1 response is required for the logic state '0' indicates that it is not. The arbitrary items represents in then equation (1) is 'x' and that could be either '0' or '1'. The O_0 O_1 ……$O_4$are the final outputs of the encoder that could response of the given inputs. The output is '0' if there are no inputs i.e all inputs pulses are low. Therefore, encoder outputs are conflicts for the inputs combinations of $I_{15}I_{14}$ I_{13} I_{12} I_{11} $I_{10}I_9$ I_8 I_7 I_6 I_5 I_4 I_3 I_2 I_1 I_0 =0000000000000001. Hence, if $I_{15}I_{14}$ are 11 then I_{15} will be encoded.

From eq. (1), we see that the priority encoder is mainly made up of logic OR and AND functions.

$$O_0 = \overline{\overline{(D_8D_9)(D_{10}D_{11})(D_{12}D_{13})(D_{14}D_{15})}}$$
$$O_1 = \overline{\overline{(D_4D_5)(D_6D_7)(D_{12}D_{13})(D_{14}D_{15})}}$$
$$O_2 = \overline{\overline{(D_2D_3)(D_6D_7)(D_{10}D_{11})(D_{14}D_{15})}}$$
$$O_3 = \overline{\overline{(D_1D_3)(D_3D_7)(D_9D_{11})(D_{13}D_{15})}} \qquad (1)$$

In any case, the OR rationale contained in Y1 and Y0 can't be gotten by coupling the things on the privilege of the articulations specifically in light of the fact that there may be an indistinguishable piece "1" in various sources of info that will actuate staggered powers in the yields Y1 and Y0. Aside from this, no less than two so as are required to accomplish Y0. One is utilized to acquire 2 1 I and the other is utilized to get I3+I2I1. GS is additionally hard to acquire utilizing an AND door in light of the fact that there are an excessive number of sources of info. To stay away from staggered forces, diminish the quantity of SOAs and abstain from utilizing AND rationale for various sources of info, the articulations are altered as shown in Fig.1 (a). and its simulated results are shown in Fig.1 (b).

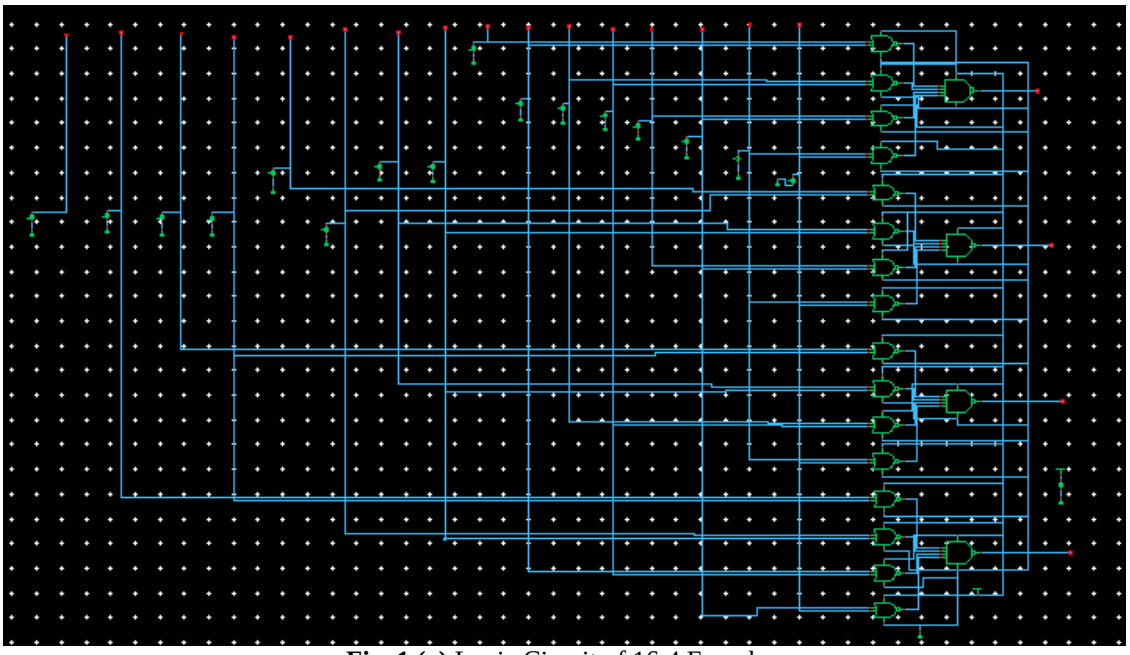

Fig. 1 (a) Logic Circuit of 16:4 Encoder

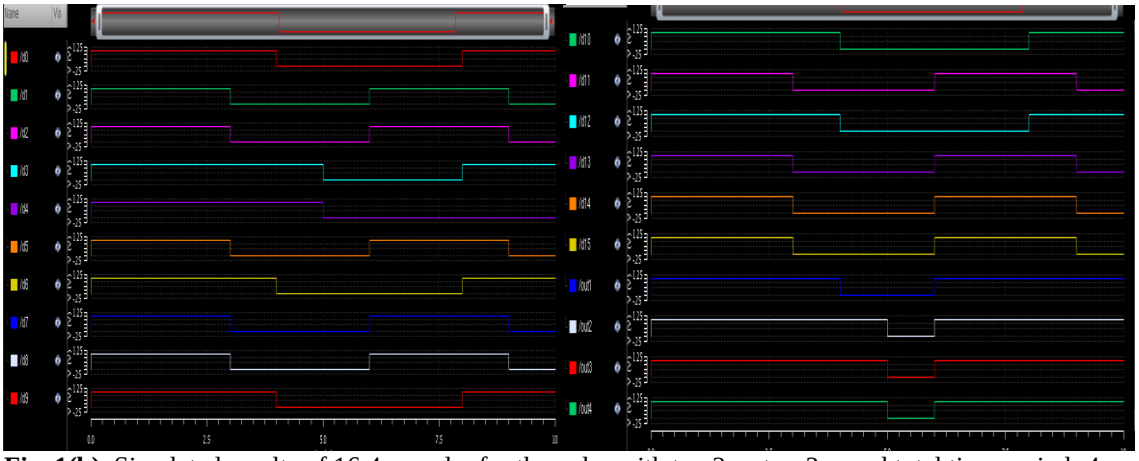

Fig. 1(b). Simulated results of 16:4 encoder for the pulse with t_{on}=2us, t_{off}=2us and total time period=4ns.

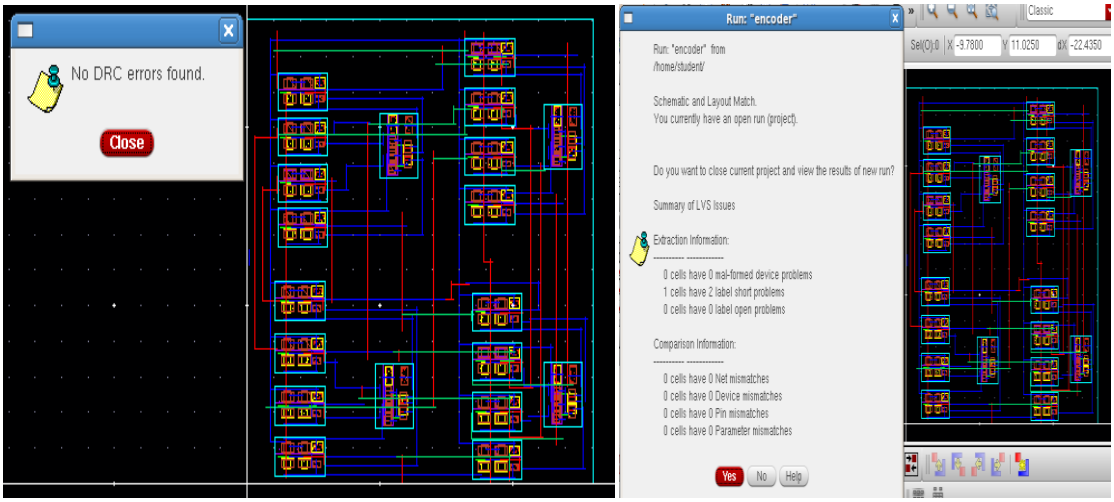

Fig.1(c). Layout design of 16:4 encoder and verification of DRC and LVS for generation of chip level.

The framework arrangement is represented in Fig. 1. As to, the power of the test light I_2 is regulated by the force of the siphon light I_{15} as indicated by the XGM impact in the SOA. At the point when I_{15} is solid

(abnormal state), bearers in SOA1 are vigorously devoured and SOA1 winds up soaked. In this manner, I_{14} can't be enhanced and the yield is "0". Unexpectedly, when I_{15} is feeble (low dimension), no transporters in SOA1 are expended and I_{14} is intensified.The proposed encoder is designed for chip level using 32nm technology in terms of layout and validated the area, power and delay from layout design as shown in Fig. 1(c).

4:16Decoder

A 4:16 is a digital circuit which is used to get the desired signal output from the input code. The truth table of 4:16 decoder is given in Table in 2 and its logic circuit is given Fig. 2.The encoder and decoder also challenge task to carry out complete physical design for that, after adding power supply, the pins were arranged around that outer side of the chip with their placement based on codec functionality. The encoder data input and output bus width lines are carefully placed in order to transfer the information from the encoder to decoder were placed on the upper and lower respectively. The digital physical layout process starts with floor planning and finish with post routing. The complete process around forty two steps to design the complete 16:4 bit CODEC digital physical layout as shown in Fig.2 (c). Finally we have investigated from our design with different parameters to minimize the power, area and timing for battery based devices in multimedia applications and these results are shown in the Fig.2(a). The design is simulated using Cadence NC Launch for the pulse period of t_{on}=2us, t_{off}=2us and total time period=4ns and results are shown in Fig. 2(b).

Decoder Design equation:

Inputs (A,B,C,D)

Output: ($q_0q_1q_2q_3q_4q_5q_6q_7q_8q_9q_{10}q_{11}q_{12}q_{13}q_{14}q_{15}$)

$q_0 = (\bar{A}\bar{B}\bar{C}\bar{D}),\ q_1 = (\bar{A}\bar{B}\bar{C}D),\ q_2 = (\bar{A}\bar{B}C\bar{D}),\ q_3 = (\bar{A}\bar{B}CD),\ q_4 = (\bar{A}B\bar{C}\bar{D}),$
$q_5 = (\bar{A}B\bar{C}D),\quad q_6 = (\bar{A}BC\bar{D}),\ q_7 = (\bar{A}BCD),\ q_8 = (A\bar{B}\bar{C}\bar{D}),\ q_9 = (A\bar{B}\bar{C}D),\ q_{10} = (A\bar{B}C\bar{D}), q_{11} = (A\bar{B}CD),\quad q_{12} = (AB\bar{C}\bar{D}),\ q_{13} = (AB\bar{C}D),\ q_{14} = (ABC\bar{D}),\ q_{15} = (ABCD)$

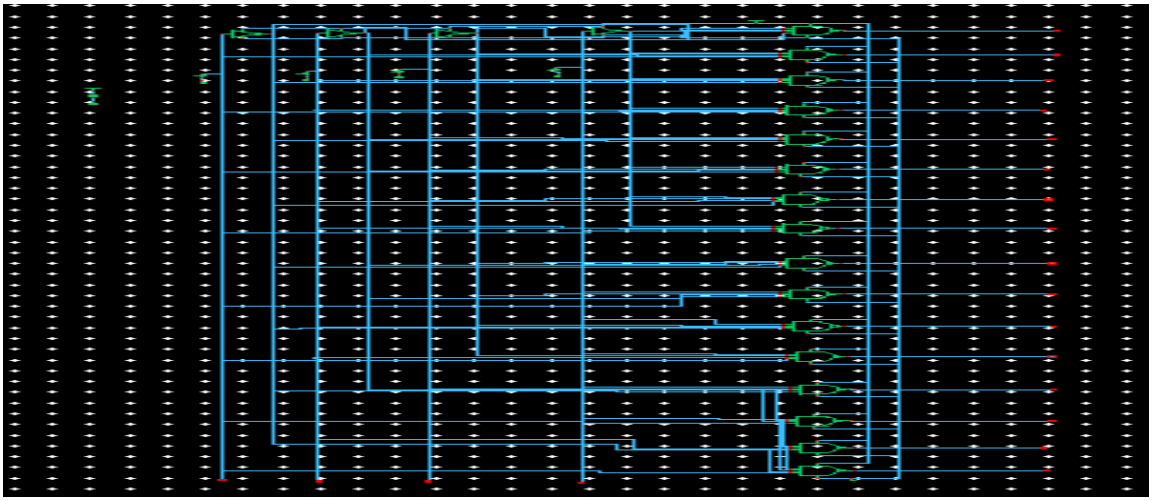

Fig. 2 (a). Logic Circuit of 4:16 Decoder

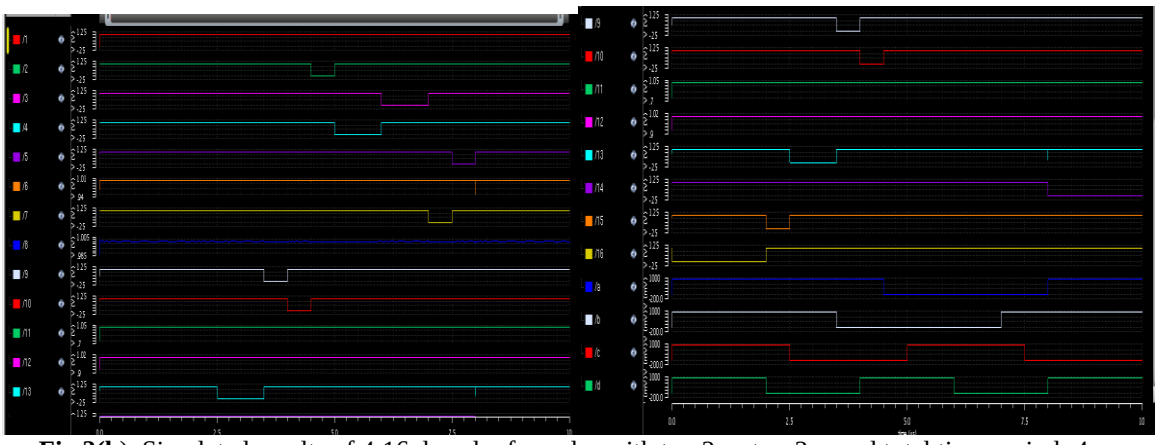

Fig.2(b). Simulated results of 4:16 decoder for pulse with t_{on}=2us, t_{off}=2us and total time period=4ns.

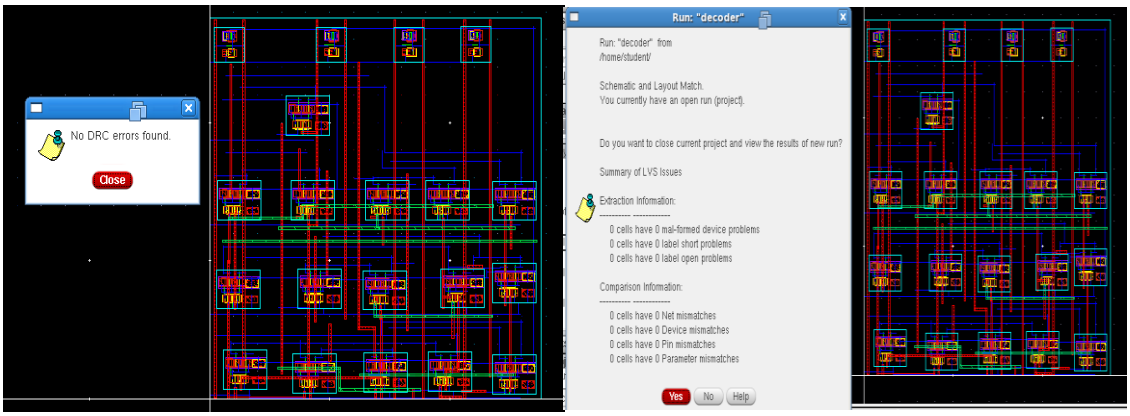

Fig. 2(c). Layout design of 4:16 decoder using 32 nm FinFET based and its DRC and LVS Verification.

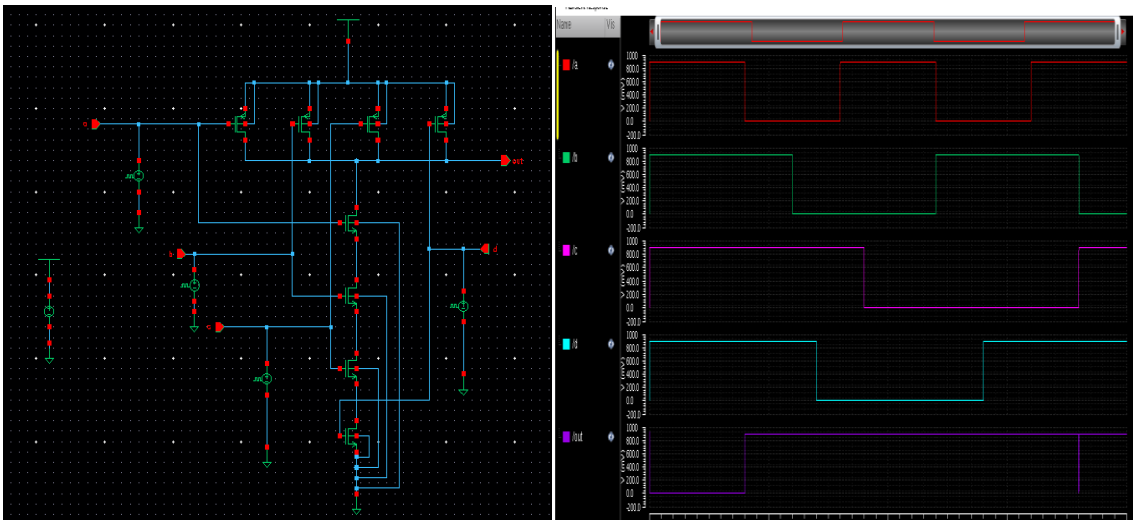

Fig. 3 (a). 4-bit input NAND gate which is used for the design of encoder and decoder and its simulated results for pulse width of 10nm, t_{on}=4um and t_{off}=4um.

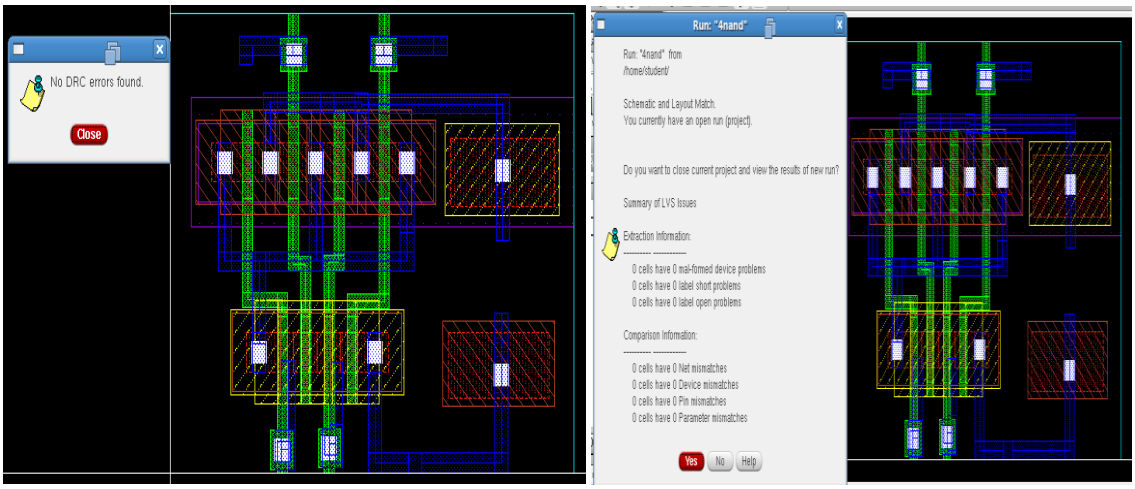

Fig. 3 (b).Layout design of NAND gate and its DRC and VLS Verification

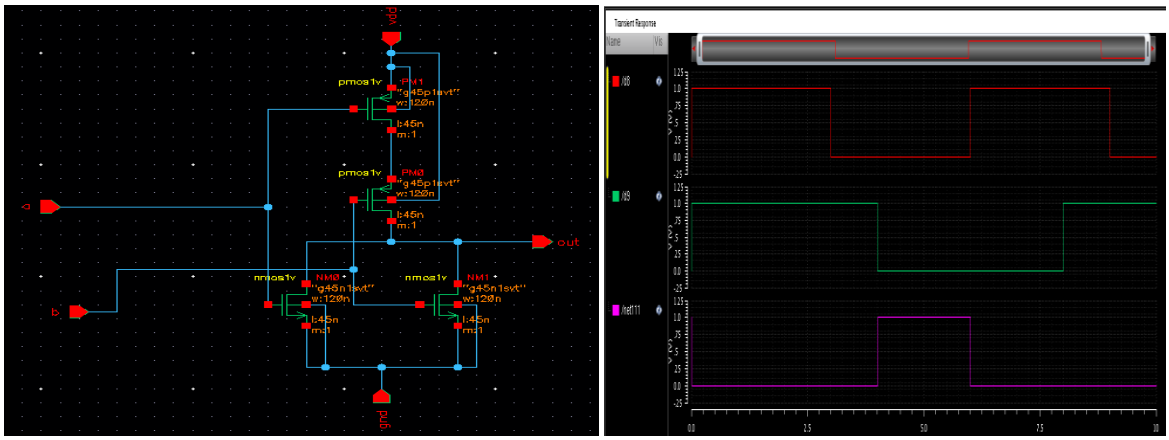

Fig. 4(a). Schematic diagram of 2 input NOR gate and its simulated results

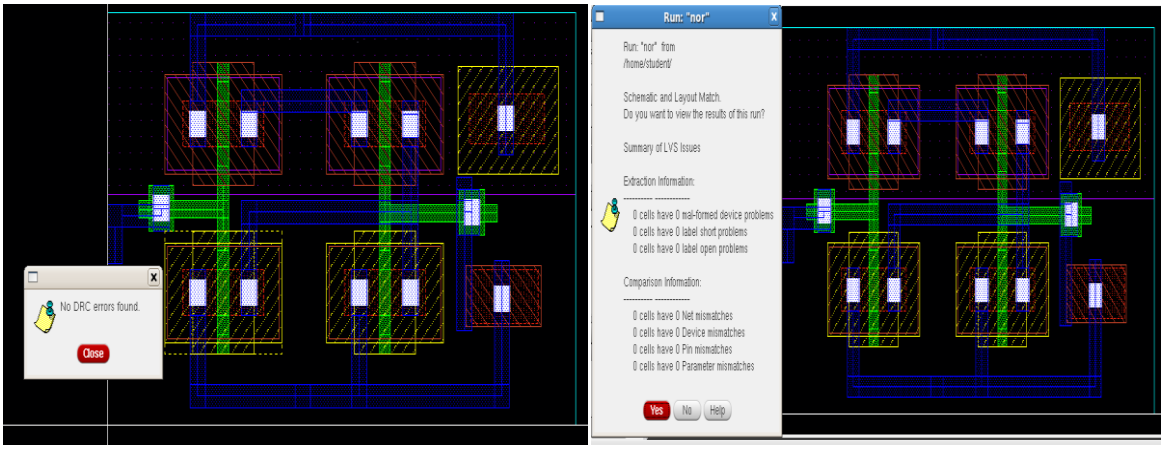

Fig.4(b). Layout design of NOR gate and its DRC and LVS Verification

IV. Performance Comparision

Component	CMOS 45nm		finFET 65nm		finFET 32nm	
	Power(uW) [16]	Area (um^2)[16]	Power (uW)	Area (um^2)	Power	Area (um^2)
NAND (4input)	56.7	732.1	76.5	856.3	108.54pW	2.56
NOR (2-input)	83.5	864.4	95.3	1034.4	31.39nW	2.01
4:16 Decoder	329592.263	3237	358542.713	3628	1.982uW	170.04
16:4 Encoder	362858.23	3409	474625.33	4215	2.68uW	189.88

Table.1 Comparative table between existing and proposed for three different technologies

The Encoder and decoder aredesigned has been effectively actualized with the SOC Encounter apparatuses with 32nm innovation of computerized physical format and the activity of encoding and translating the information from Cadence RTL Compiler code level information, to entryway level and transistor level execution, combination results with structure measurements like power, region and timing completed and contrasted and existing structures. Table-1 Synthesis of Physical Layout Results Implemented in SOC Encounter Tool.

V. Conclusion

The all-advanced 16:4-piece encoder dependent on various heartbeat signals at 20 Gbit/s is proposed and tentatively exhibited utilizing the 4-bit inputs NAND impact in SOAs fell with detuning NOR entryways. As the last outcomes, right and clear transient waveforms and open eye designs were acquired, and elimination proportions surpassing 15 dB were accomplished. An increasingly confused computerized need encoder circuit with a higher activity bit rate could be acknowledged by falling the 16:4-piece need encoder 4:16 decoder. In addition, the proposed plan can possibly be substantial scale incorporated.

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